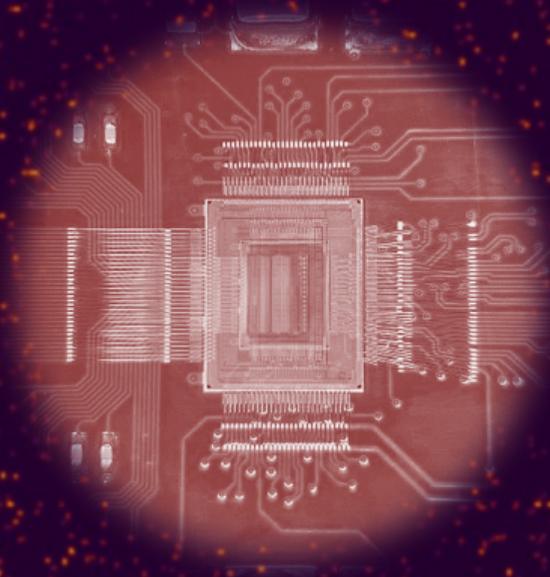


2025/06/27

Reconfigurable on-pixel analog and mixed-signal IPs

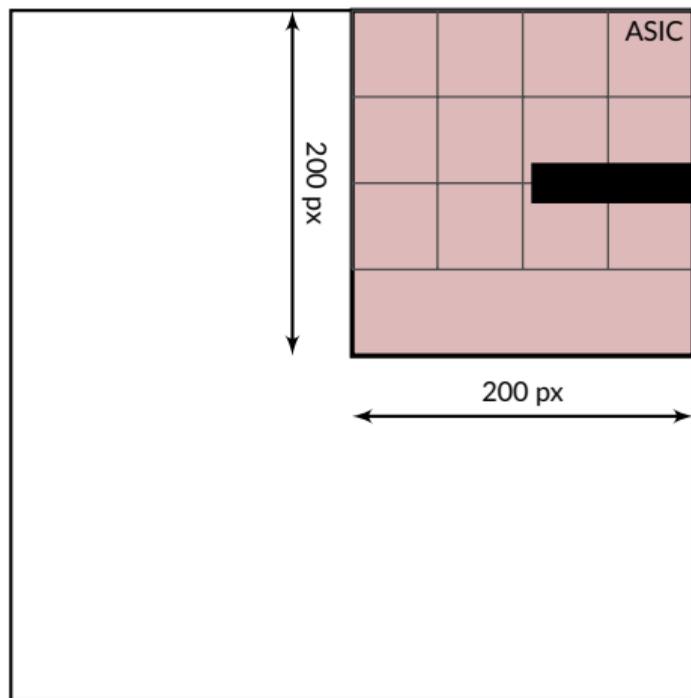


Llorenç Fanals-i-Batllori^{1†} on behalf of the TID-ID-IC team

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Challenges [arXiv:2312.07602]



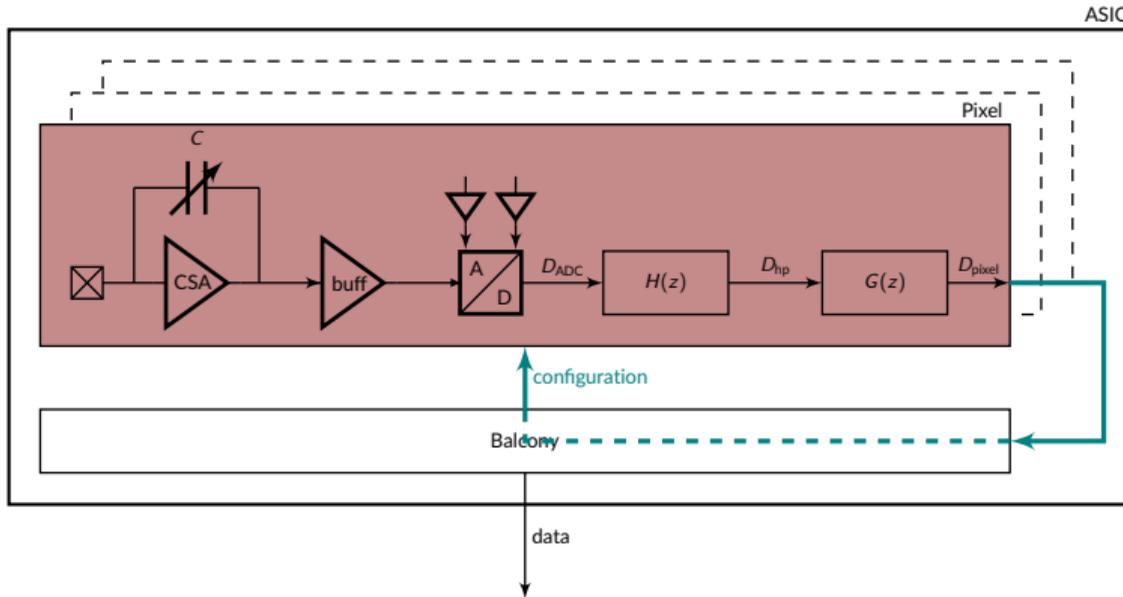
$$200 \text{ px} \cdot 200 \text{ px} \cdot 12 \text{ bit} \cdot 1 \text{ MS/s} \approx 500 \text{ Gbps ?!}$$

=

20,000 4K movies

NETFLIX

System overview

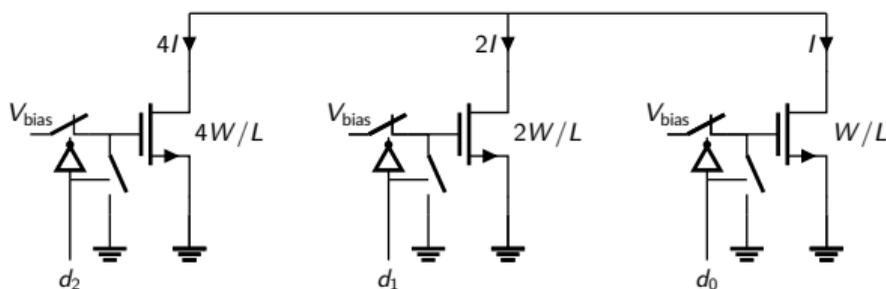
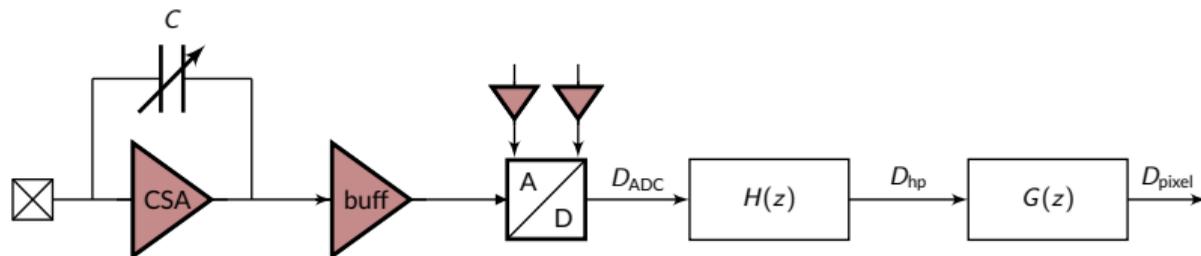


- A data-driven system can reduce the amount and output data and improve its quality.
- Reconfigurable analog and mixed-signal IPs are mandatory.

Potential pixel capabilities

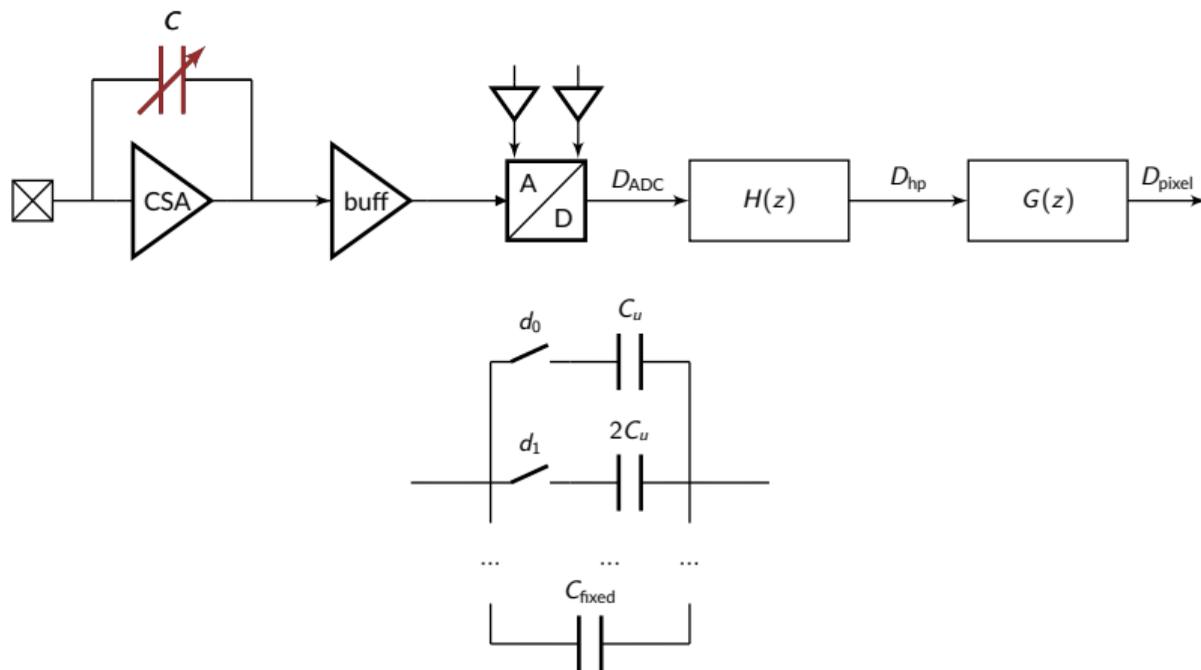
- Adaptive spatial resolution.
- Adaptive gain.
- Adaptive filtering.
- Adaptive range.
- Adaptive binning/quantization.
- Adaptive rate.
- Adaptive threshold.
- Adaptive power consumption.

Analog configurability



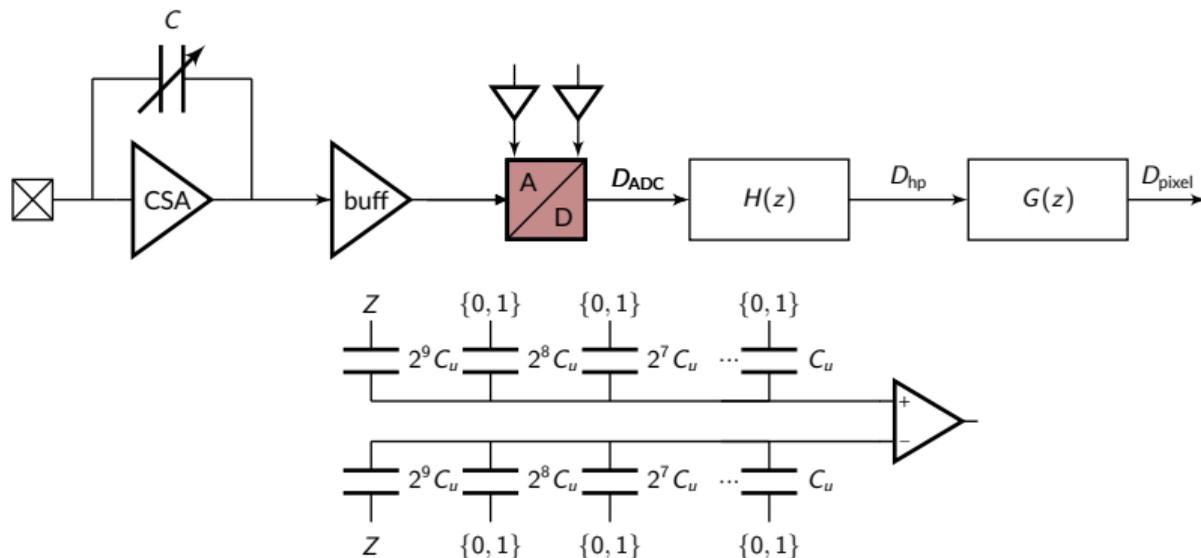
- Binary-weighted current sources: $I_{total} = I(4d_2 + 2d_1 + d_0)$.
- Tradeoff between speed and power consumption.

Analog configurability



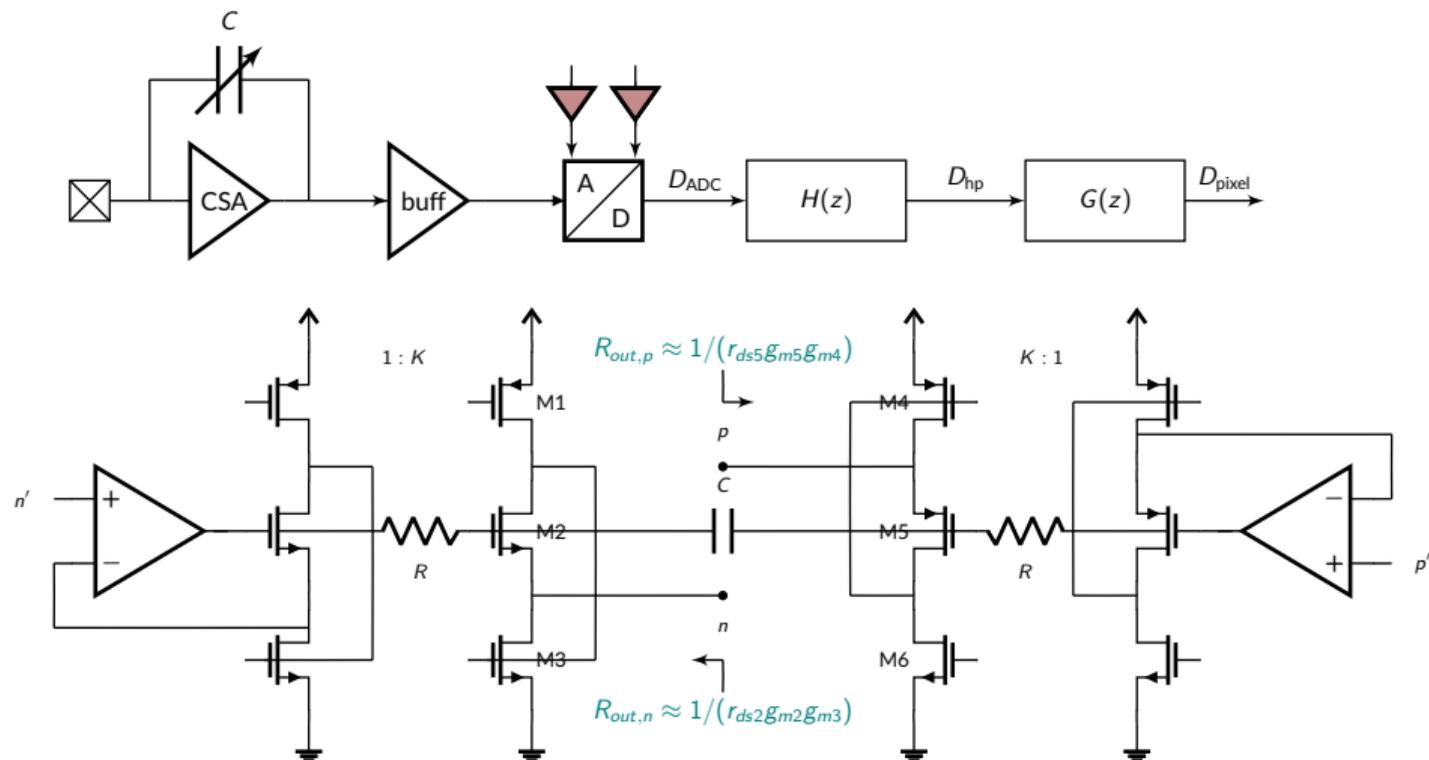
- Tunable gain $A_v \propto 1/C$.

Analog configurability

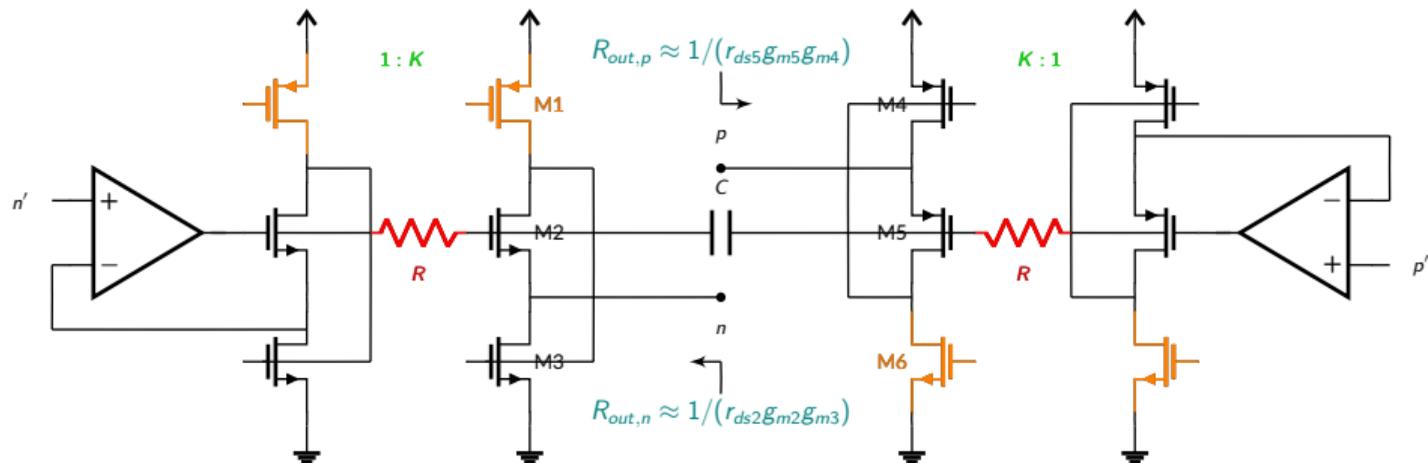


- If $N_{bits} \rightarrow N_{bits} - 1$, $\sum C \rightarrow \sum C/4$ to meet $\sqrt{kT/C}$ noise.
- $\sum C \rightarrow \sum C/2$ is straightforward to achieve. Ongoing research to achieve $\sum C \rightarrow \sum C/4$.

Analog reference buffers

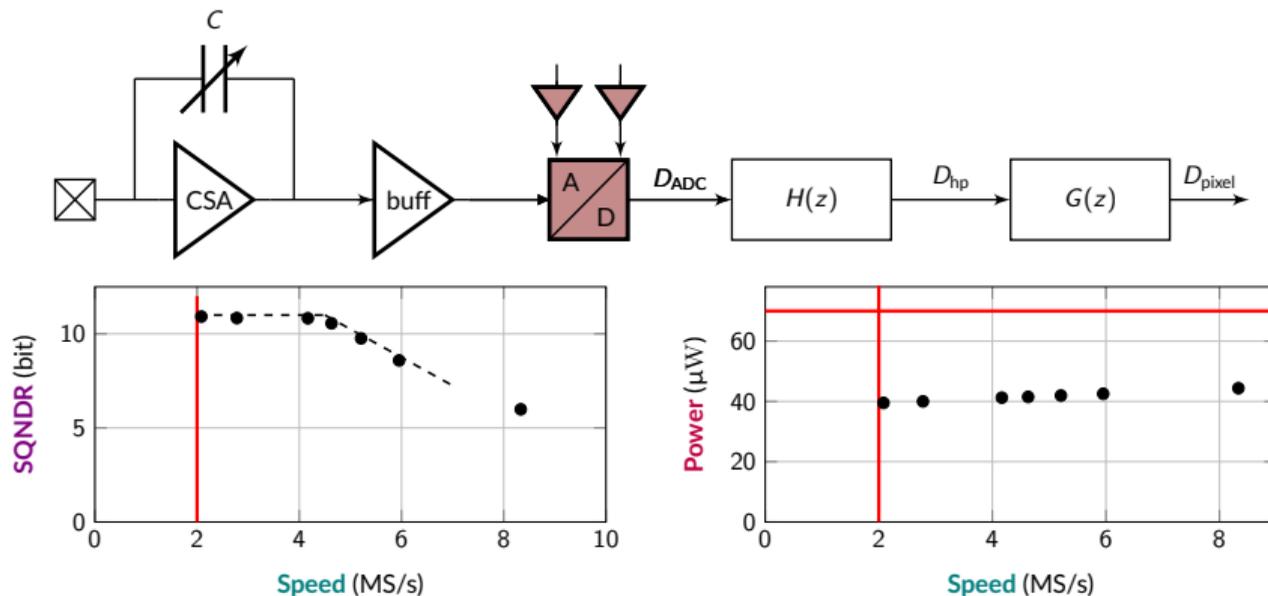


Analog reference buffers



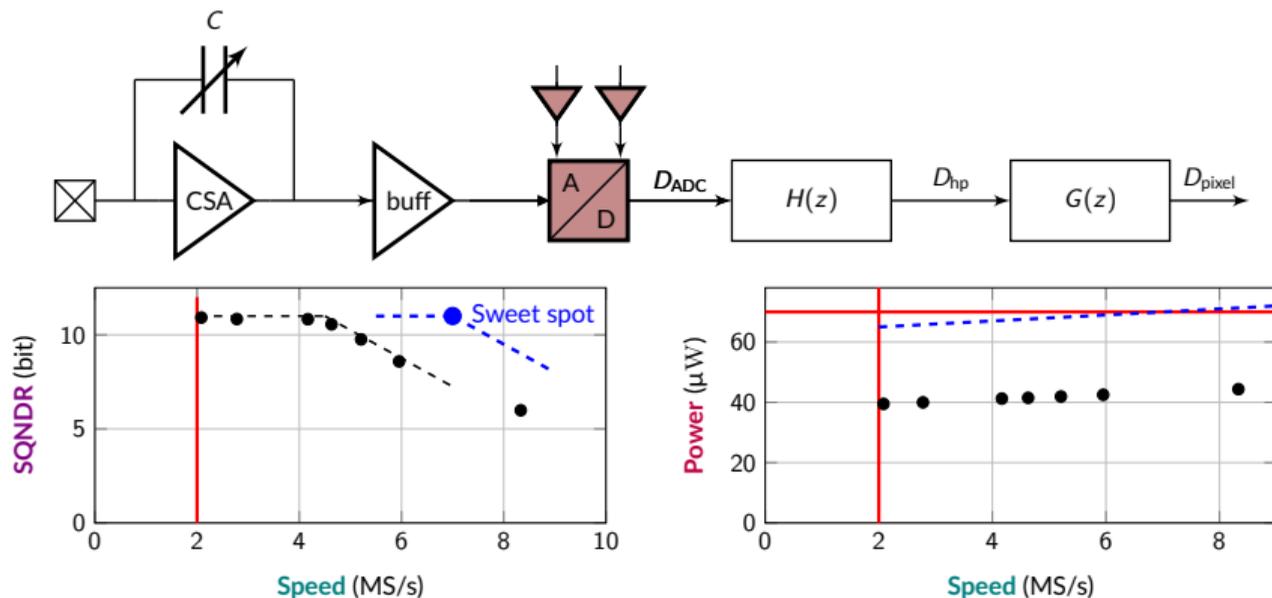
- Tunable current.
- Optimized for low output impedance.
- Low-area strategies: pseudo-resistors, flipped-voltage-follower buffers, small replica branch.

Analog configurability



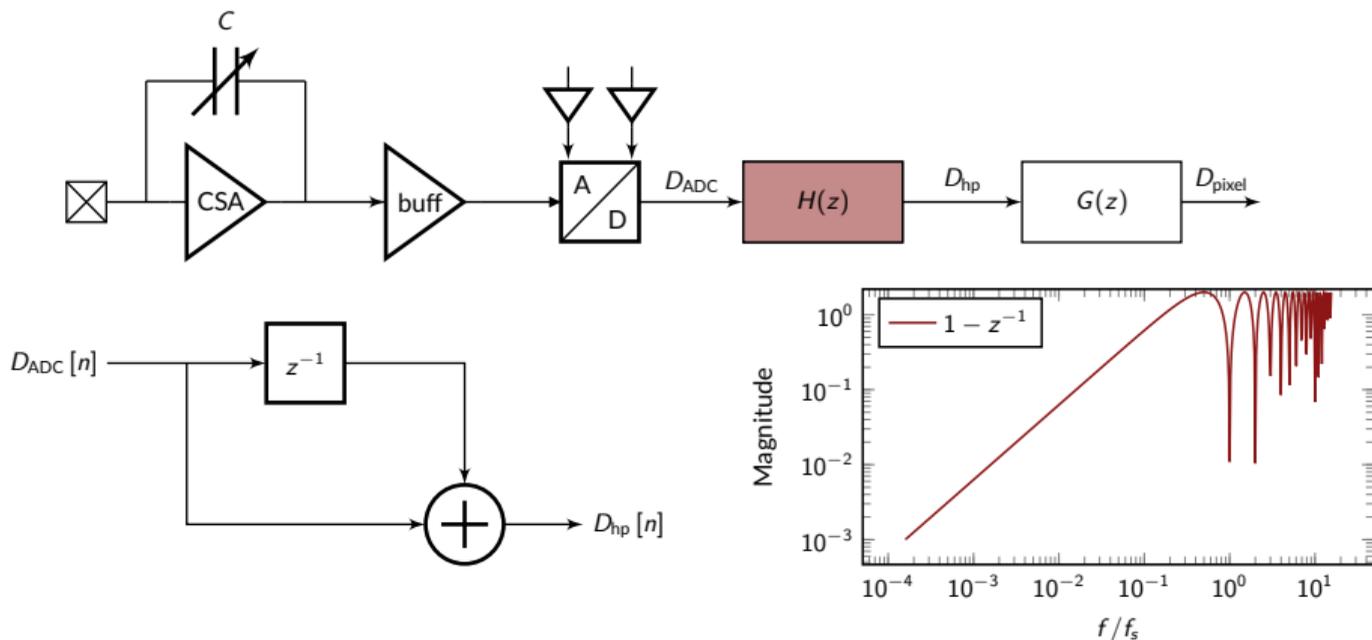
- Speed \nearrow : Power \nearrow , SQNDR \searrow .
- SQNDR \nearrow : Speed \searrow .

Analog configurability



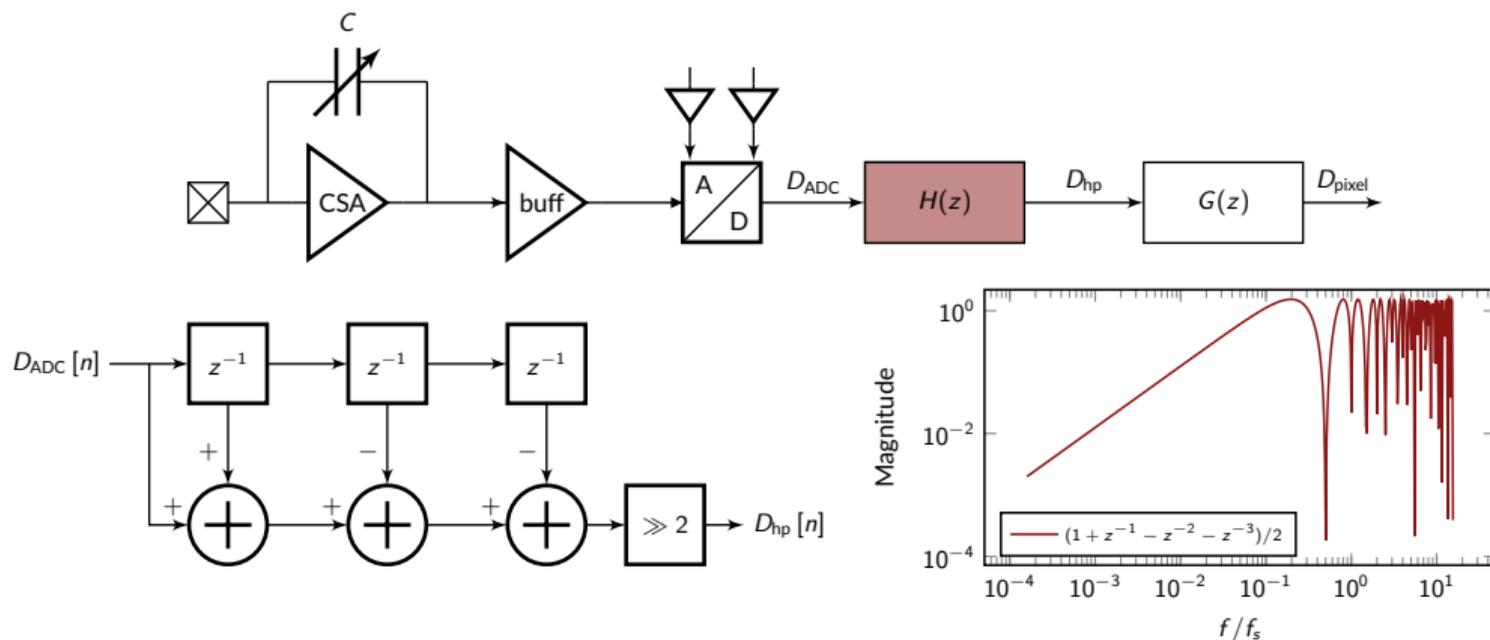
- Speed \nearrow : Power \nearrow , SQNDR \searrow .
- SQNDR \nearrow : Speed \searrow or oversample via Power \nearrow , Speed \nearrow .

Digital configurability



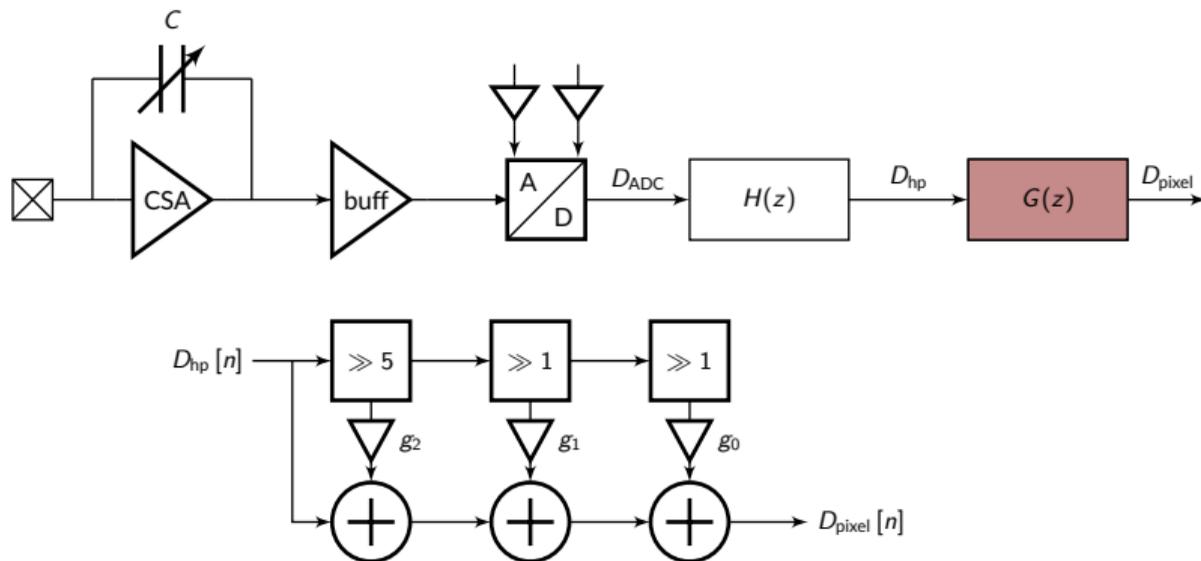
- Perform digital CDS to eliminate offsets and low-freq noise: $\frac{D_{hp}(z)}{D_{ADC}(z)} = 1 - z^{-1}$.
- Targeted pixel ADC: 12-bit, 2 MS/s \rightarrow D_{hp} data is at 1 MHz (Nyquist frequency = 0.5 MHz).

Digital configurability



- Oversampling: tradeoff between frame-rate and noise. $OSR = 4 \rightarrow +1$ bit (white noise).
- Relatively low area: z^{-1} is a 12-bit DFF with ~ 120 gates, a 12-bit adder can be 84 gates.

Digital configurability



- $D_{pixel} = D_{hp} (1 + g_2/32 + g_1/64 + g_0/128)$. This can replace analog gain tuning.
- Shift right (divide by 2^n) is "free".

Next steps

- Finalize the design of a prototype and fabricate in the next months.
- Collaborate closely within Thrust 3: L. Rota, A. Arbabian, B. Murmann, C. Grace, A. Quinn, A. Pena Perez, P.C. Huang, J. Johnson, A. Dragone.
- Codesign with other thrusts (Thrust 2 and Thrust 4 specially).