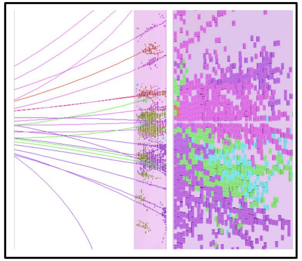
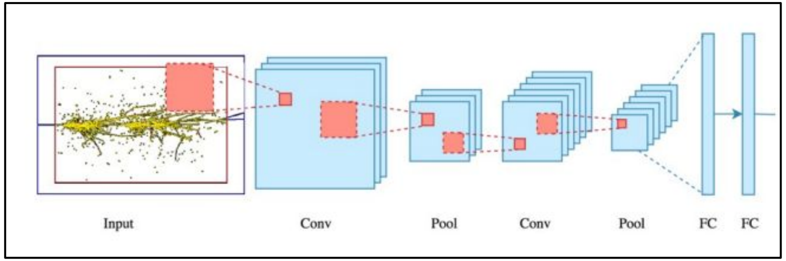
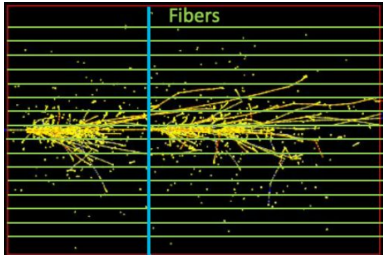
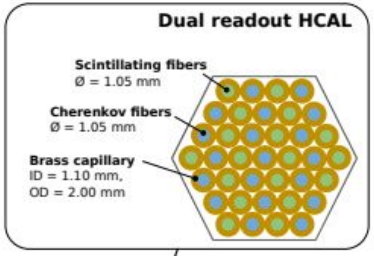






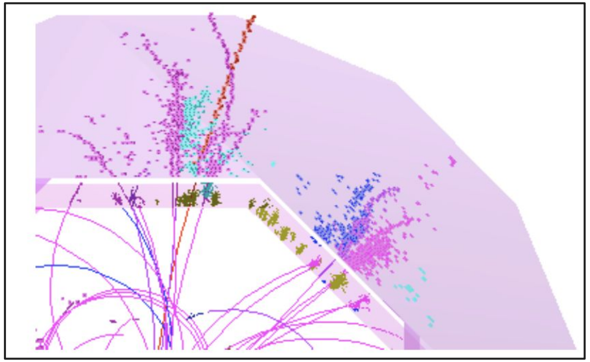


Proposal for Digital SiPM R&D for 5D Calorimetry

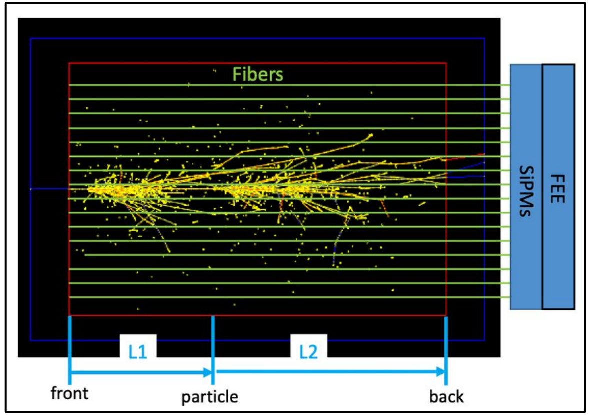
Ariel Schwartzman, **Bojan Markovic**, **Lorenzo Rota**, **Chris Kenney**, Rainer Bartoldus, Su Dong

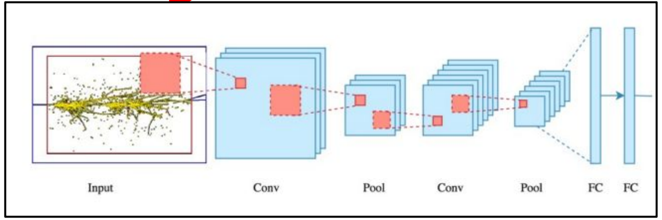
SLAC NATIONAL ACCELERATOR LABORATORY

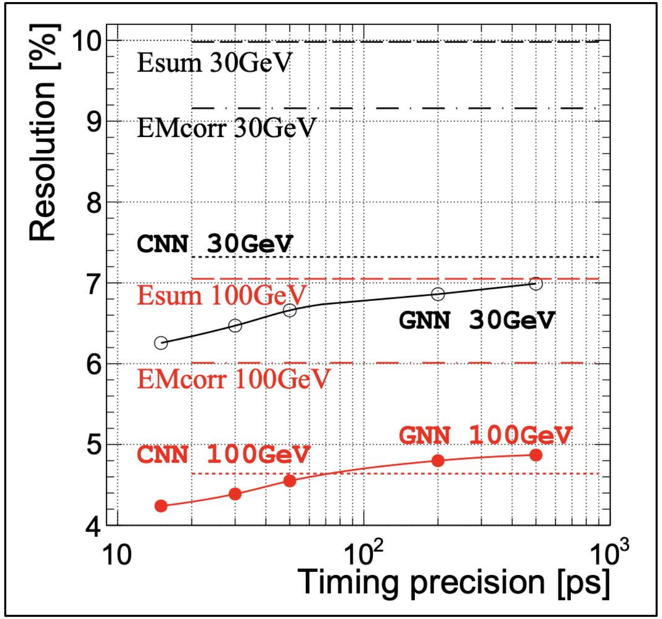
5D Calorimetry



Akchurin, et. al.



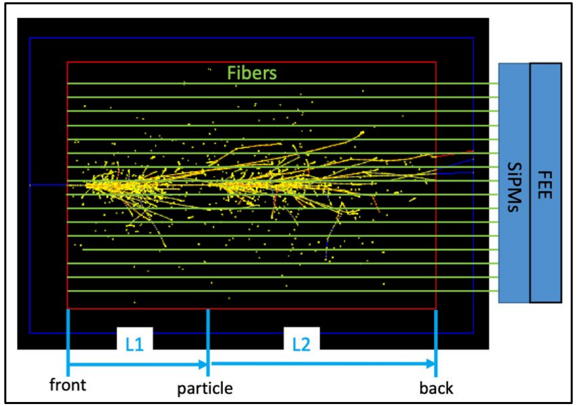


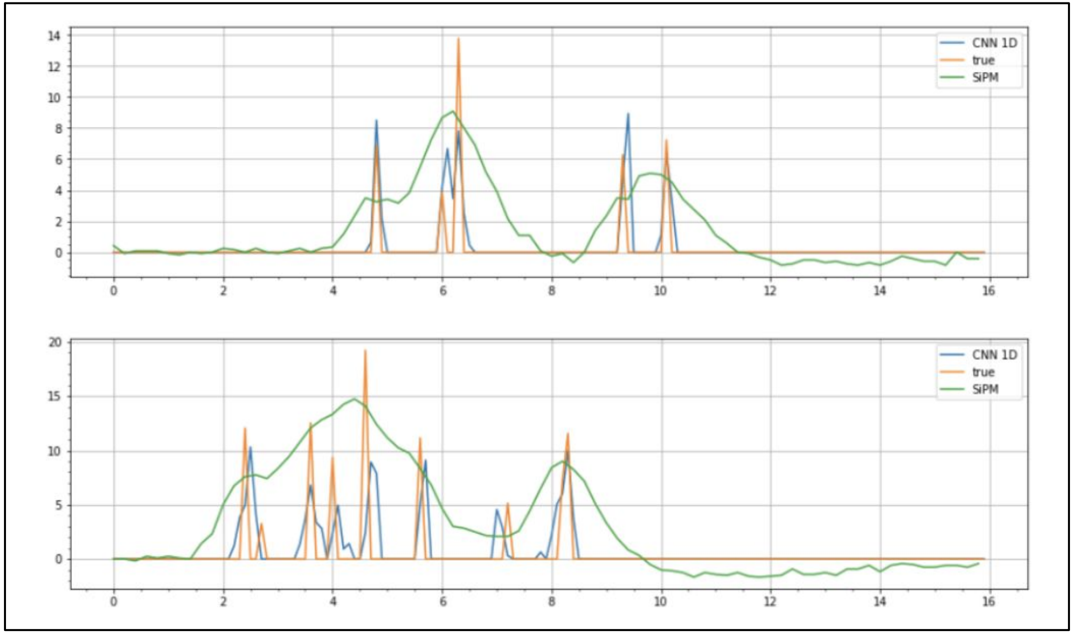


- **Performance of particle flow limited by the ability to accurately associate *tracks* to calorimeter clusters**
  - Challenging when showers overlap in space
- **Exploit the full space-time structure of showers to improve the jet energy resolution (5D PFA)**
- **Example: IDEA fiber dual-readout hadronic calorimeter**
  - 50ps time resolution for ~2cm depth segmentation
  - $t = L_1/c + L_2/(c/n)$, *with n=1.46*
- Timing layers for other calorimeter concepts
- **Fast timing can also provide ToF for LLP**

State of the Art

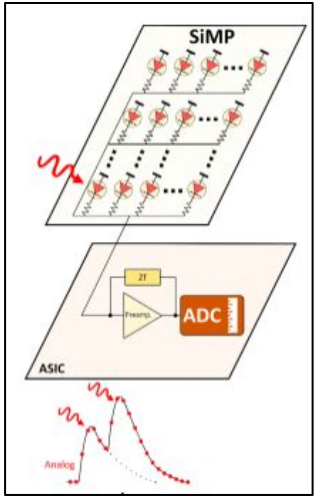
Onsemi SiPM C-series + NALU's AARDVARC V3 10Gb/s digitizer used to simulate waveforms of convoluted pulses.
Pulse shape extracted from HG-DREAM test beam





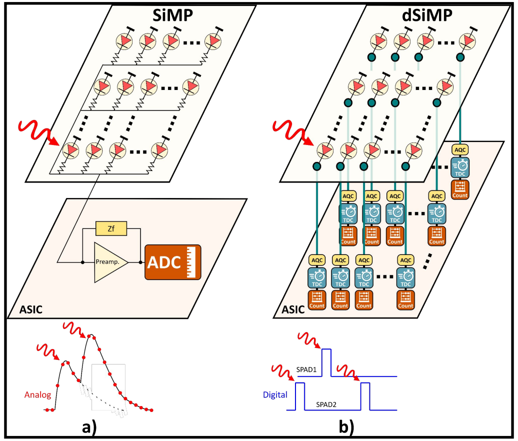
State of the Art Challenges

- Current HG-DREAM prototype is based on conventional (analog) SiPMs and high-speed analog sampling and digitization (ADC conversion) of signal waveforms.
- Signal amplitude (energy) and time of arrival (TOA) extracted from the ADC samples
- **Challenging to scale** to channel sizes necessary for high-granularity calorimeters at future colliders
- High speed ADC sampling is **power hungry**
- Dealing with **large data volumes** is not trivial
- Extracting timing at 10ps precision from analog samples requires **intensive calibration** and **data processing**
- **All these issues become increasingly difficult to deal with as the number of channels increases**



In a conventional SiPMs, thousands of SPAD microcells are placed in parallel, summing all their currents and resulting in a device where output current is an analog waveform with amplitude proportional to the number of avalanche-triggered SPADs.

Next-gen dSiPM with 3D-stacked semiconductor imaging technology



- **Develop a fully-digital approach based on digital SiPM 3D stacked to a dedicated front-end ASIC incorporating high-precision TDCs for ~10ps time-tagging and counters for energy measurements**
- Unlike conventional SiPMs, in the dSiPM every SPAD microcell provides a separate output that can be treated by digital circuits: the signal amplitude is recovered by counting the number of triggered cells while the timing information is extracted from digital pulses employing high-precision TDCs.
- **Operating every SiPM microcell digitally and in-parallel offers many advantages:**

- **lower power consumption** as power hungry analog front-end and high-speed ADCs are avoided
- **lower data rates** as amplitude and time information are directly extracted in presence of the signal
- separate access to every microcell allows the use of the **fine spatial (tens of μm) information** as well as disabling of "hot" cells that exhibit elevated dark cout rates, **improving noise performance**
- the all-digital system is robust and requires **minimal calibration**, making it **easily scale from a prototype to large systems**, *a step often not trivial for high-precision analog systems*

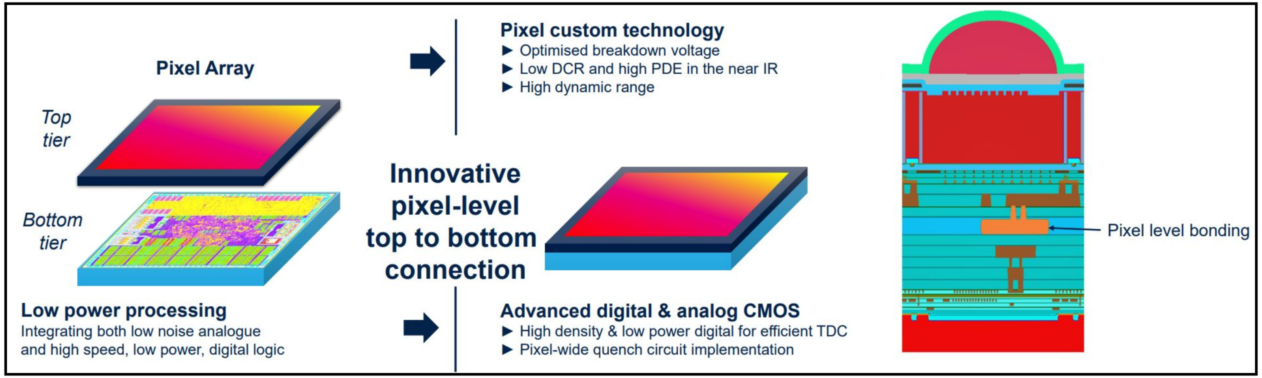
3D Stacking Technology

3D stacking at semiconductor foundries has become a well-established technology

We have identified a technology from ST Microelectronics that promises unprecedented performance in terms of PDE, pixel pitch (and thus dynamic range), and readout capabilities

This technology features a dedicated **top-tier pixel array of SPADs with a 10 µm pitch and near-100% fill-factor, connected via ultra-fine-pitch to a 40 nm CMOS die, where the readout electronics can be implemented**

What sets this technology apart is its feasibility for **fabricating small prototypes at a cost compatible with this proposal**



Readout ASIC

As part of this proposal we will design and fabricate a dSiPM readout-timing ASIC in the 40nm CMOS process from STMicroelectronics

The ASIC will incorporate:

- Active quenching circuit (AQC) for SPAD readout and quenching
- ~10ps Time-to-Digital Converter (TDC) for time-of-arrival (TOA) measurements
- Counters for signal amplitude (energy) measurements
- Readout and configuration logic

The SLAC team has significant experience in designing high-precision timing detector ASICs as well as design of SPAD-based circuitry