Design of Cryo-CMOS Circuits

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June 26th, 2025

My Odyssey into Quantum Computing

- PhD in EE – UT-Dallas (2014)
- 20+ years in semiconductor industry
- Experience with wireless connectivity, cellular chipsets & image sensing ICs
- Work experience at TI, Nvidia (Icera), Senseeker Engineering Inc., Cypress Semi
- Joined a Quantum Computing Startup Equal1 Labs in 2019
- Enrolled in Masters In Quantum Technology program at SJSU

Part I: Silicon Spin Qubit Architecture

- Quantum Computing Full Stack
- Thermodynamics: Heat loads
- Quantum and Control & Readout Plane
- Quantum Dots, Spin Manipulation & Readout

What does it take to build a Quantum Computer?

npr.org/

- Apollo11 workforce comprised of over 400,000 engineers of the following disciplines:
- Aerospace
- Electrical
- Mechanical
- Systems
- Software
- Structural
- Propulsion
- Thermal
- Materials
- Environmental

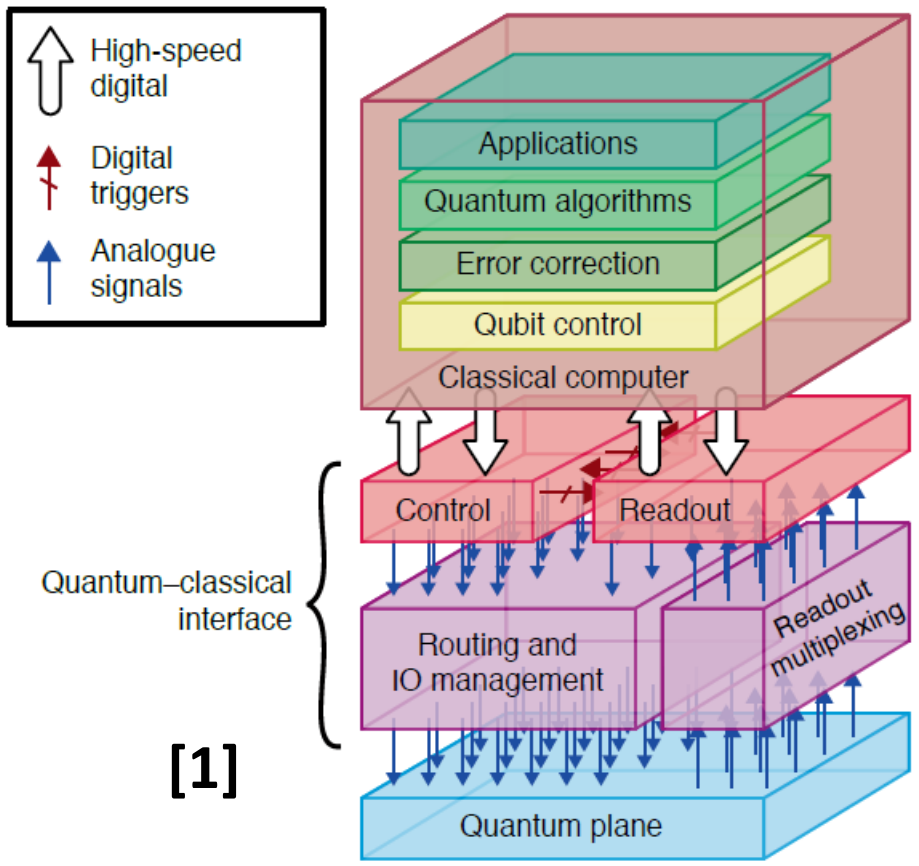
What does it take to build a Quantum Computer?

• Mechanical	Cryocooler, compressor, chiller, vacuum pump, pipes, Helium
• Systems/Hardware	Instrumentation, cable plant, cryogenic sensors, amplifiers
• Software	Automation, calibration, computation
• Physicist	Qubit Substrate

….and more recently…

• Electrical (IC)	Cryogenic Controller IC

Quantum Computer Stack



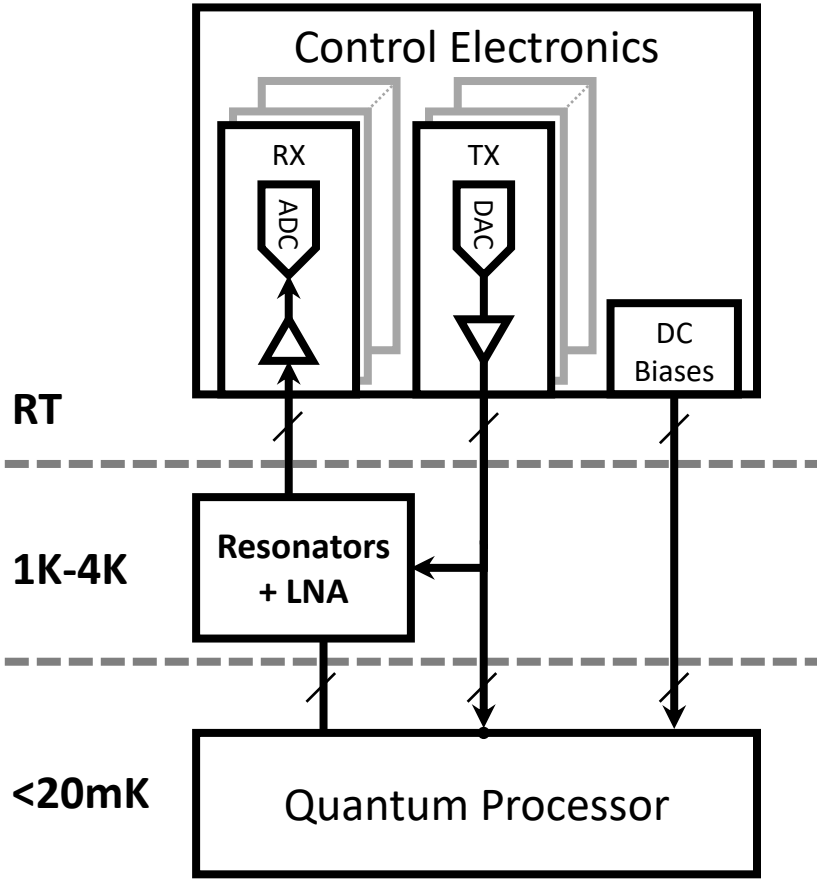
[1]

Innovations & Trends

- Quantum + AI, Error Correction & Encoding, State Classifiers, Efficient Transpilers
- Low power & high fidelity qubit drive and read out architecture
- High density multiplexing at mK, 2.5D / 3D packaging
- Superconductor, semiconductor, photonics, trapped ions

Quantum Control and Readout at RT

- Main Electrical Components of a Quantum Computer
  - Quantum Processor where qubits are located
  - Classical Controller:
    - Driving circuits: Generate waveforms to induce quantum operations
    - Read out circuits: read the state of qubit using SET, RF reflectometry (drain or gate)
  - Other: Couplers, amplifiers, attenuators, circulators, resonators
- Is this the best architecture to support 1M qubits? What are the limits?



A Little Detour into Thermodynamics

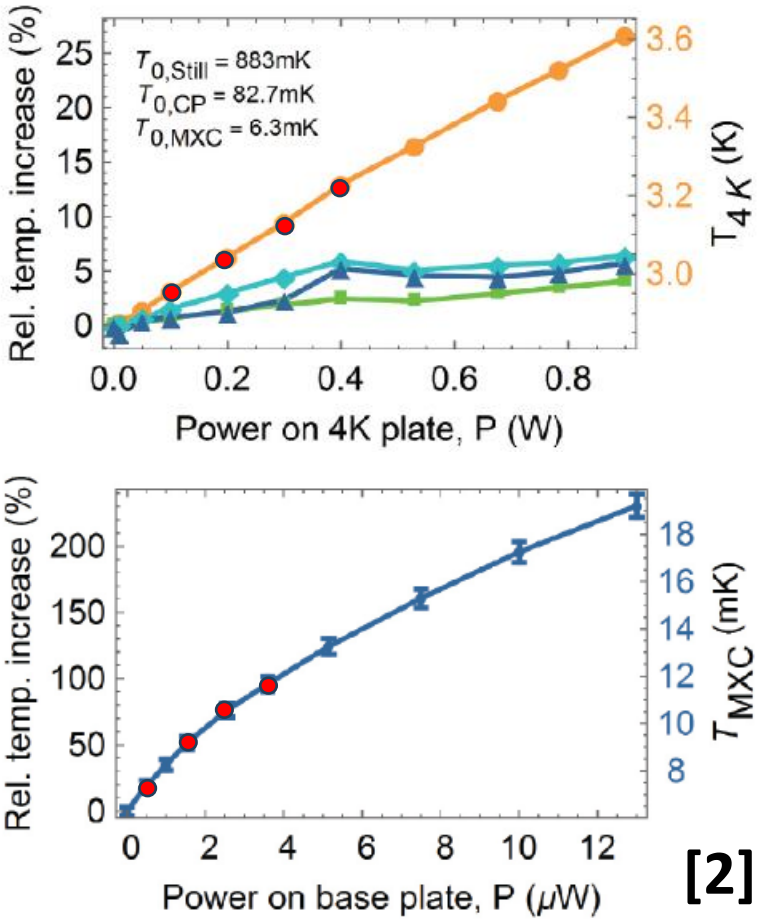
- Passive Heat Loads

$$\Delta P_i = \frac{\partial P_i}{\partial T_i} \Delta T_i$$

- Active Heat Loads

$$P = I^2 R$$

- Radiative Loads
  - Ignored for lower temperature stages



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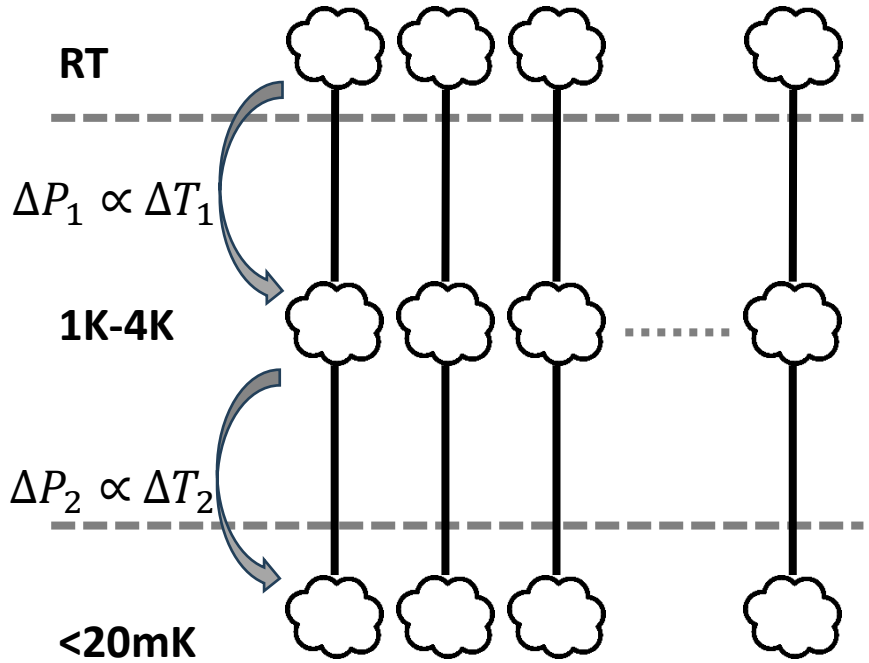
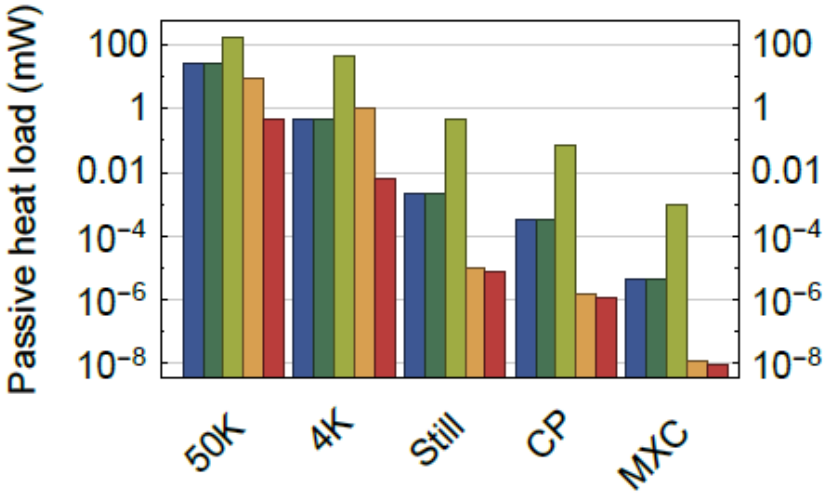


Integration Strategies and Challenges

- Considering passive loads ONLY
  - 20 µW/13nW ~ 1538 cables @ MXC
- *Not enough for 1M qubits*
- *Requires high density cabling*



Preferred for RF Signals

UT85–SS–SS
UT85–NbTi
UT85–SPCW

[2]

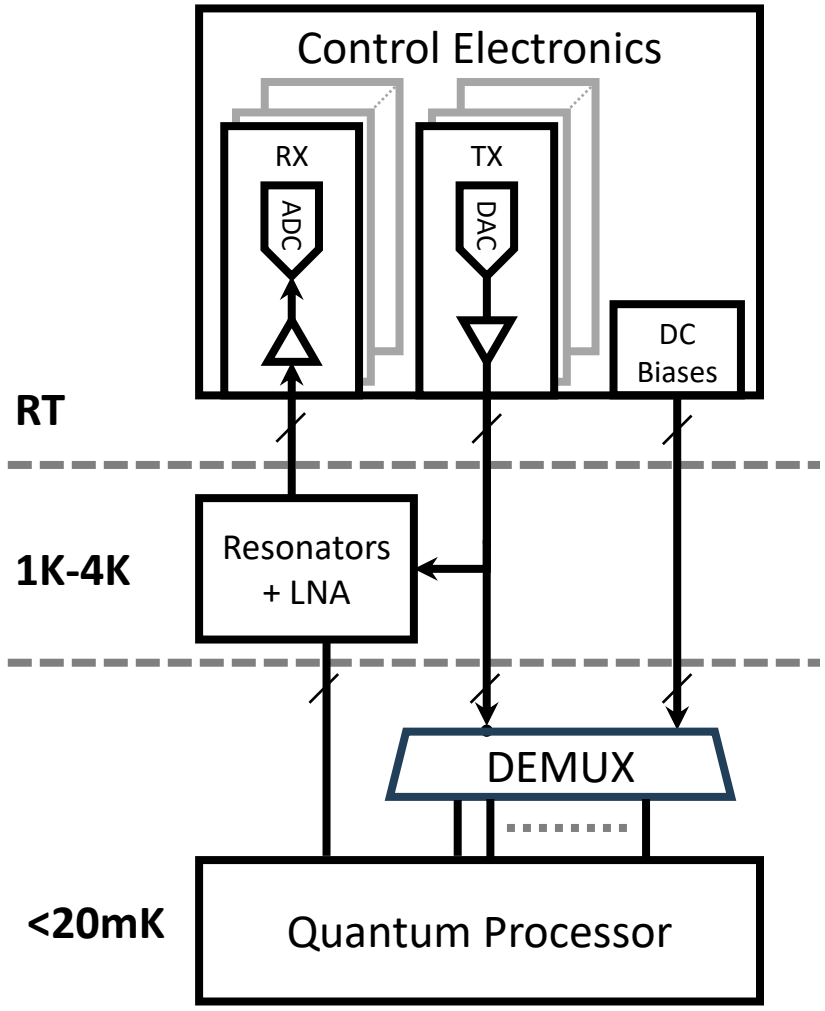
TwP AWG35 Cu–NbTi
TwP AWG36 PhBr–NbTi

Preferred for DC Signals

Stage name	Temperature (K)	Cooling power (W)	Cable length (mm)
50K	35	30 (at 45 K)	200
4K	2.85	1.5 (at 4.2 K)	290
Still	882×10^{-3}	40×10^{-3} (at 1.2 K)	250
CP	82×10^{-3}	200×10^{-6} (at 140 mK)	170
MXC	6×10^{-3}	19×10^{-6} (at 20 mK)	140

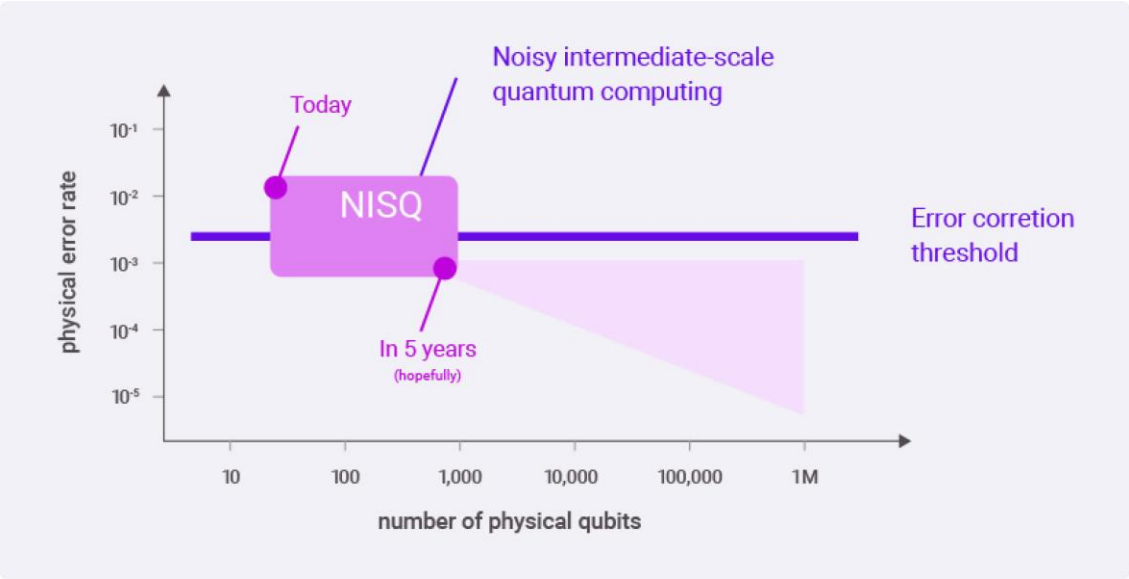
Scaling of Quantum Processors with Demux

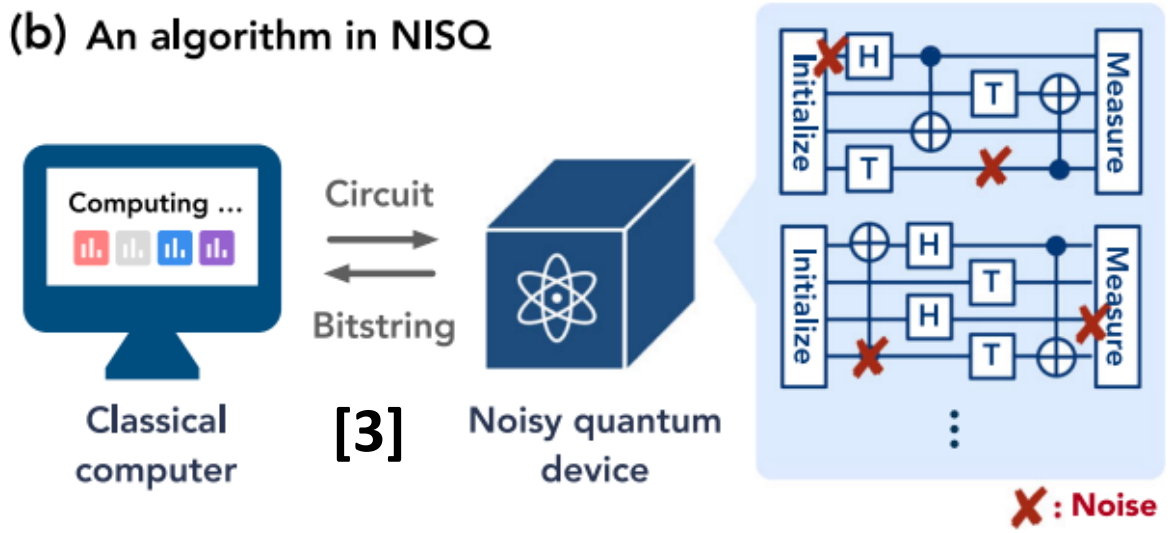
- Reduces cabling bottleneck above MXC stage (20mK)
- Efficient scaling of connections from the quantum substrate to control and readout plane
- Maintains thermal load with increasing qubit count in the Quantum Processor



From NISQ to FTQC

- NISQ era is defined by quantum systems with fewer and noisier qubits.
- Entering the FTQC era requires
  - Building error correction as part of the system
  - Low latency between Control & Readout and QPU (100's of ns)





q-ctrl.com, Adapted from Rigetti

How to design the quantum-classical interface in the FTQC era with low latency?

From NISQ to FTQC

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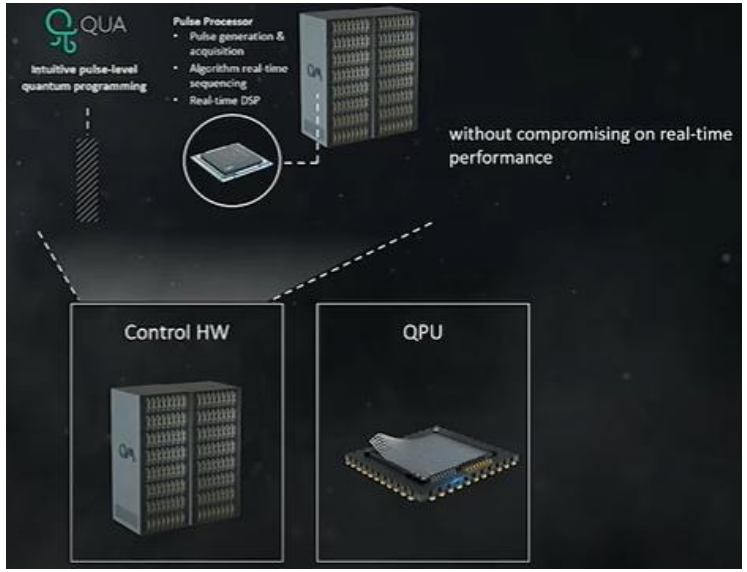

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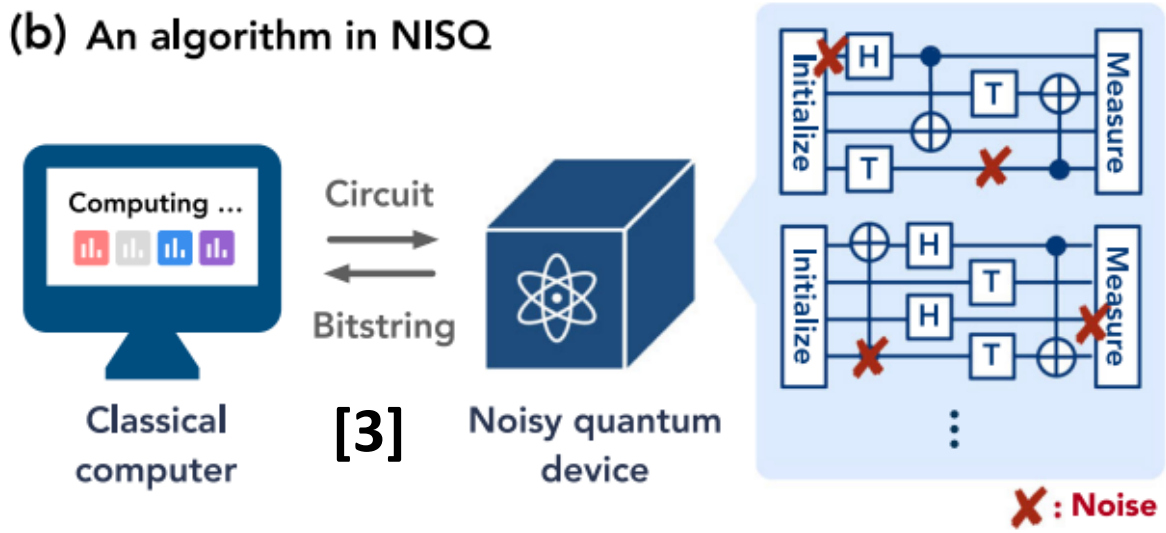

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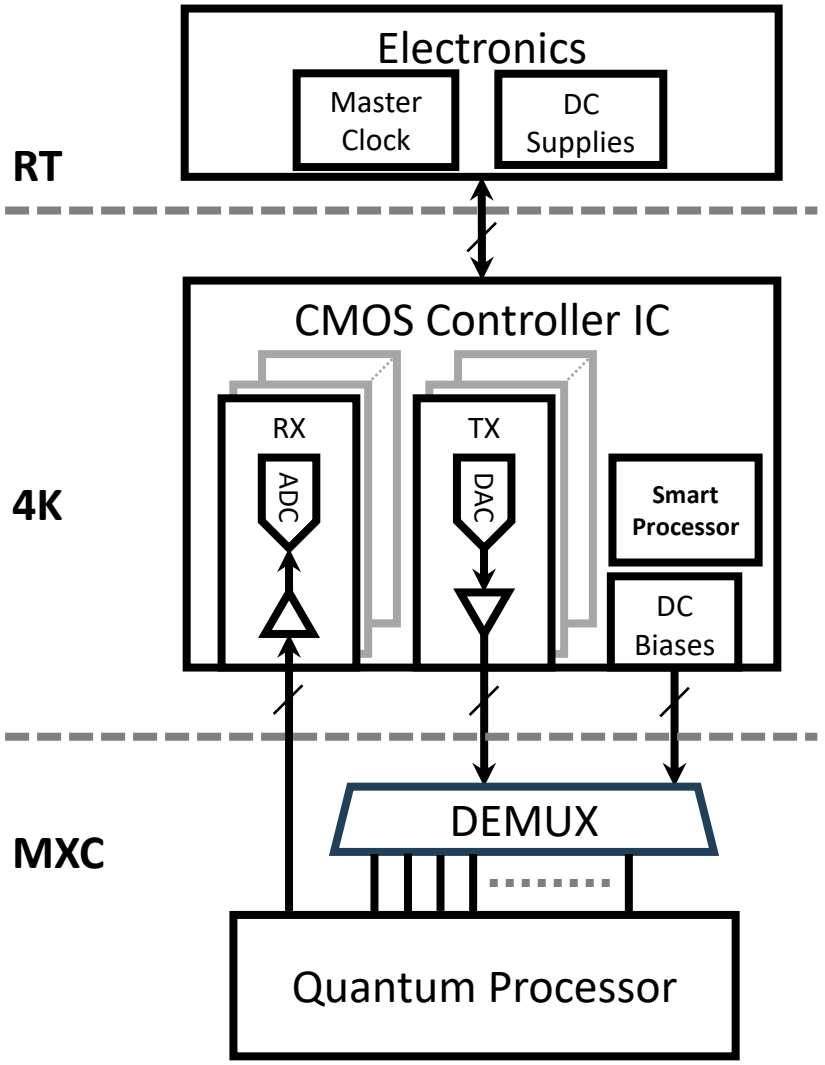
How to design the quantum-classical interface in the FTQC era with low latency?

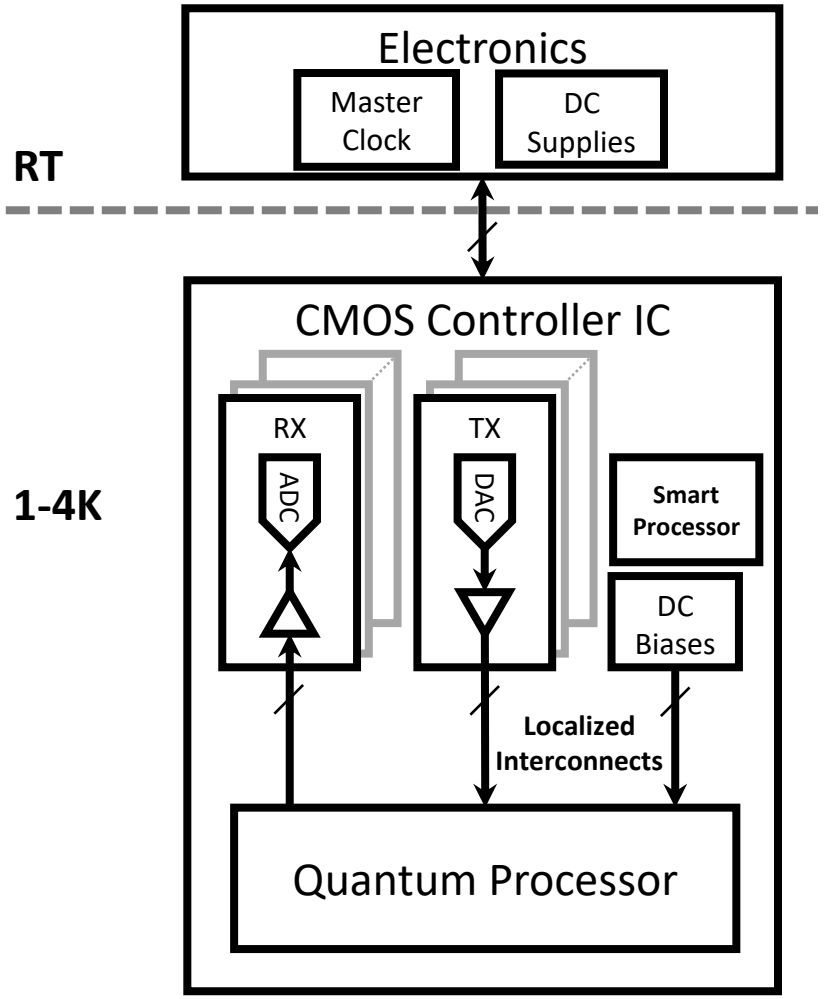
Control and Readout Plane at Cryogenic Temperature

- Move main functions of signal generation / detection to/from the quantum processor to 4K. Only a few clock & bias channels needed from RT electronics.
- Pros:
  - Simplified cable plant from RT to 4K
  - Seamless quantum control operation
  - Qubit substrate is located at MXC to achieve optimum quantum metrics in best technology option
  - Cryogenic controller is located at 4K → reasonable high cooling power → more TX/RX channels designed in commercial CMOS. Risk of carrier freeze out mitigated.



Monolithic Integration of Qubits and Control Electronics

- Qubits and localized control electronics on the same die
- Pros:
  - IO bottleneck addressed with dense localized routing in process
  - Seamless control of electronics for qubit operations
  - Low parasitics → large signal bandwidths
- Challenges:
  - Qubit substrate designed in commercial CMOS technology
  - ‘Hot Qubits’
  - Heating effects (Mathieu de Kruijf arXiv:2310.11383)

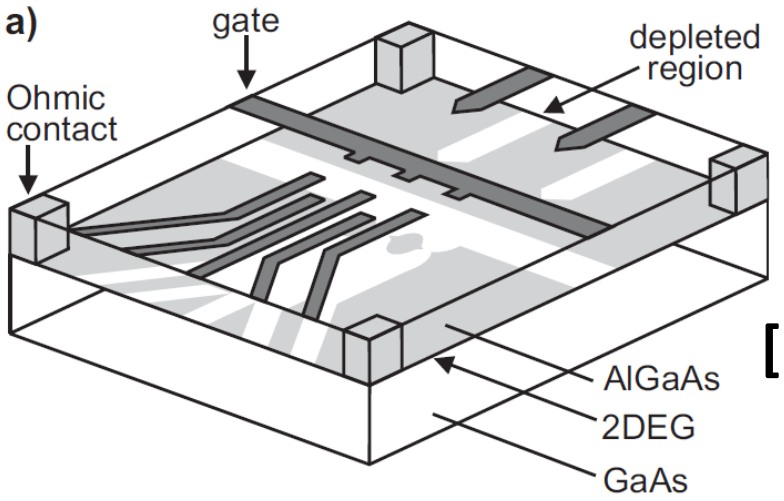


Spin Qubits

- What is it?
  - A quantum mechanical system located in a semiconductor host material in which the spin dipole of an elementary particle such as an electron or hole can be used to encode information.
- What is the process?
  - The electrons or holes are extracted from a reservoir and into a quantum dot
  - The spin dipole is initialized with an external DC magnetic field
  - The spin is manipulated using a localized AC magnetic field
  - The readout is done through a charge sensor or SET device
- *Trivia: What is spin? (Food for thought during lunch break)*

Quantum Dots (Particle in a Box)

An elementary treatment of Quantum Dot reveals discrete energy levels and the criterion for charge confinement.



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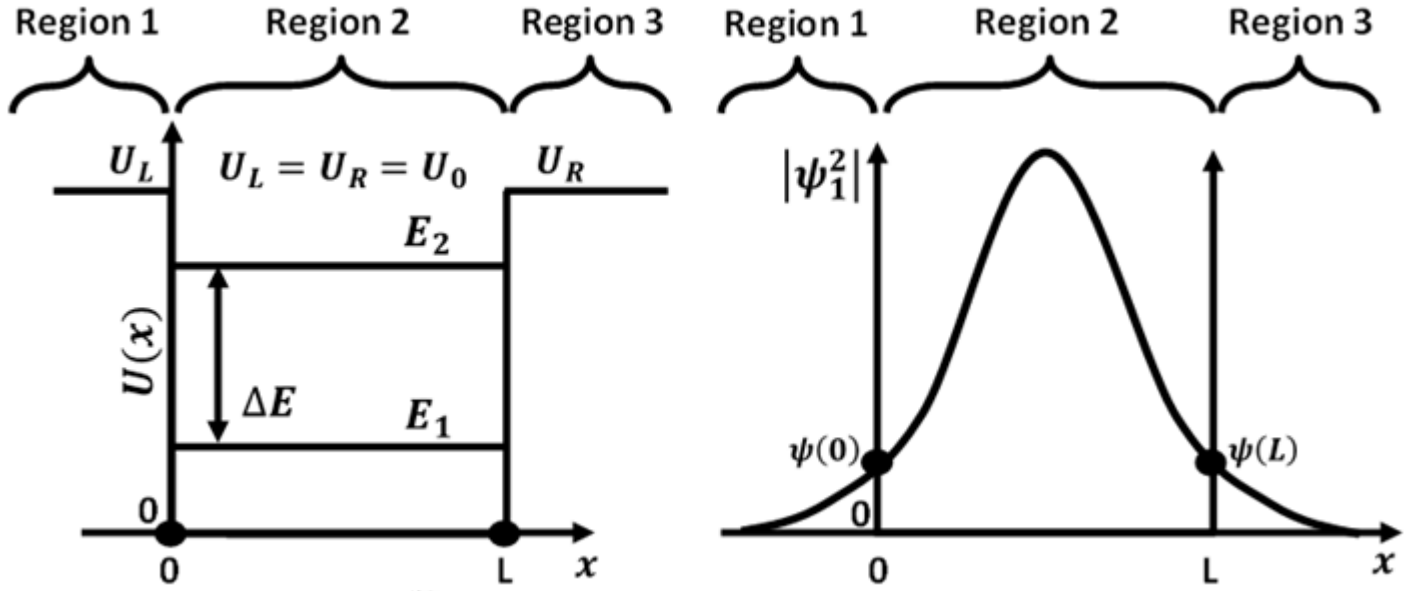


Solve 1-D Time Independent Schrodinger Eqn. over x

$$-\frac{\hbar^2}{2m^*}\frac{d^2\psi}{dx^2} + U(x)\psi(x) = E\psi(x)$$

$\Rightarrow$

$$E = \frac{p^2}{2m^*} \approx \frac{1}{2}k_bT$$

$$\lambda_g = \sqrt{\frac{4\pi^2\hbar^2}{m^*k_bT}}$$

$U(x)$ = Potential Energy

$\psi(x)$ = Wave Function

E = System Energy

Conditions for e confinement

$L \leq \lambda_g$ (De Broglie)

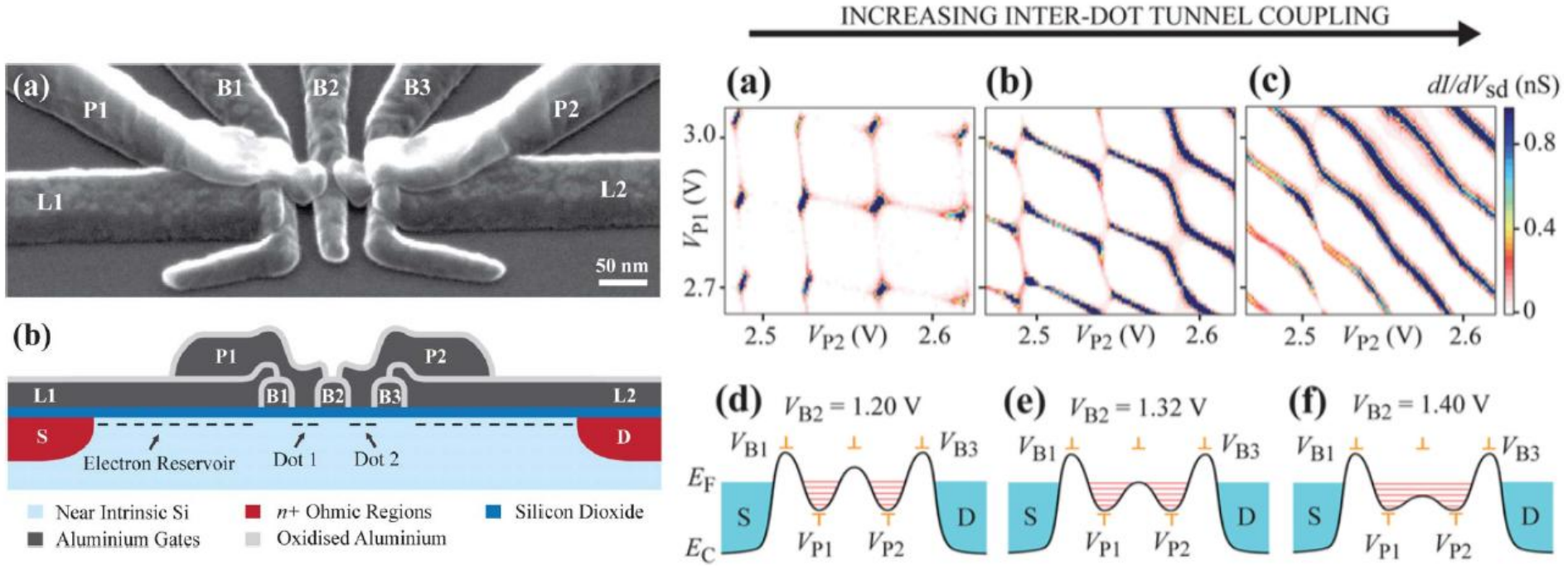
$T = 4K, m^* = 0.19m_e$

$L \leq 410nm$

equal1

Quantum Dots: Si MOS

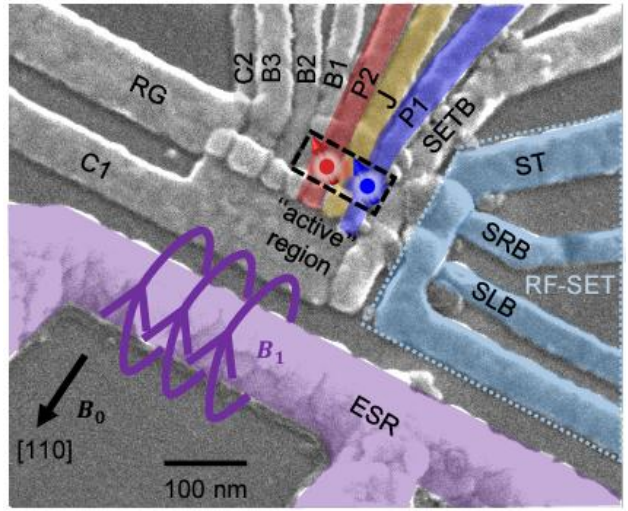
- Barriers & plungers control the potential energy profile in the Si substrate
- Plungers are biased to create a ‘potential well’ or quantum dots
- Barriers are biased to isolate the wells and create interactions between electrons in those wells



[11]

Quantum Dots: Building Blocks

- Bx: barrier control, control e/h tunneling between wells
- Px: plungers, electrostatic control of electron or hole inside the well
- J: exchange interaction between neighboring spins
- ESR line: AC magnetic field to create spin resonance
- ST, SRB, SLB: RF-SET device for performing measurement
- Magnet (not shown)



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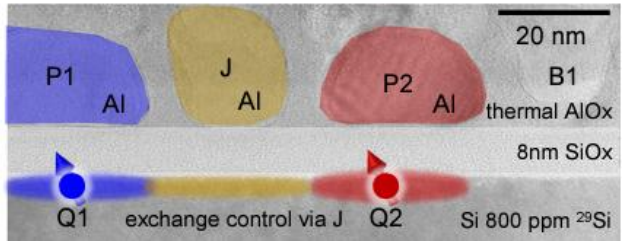
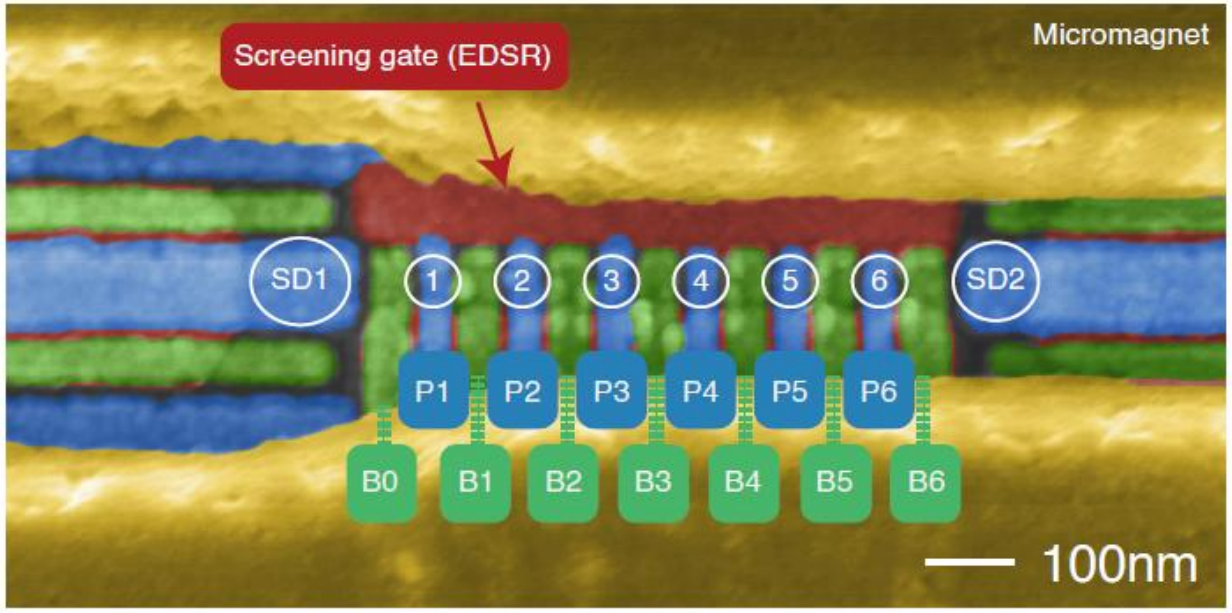


[12]

equal1

Quantum Dots: Si/SiGe

- Quantum Processor substrate is a SiGe/Si Heterostructure
- Carriers are electrons
- The beveled gold colored layer is the micromagnet that creates a magnetic field gradient to control qubit Larmor frequency



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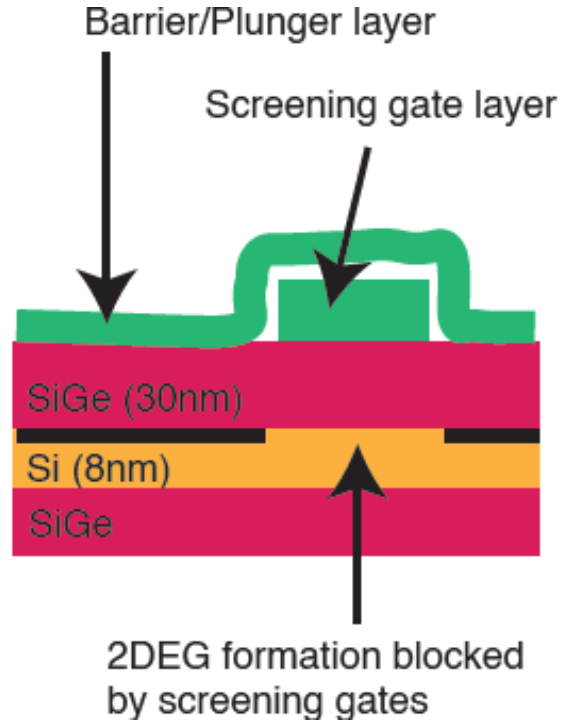
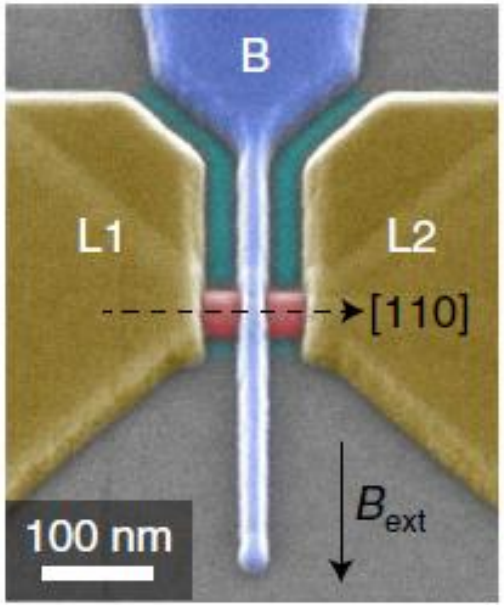


Quantum Dots: Si FinFET

- FinFET like structure in Si (as fin)
- Barrier gate ‘B’ wraps around Si fin
- Plunger gates ‘P1’ and ‘P2’ create wells to trap holes
- Spin is manipulated with EDSR mode
  - Microwave signal applied at the plunger gate to manipulate hole spin



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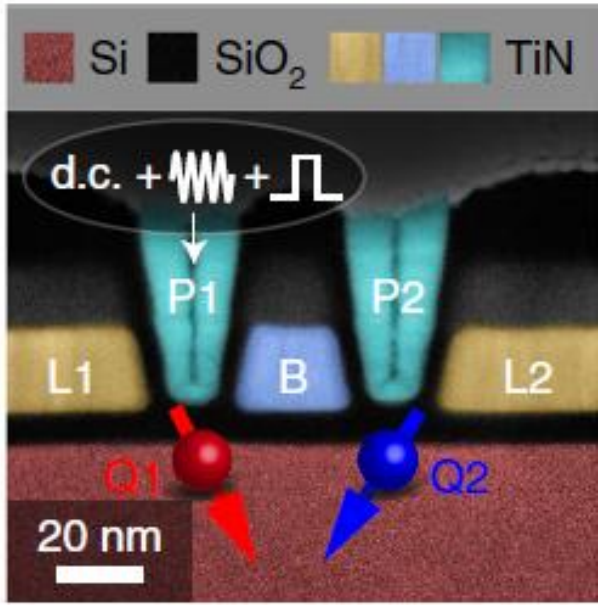
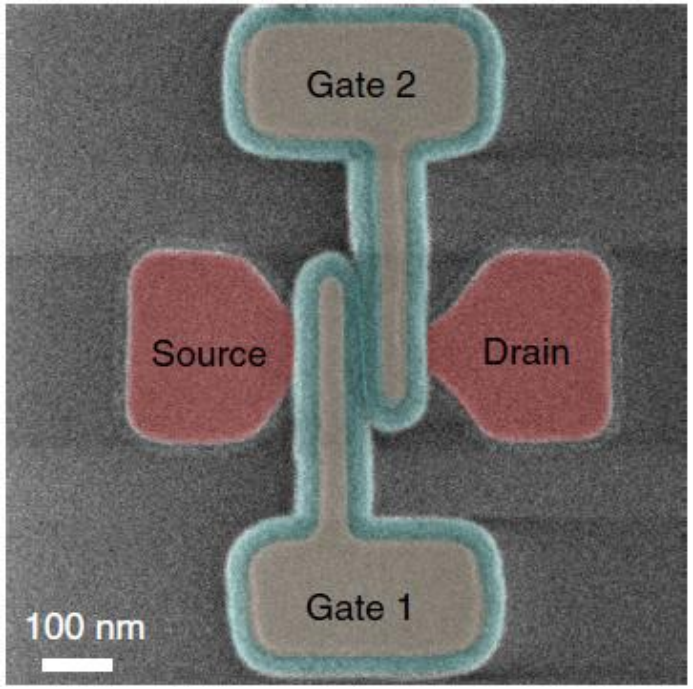
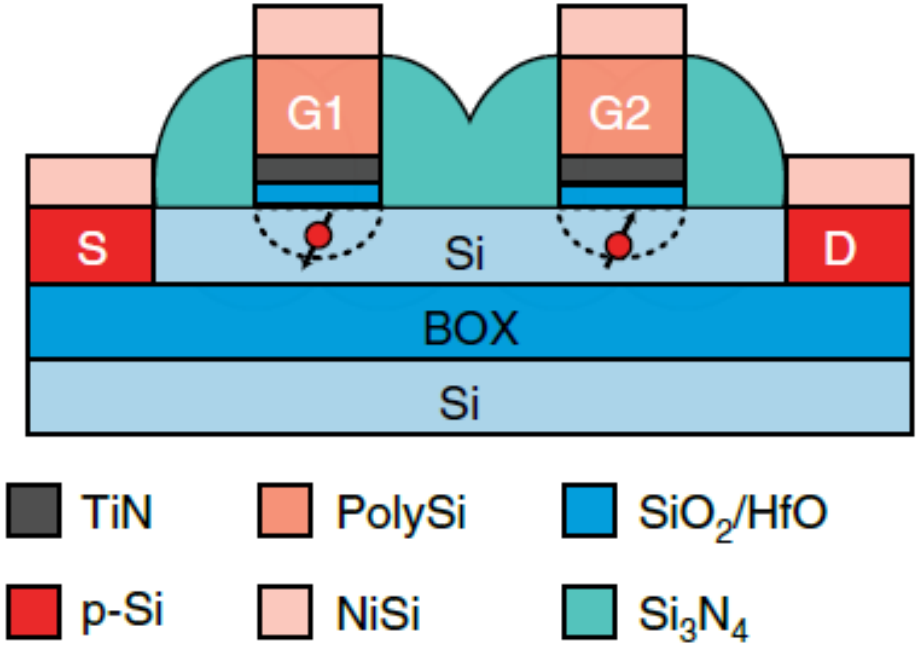


Quantum Dots: Si FD-SOI

- Manufacturing approaching ‘commercial’ FD-SOI foundry process
- Quantum dots formed under gates in thin undoped Si film above BOX
- Challenges in implementing barrier and plunger gates at fine pitch



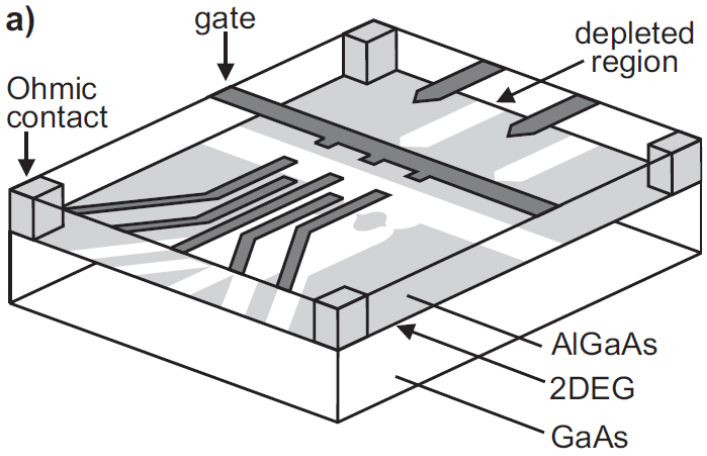


[14]

Engineered Process vs. Foundry Process

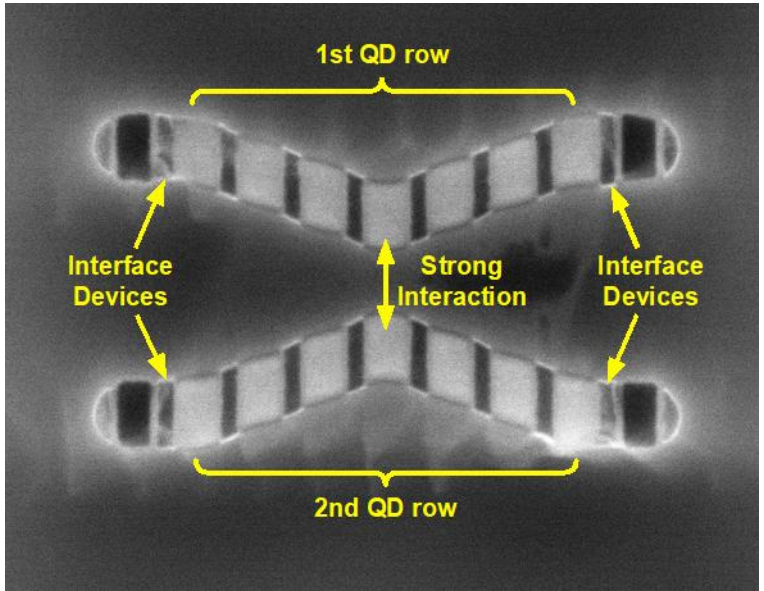
Engineered Process

- CVD or Molecular Beam Epitaxy for crystal growth
- E-Beam based patterning
- Custom recipe & flexible design rules
- Fine pitch between barriers and plungers
- Integrated micro-magnets **[10,5]**



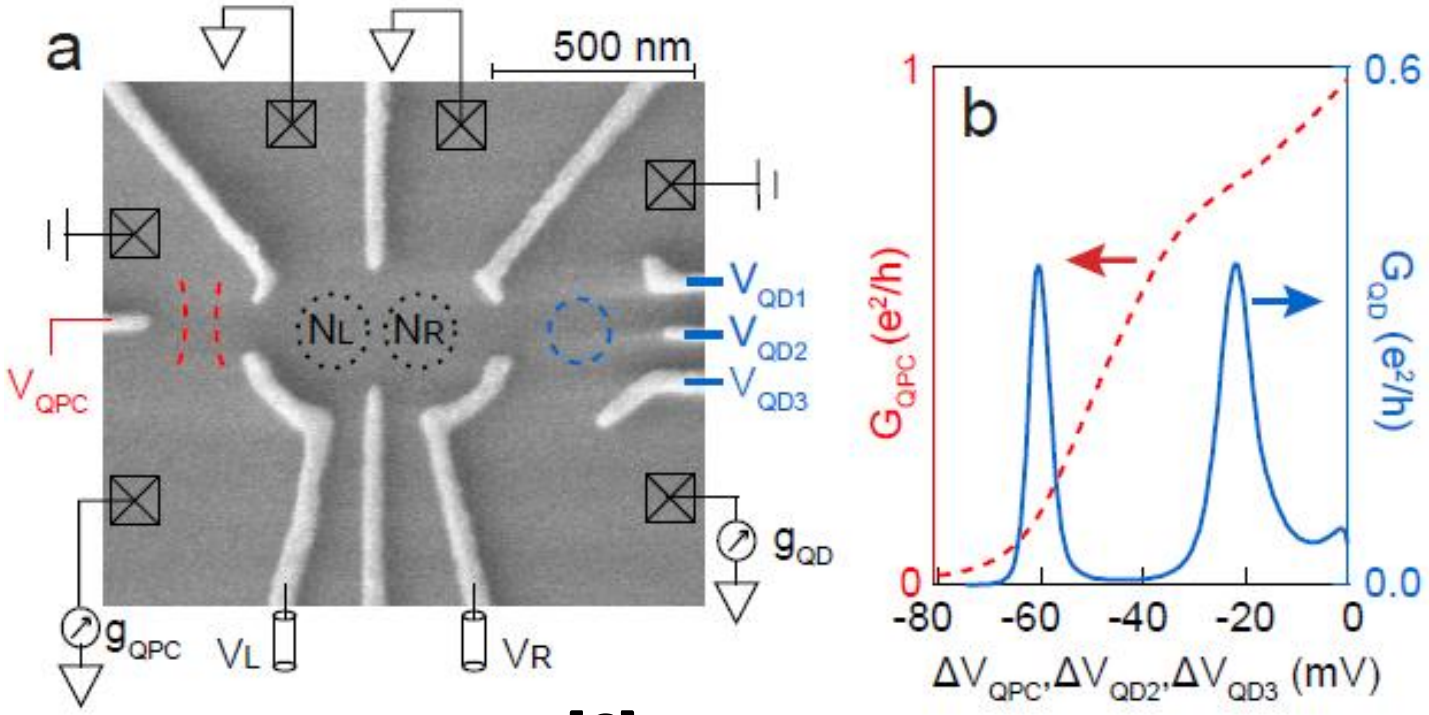
Commercial Foundry Process

- Czochralski (CZ) Method for crystal growth
- Photolithography / EUV
- Fixed recipe & design rules
- Gate pitch defined by process spec
- No integrated micro-magnets **[24]**



Charge Sensors

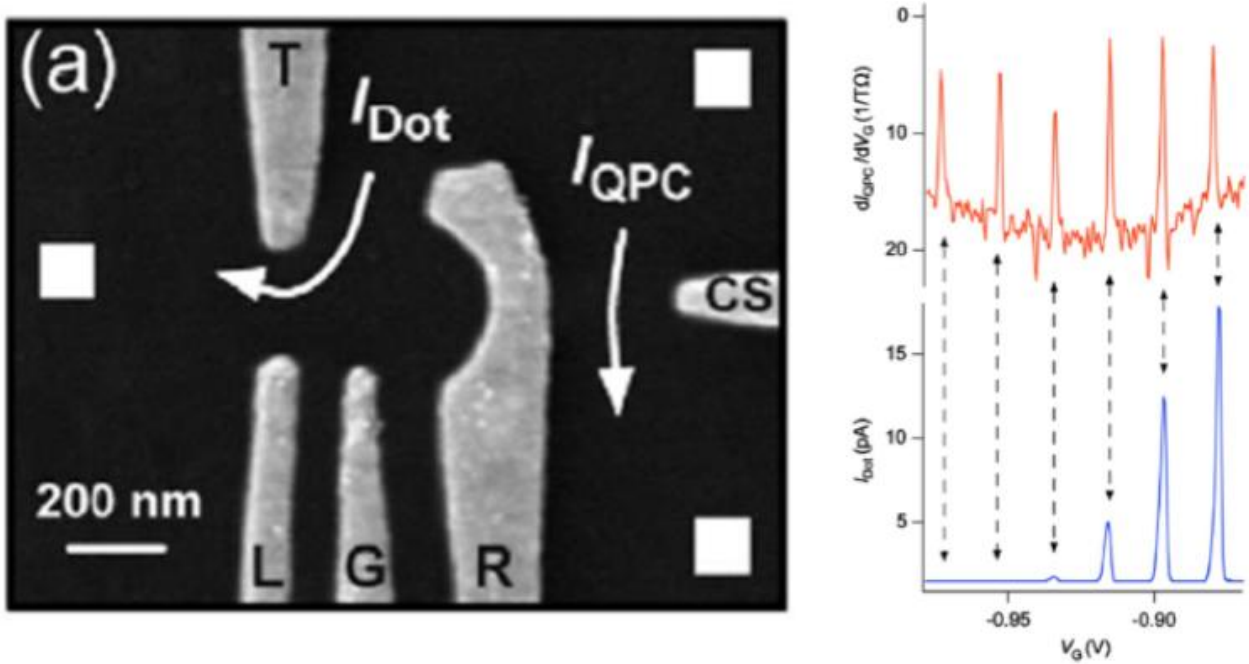
A charge sensor is sensitive to the number of charge carriers in the neighboring quantum dots. The curves in figure ‘b’ shift as a function of occupancy state in quantum dots.



[6]

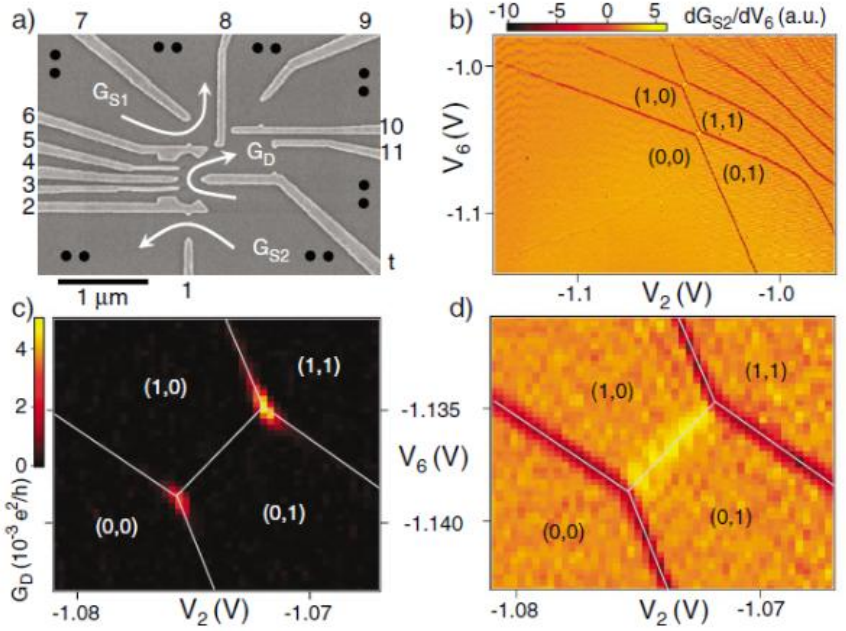
Charge Sensors

A charge sensor shows more features regarding the occupancy state in its transport current compared to a direct current measurement of the quantum dot.



Si Hetrostructure with 1 QD and 1 QPC structure (left); Measurement from QPC sensor (top/red) & QD tunnel current (bottom/blue).

[7]

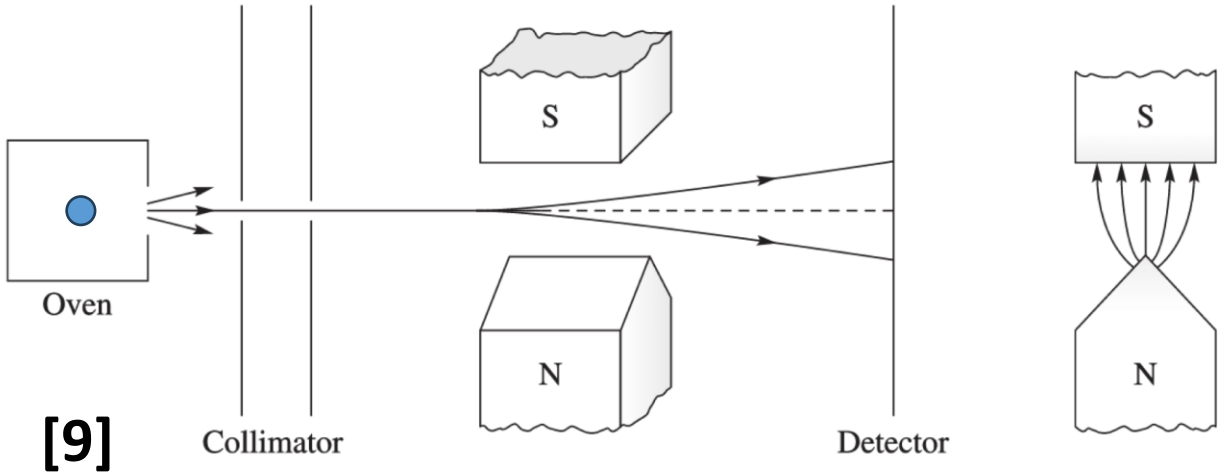


Measurements on DQD with transport current (lower left) and QPC charge sensor (top and bottom right).

[8]

Stern-Gerlach Experiment

- Performed in 1922 by Otto Stern and Walther Gerlach
- Proved quantization of *spin angular momentum $\vec{S}$ and energy $\hat{E}$*



[9]

$$\vec{B} = B_o \vec{z}$$

$$\hat{E} = -\vec{\mu} \cdot \vec{B}$$

$$\vec{\mu} = -g \cdot \frac{e}{2m_e} \vec{S}$$

$$\vec{F} = \nabla(\mu \cdot \overrightarrow{B})$$

$$\vec{S} = \widehat{S_x}\vec{x} + \widehat{S_y}\vec{y} + \widehat{S_z}\vec{z}$$

$$S_z = \frac{\hbar}{2} \cdot \begin{pmatrix} 1 & 0 \\ 0 & -1 \end{pmatrix}$$

$\vec{B}$ *Magnetic Field*
μ Magnetic Moment
g Gyromagnetic ratio
$\vec{F}$ Force causing deflection
$\vec{S}$ Spin angular momentum

Quantum Dot with a DC Magnetic Field

$$\vec{B} = B_o\vec{z}$$

$$\hat{H} = -\vec{\mu}\cdot\vec{B}$$

$$\vec{\mu} = -g\cdot\frac{e}{2m_e}\vec{S}$$

$$\vec{S} = \widehat{S_x}\vec{x} + \widehat{S_y}\vec{y} + \widehat{S_z}\vec{z}$$

$$\hat{H} = \frac{\hbar\omega_o}{2}\cdot\begin{pmatrix}1 & 0\\ 0 & -1\end{pmatrix}$$

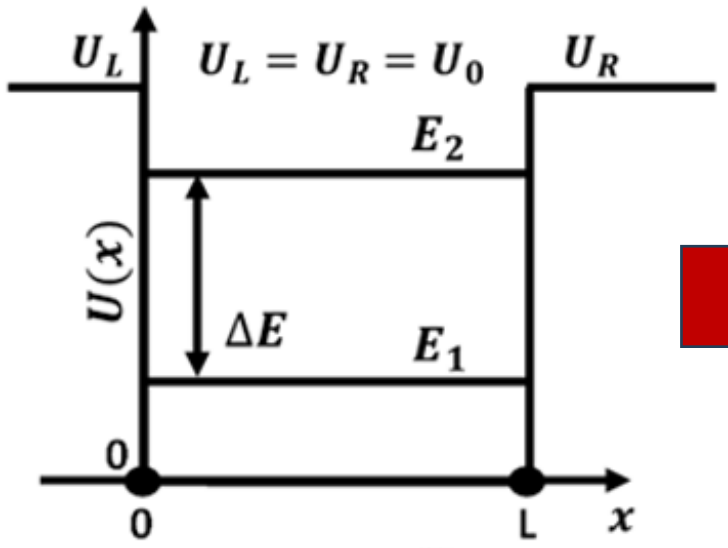
$$\omega_o = \frac{e\cdot B_o}{m_e}$$

$$H|\uparrow\rangle = E_+|\uparrow\rangle$$

$$H|\downarrow\rangle = E_-|\downarrow\rangle$$

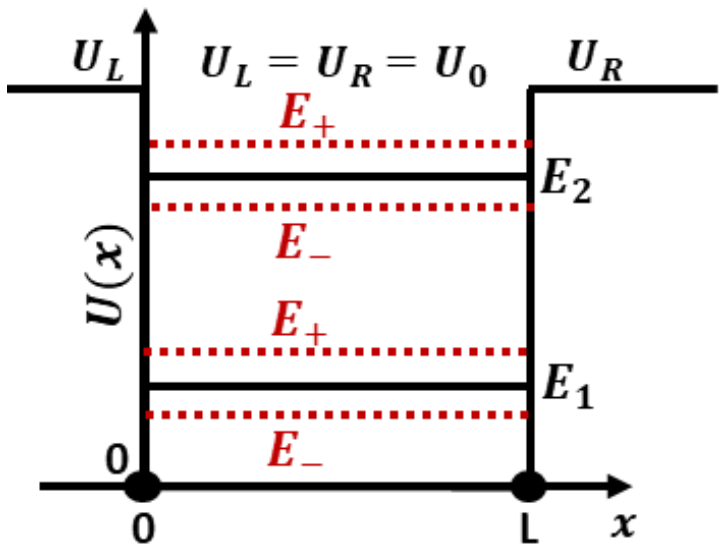
$$E_+ = +\frac{\hbar\omega_o}{2};\ E_- = -\frac{\hbar\omega_o}{2}$$

$\vec{B} = 0$



$$E_n = \frac{n^2\pi^2\hbar^2}{2m^*L^2}, n = 1,2,3,\cdots$$

$\vec{B} = B_o\vec{z}$



Each discrete energy level splits into E_+ & E_- aka Zeeman split

Singlet & Triplet States

- Defined by total spin angular momentum $\vec{S}$ of two electrons/holes in a system

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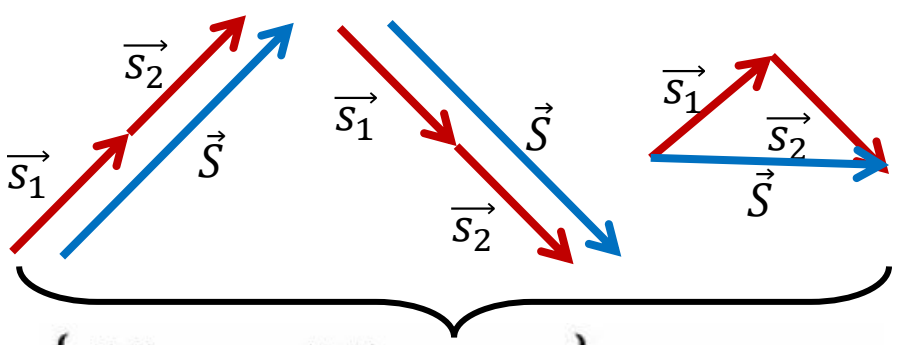
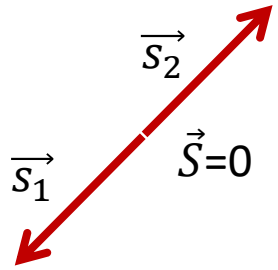
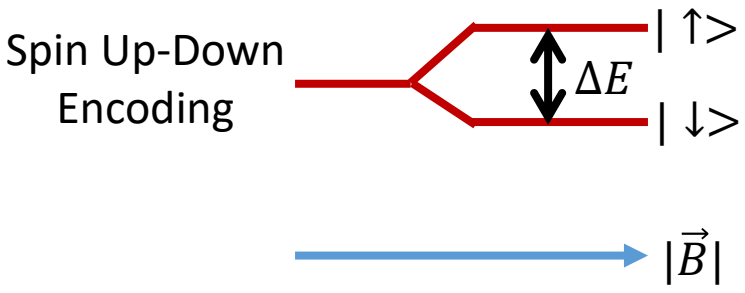


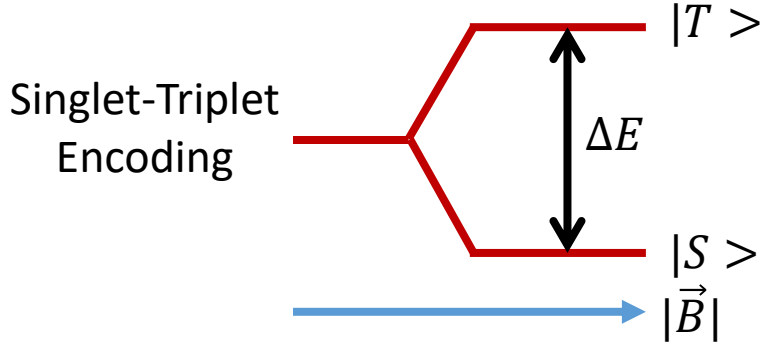
$$\left\{\begin{array}{lcl} |1\,1\rangle & = & |\uparrow\uparrow\rangle \\ |1\,0\rangle & = & \frac{1}{\sqrt{2}}(|\uparrow\downarrow\rangle + |\downarrow\uparrow\rangle) \\ |1\,-1\rangle & = & |\downarrow\downarrow\rangle \end{array}\right\} \quad s = 1 \text{ (triplet)}.$$



$$\left\{|0\,0\rangle = \frac{1}{\sqrt{2}}(|\uparrow\downarrow\rangle - |\downarrow\uparrow\rangle)\right\} \quad s = 0 \text{ (singlet)}.$$

A singlet-triplet state is a superior information encoding scheme for high fidelity readout.

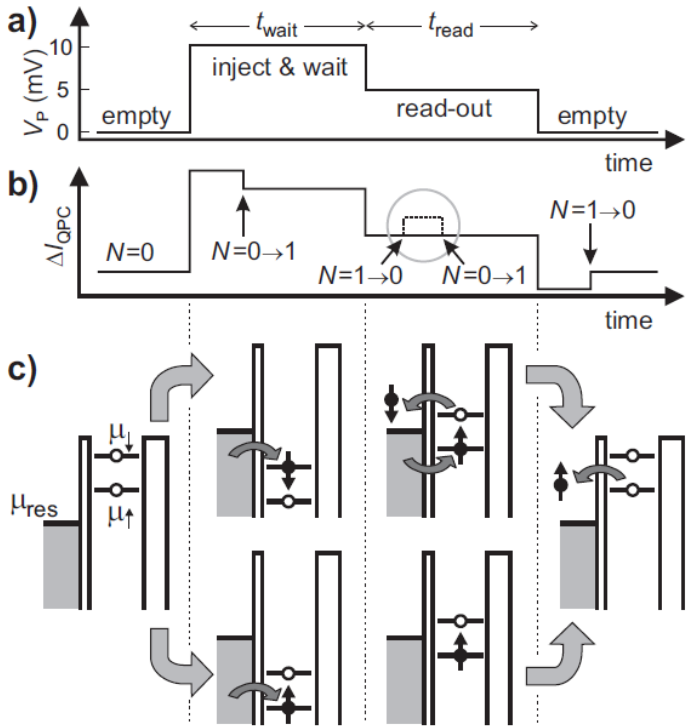


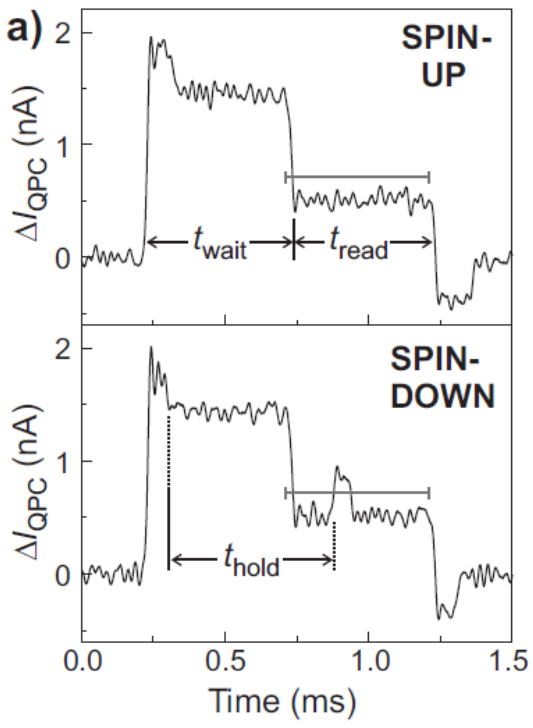


Measurement Method: Spin to Charge Conv.

Energy Selective Readout

The information is encoded in the electron spin which is detected as a change in tunneling current.

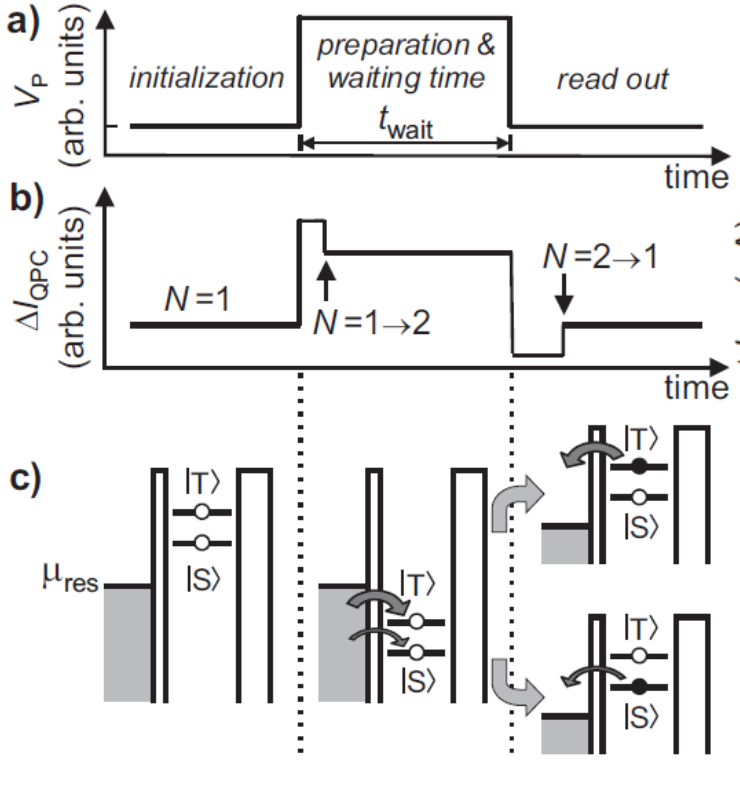


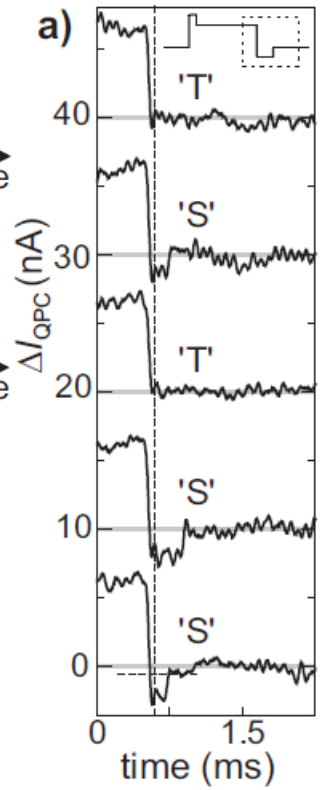


[10]

Tunnel Rate Selective Readout

The information is encoded in the tunneling rate of the charge carrier as it travels back into the reservoir.





Larmor Precession

$$\vec{B} = B_o\vec{z}$$

$$\hat{H} = -\mu \cdot \vec{B}$$

$$\hat{H} = \frac{\hbar\omega_o}{2} \cdot \begin{pmatrix} 1 & 0 \\ 0 & -1 \end{pmatrix}$$

$$\omega_o = \frac{e \cdot B_o}{m_e}$$

$$|\psi(0)\rangle = \cos\frac{\theta}{2}|\uparrow\rangle + e^{i\phi}\sin\frac{\theta}{2}|\downarrow\rangle$$

$$|\psi(t)\rangle = e^{\frac{-i\omega_o t}{2}}\left(\cos\frac{\theta}{2}|\uparrow\rangle + e^{i(\phi+\omega_o t)}\sin\frac{\theta}{2}|\downarrow\rangle\right)$$

$$P_{+x} = |\langle +_x|\psi(t)\rangle|^2 = \frac{1}{2}\cdot[1 + \sin\theta\cos(\phi + \omega_o t)]$$

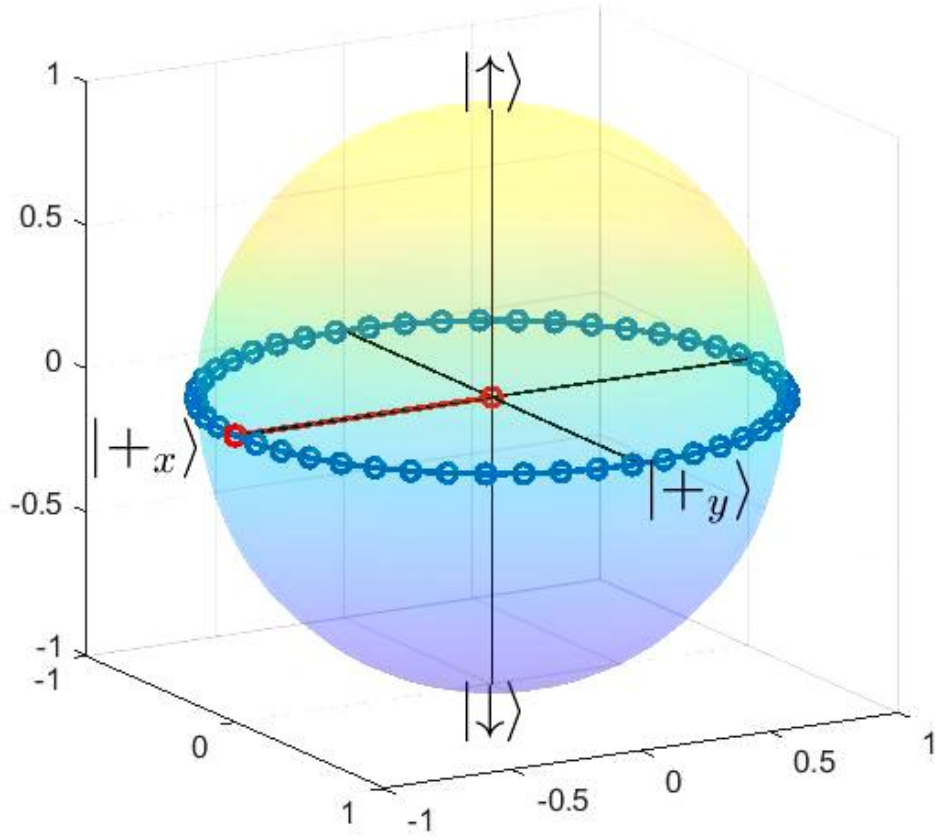
$$E_+ = +\frac{\hbar\omega_o}{2};\ E_- = -\frac{\hbar\omega_o}{2};\ \omega_o = \frac{\Delta E}{\hbar}$$

ω_o is the Larmor Frequency

Increasing $B_o \rightarrow$ Increasing ΔE & ω_o

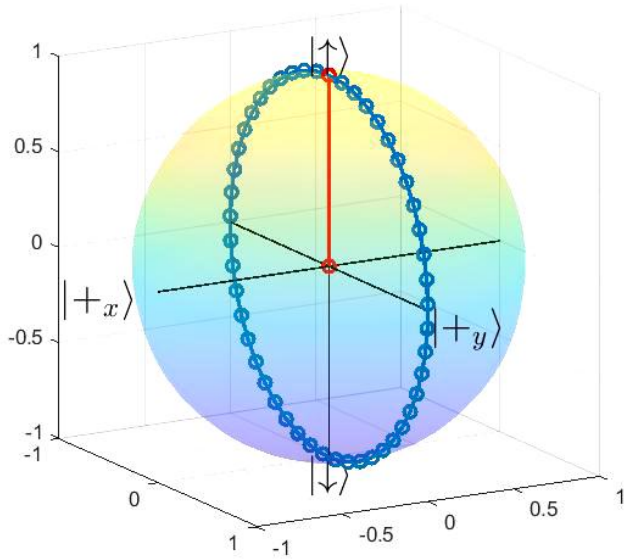
[30]

The trajectory of $|\psi(t)\rangle$ on the bloch sphere is the Larmor Precession.



Quantum Dot with an AC Magnetic Field (Rabi Oscillation)

The trajectory of $|\psi(t)\rangle$ on the bloch sphere due to excitation signal. The complete trajectory will also include Larmor precession (fast oscillations).



Excitation Signal

$$\vec{B} = B_o\vec{z} + \boxed{B_1 \cos\omega t\, \vec{x}} \;\; ; \;\; B_1 \ll B_o$$

$$\hat{H} = -\mu \cdot \vec{B}$$

$$\hat{H} = \frac{\hbar}{2} \cdot \begin{pmatrix} \omega_o & \omega_1 e^{-i\omega t} \\ \omega_1 e^{i\omega t} & -\omega_o \end{pmatrix} \leftarrow \textit{Time Dependent!}$$

Using rotation frame approximation & perturbation theory

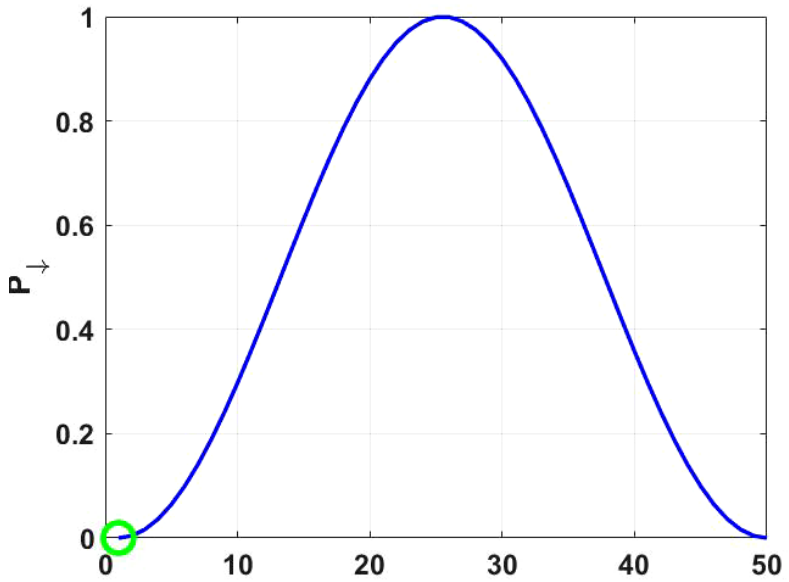
$$\hat{H} = \frac{\hbar}{2} \cdot \begin{pmatrix} -\Delta\omega & \omega_1 \\ \omega_1 & \Delta\omega \end{pmatrix} \leftarrow \textit{Time Independent!}$$

$$\omega_o = \frac{e \cdot B_o}{m_e}; \;\; \omega_1 = \frac{e \cdot B_1}{m_e}; \;\; \Delta\omega = \omega - \omega_o$$

$$|\psi(0)\rangle = \cos\frac{\theta}{2}|\uparrow\rangle + e^{i\phi}\sin\frac{\theta}{2}|\uparrow\rangle$$

$$|\psi(t)\rangle \approx e^{\frac{-i(\phi+\omega_o t)}{2}}\left(\cos\left(\frac{\theta+\omega_1 t}{2}\right)|\uparrow\rangle + e^{-i(\phi+\omega_o t)}\sin\left(\frac{\theta+\omega_1 t}{2}\right)|\downarrow\rangle\right)$$

$$P_\downarrow = |\langle\downarrow|\psi(t)\rangle|^2 = \frac{\omega_1^2}{\Delta\omega^2+\omega_1^2}\sin^2\left(\frac{\sqrt{\Delta\omega^2+\omega_1^2}}{2}t\right) \quad \textbf{[30]}$$



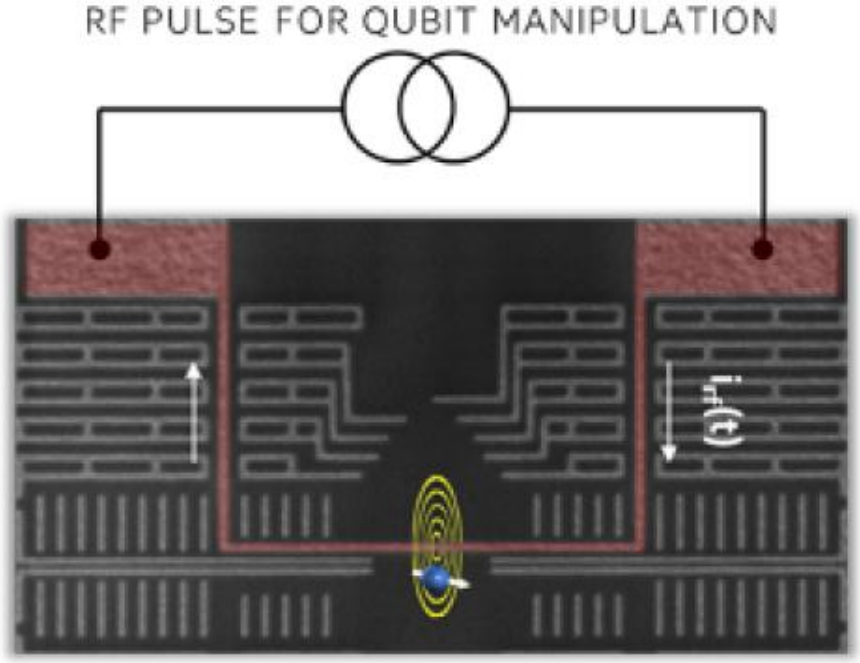
ω_o is the Larmor Frequency & ω_1 is the Rabi Frequency

Increasing excitation amplitude $B_1 \rightarrow$ Increasing ω_1

Modes of Qubit Excitation

ESR

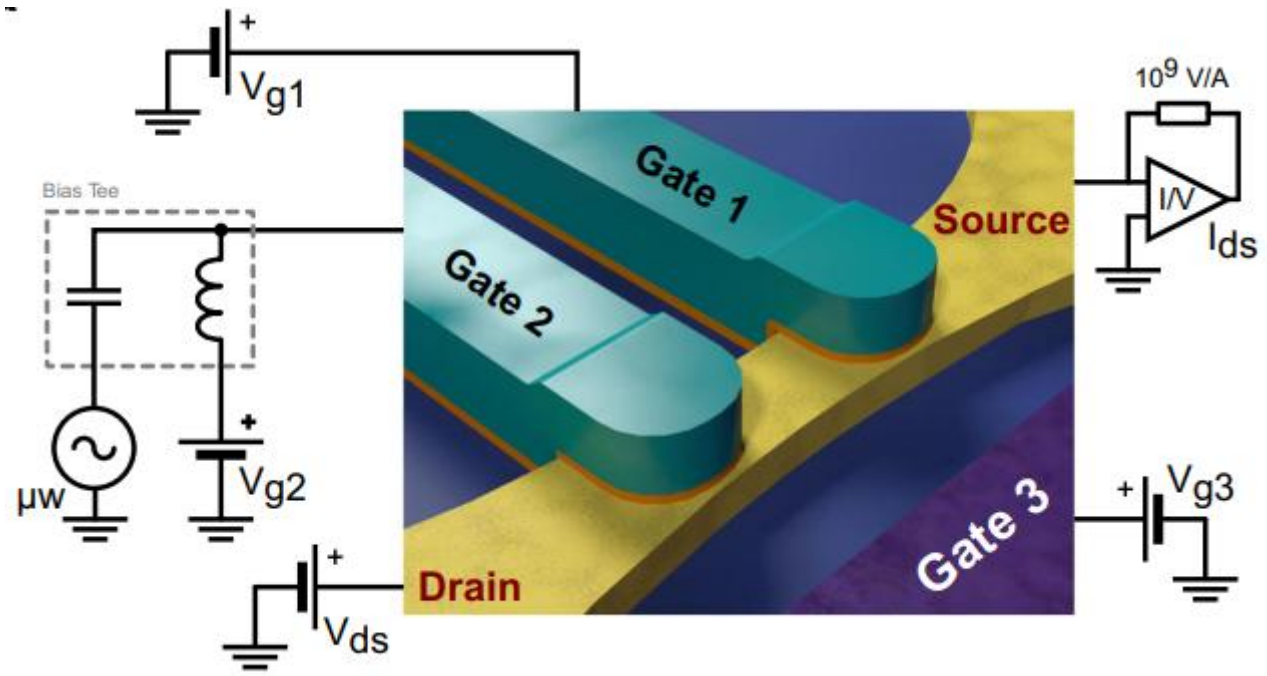
RF current through a loop conductor generates EM field in the vicinity of the quantum while the gradient from the static magnetic field determines the qubit addressability.



[15]

EDSR

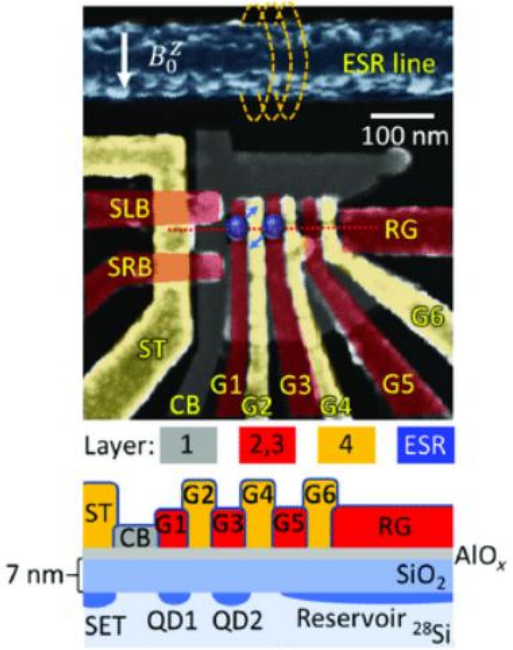
RF voltage on gate conductor (open load) generates E field in the vicinity of the quantum while the gradient from the static magnetic field determines the qubit addressability.



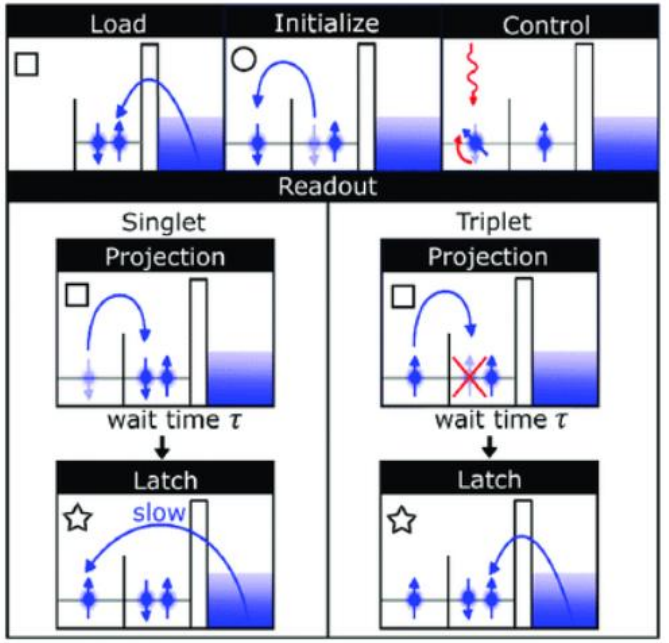
[16]

Readout Using Pauli Spin Blockade (PSB)

- Electron / holes are fermions and must obey Pauli Exclusion Principle
- PSB prevents the flow of electron/hole to/from quantum dot when neighboring dots are detuned
- This feature can be used to determine the state of the qubit using the energy selective readout or tunnel rate selective readout



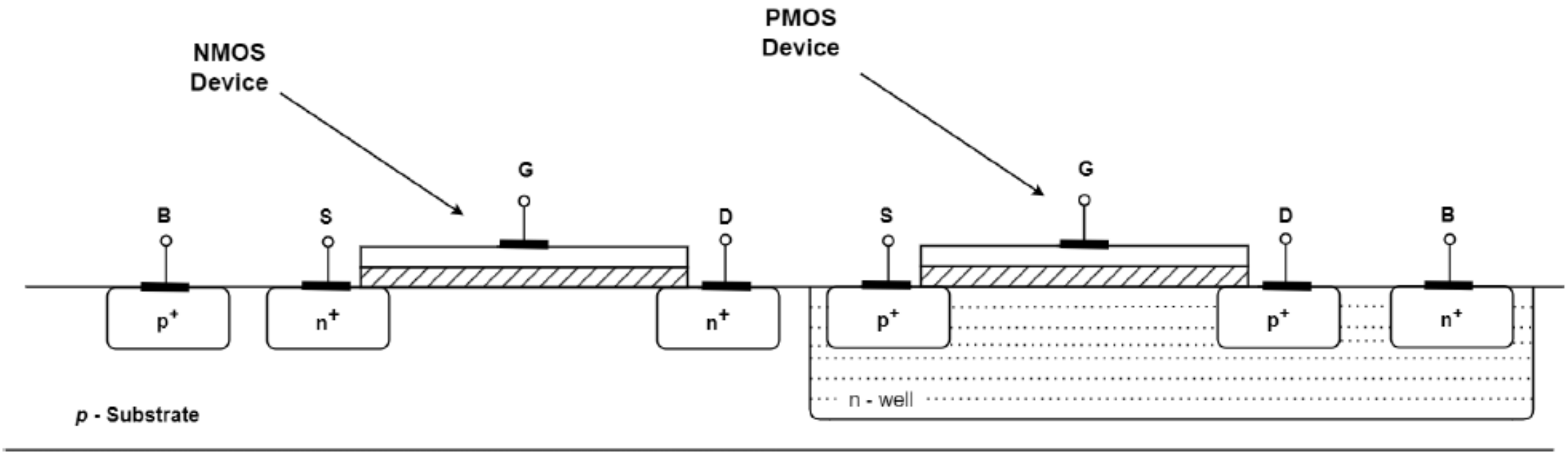
[32]



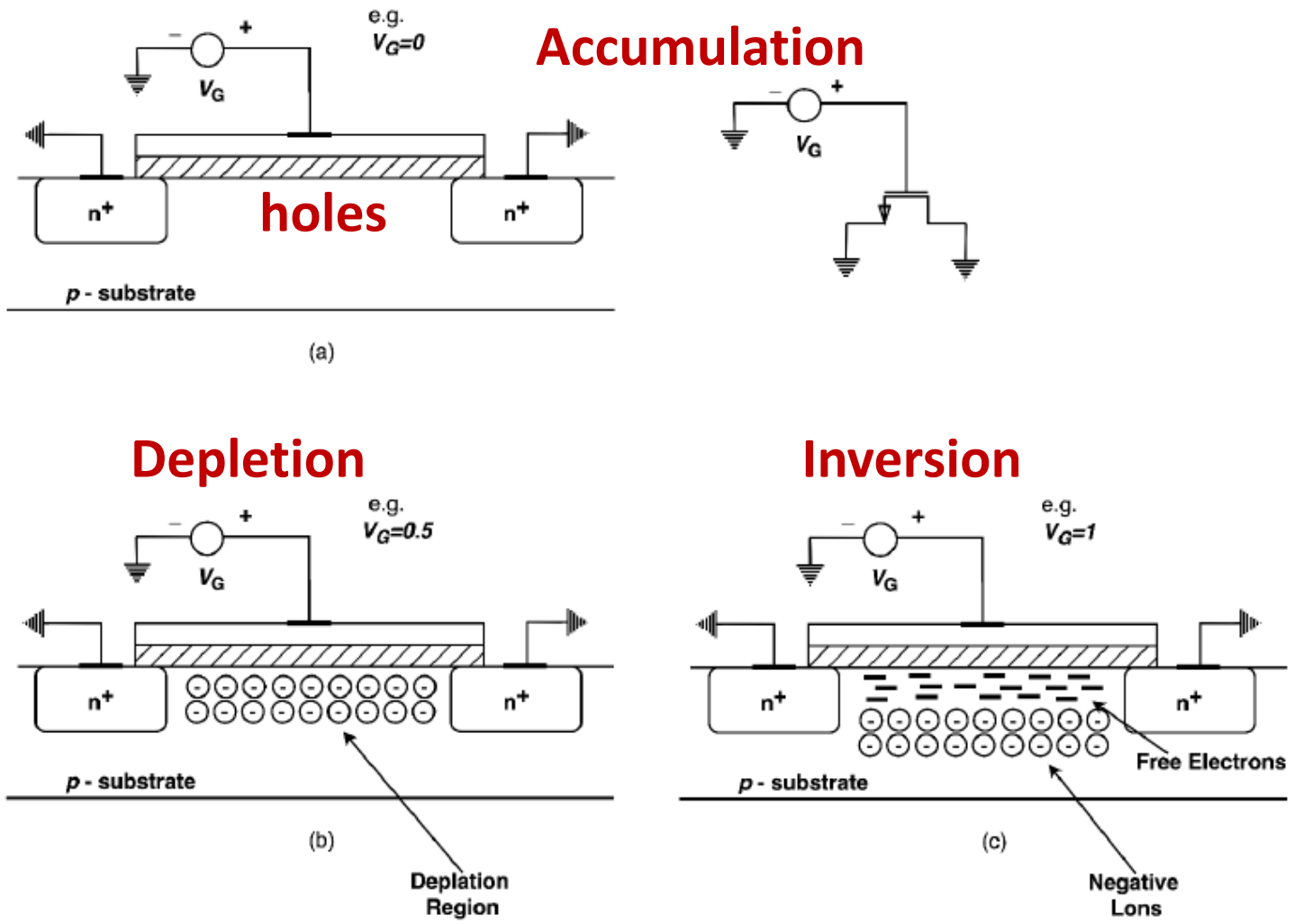
Part II: Cryogenic Behavior of CMOS Transistor

- Subthreshold Swing
- Bulk vs. FD-SOI Transistor
- Carrier Freeze Out
- The ‘Kink’ Effect & Impact Ionization

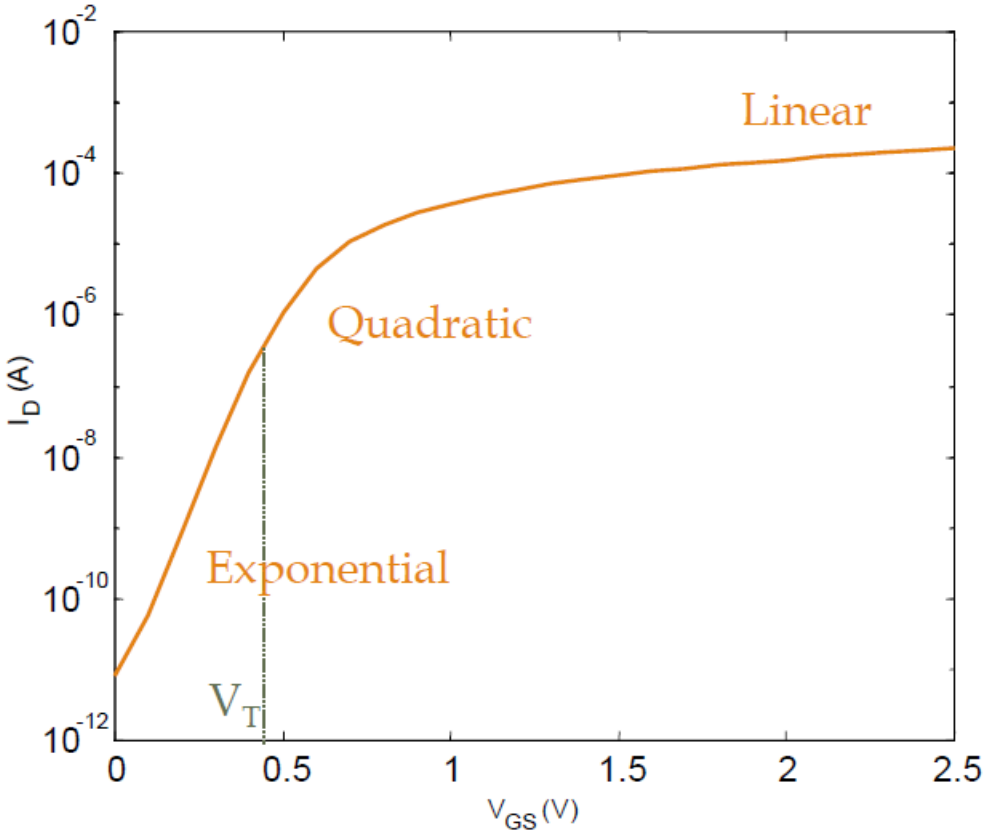
The Bulk CMOS Transistor



The Bulk CMOS Transistor



Subthreshold Swing

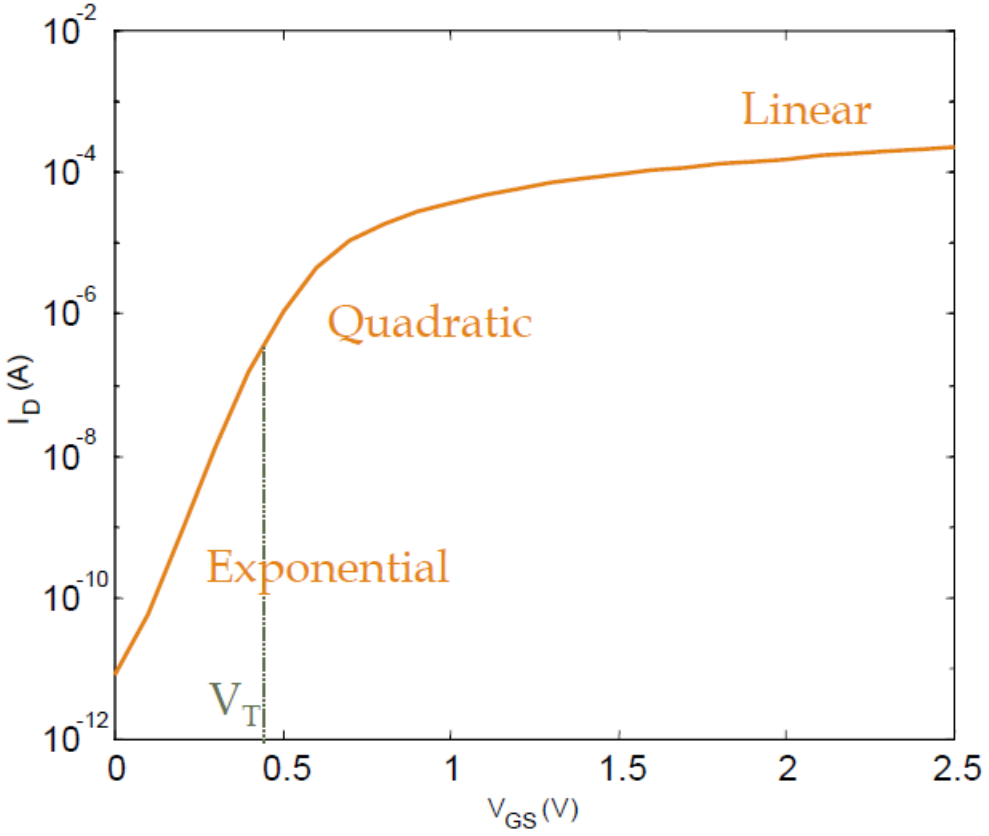


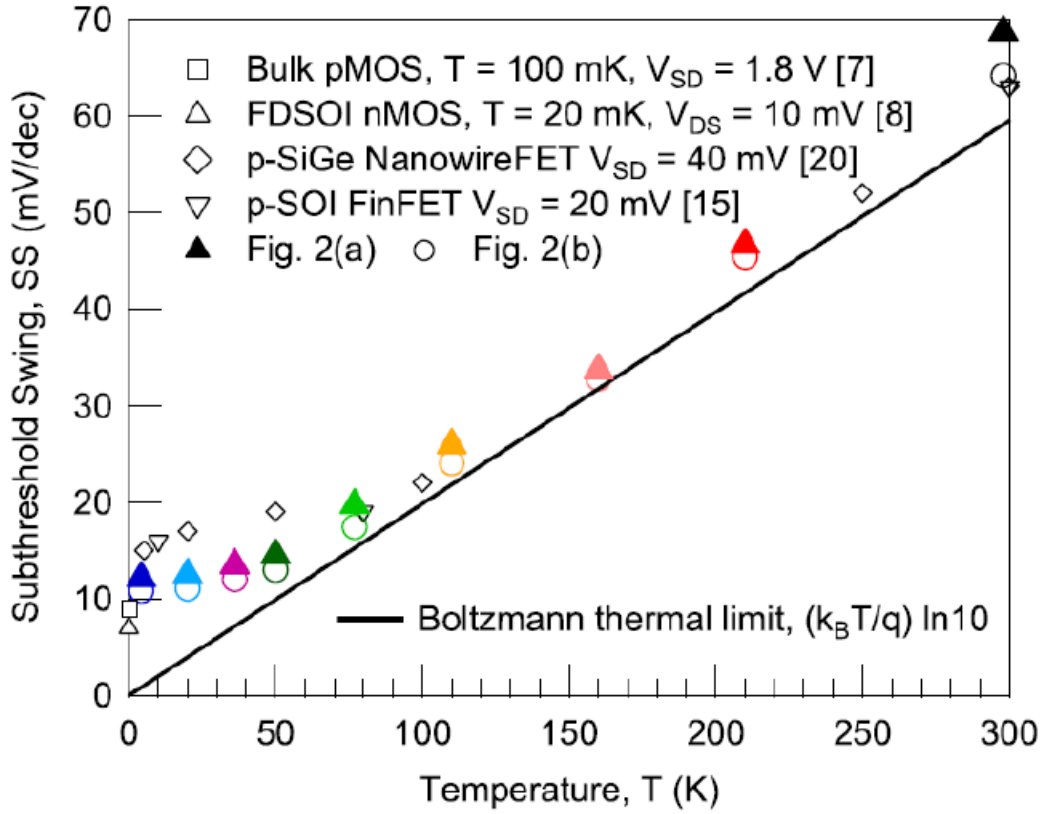
S is ΔV_{GS} for I_{D2}/I_{D1} =10

$$I_D \sim I_0 e^{\frac{qV_{GS}}{nkT}}, \quad n = 1 + \frac{C_D}{C_{ox}}$$

$$S = n\left(\frac{kT}{q}\right)\ln(10)$$

Subthreshold Swing

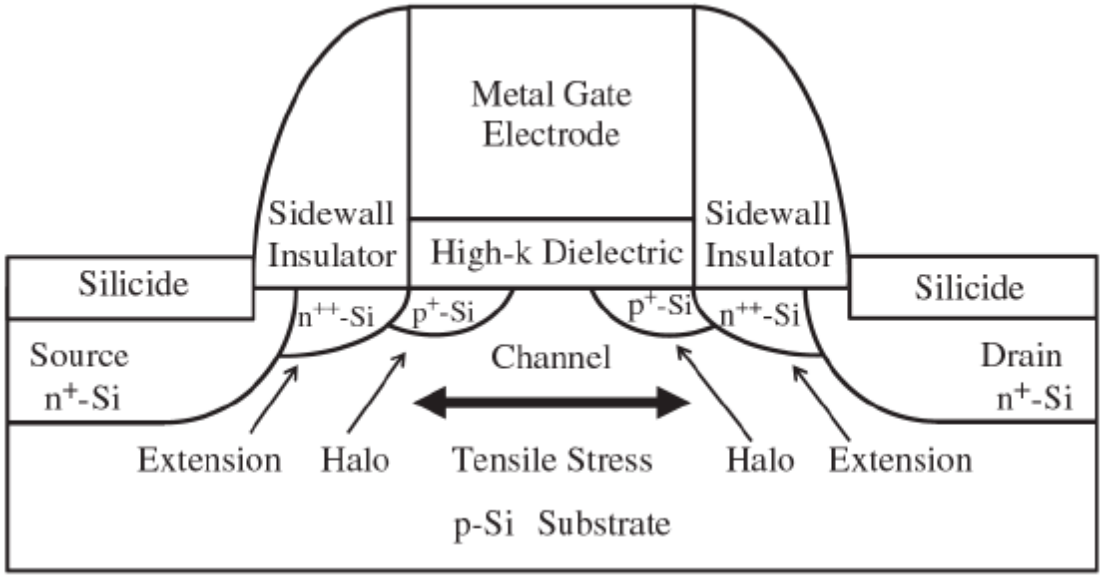




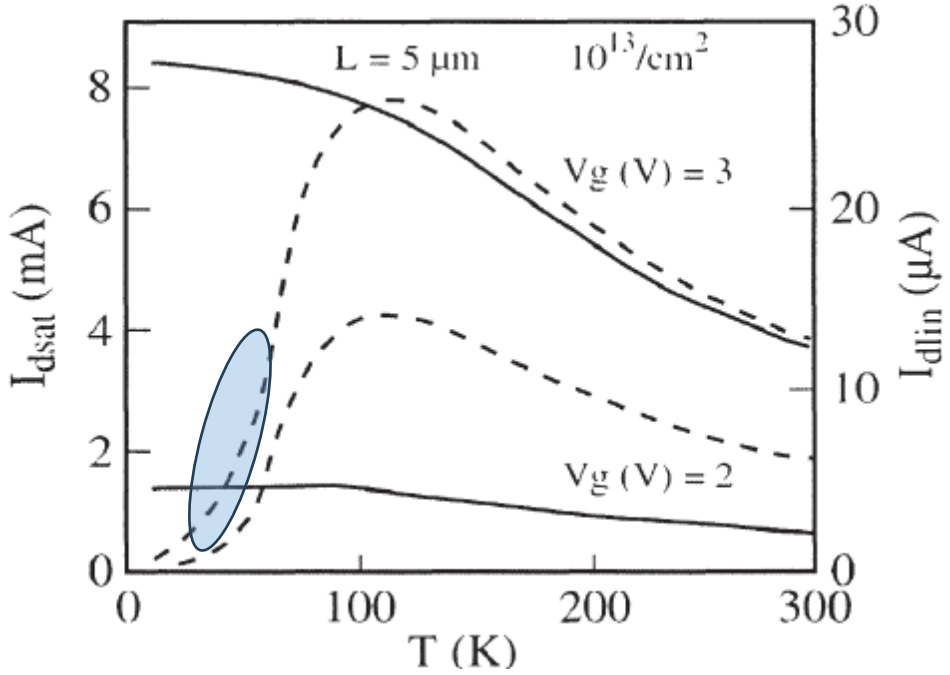
A. Beckers et al., arXiv:1811.09146, 2019.

Carrier Freeze Out

Lightly Doped Regions and p-SUB in the channel
Freeze Out at cryogenic temperatures.



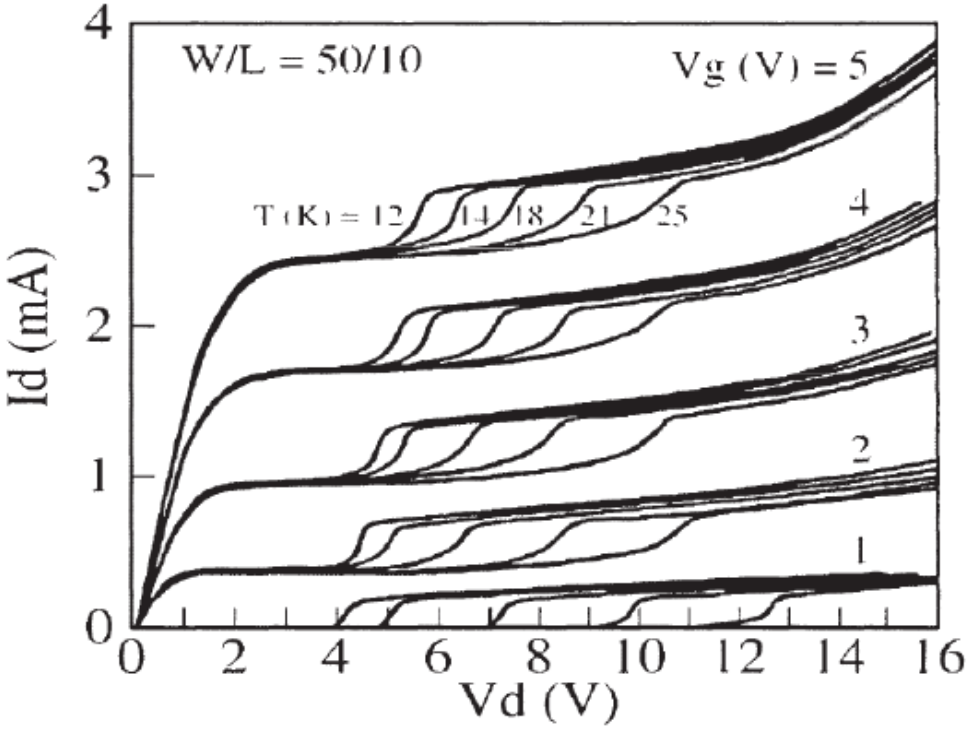
[41]



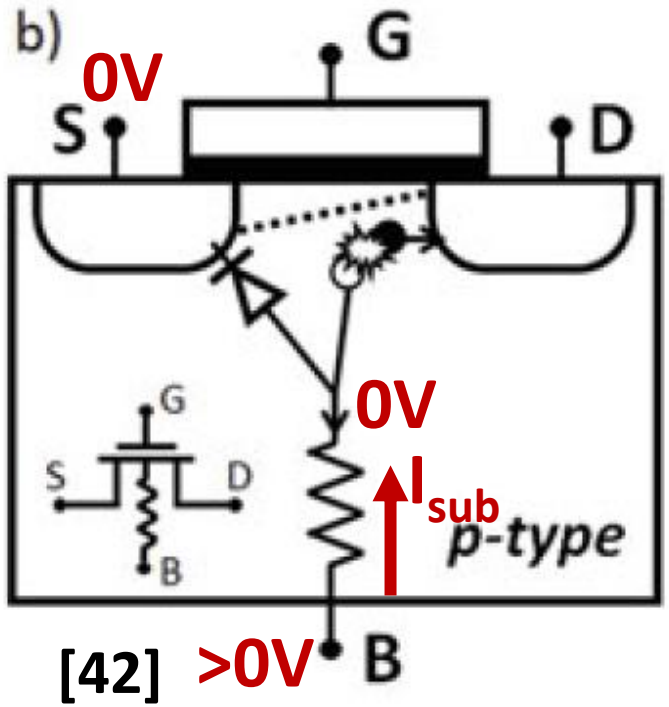
The ‘Kink’ Effect

Higher V_{BS} → V_B >V_S
→ Lower V_{th} → Higher I_{ds}

Sudden increase in Id at High Vd

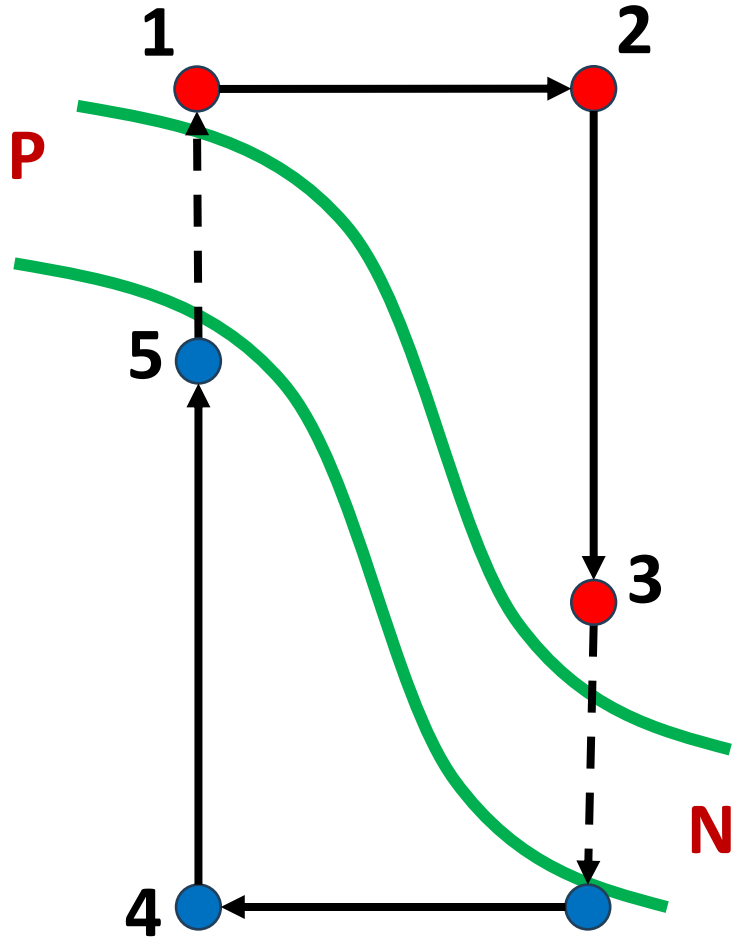


Substrate entering Freeze Out



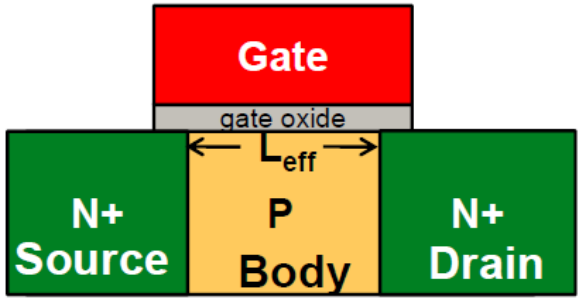
[42]

Impact Ionization Current

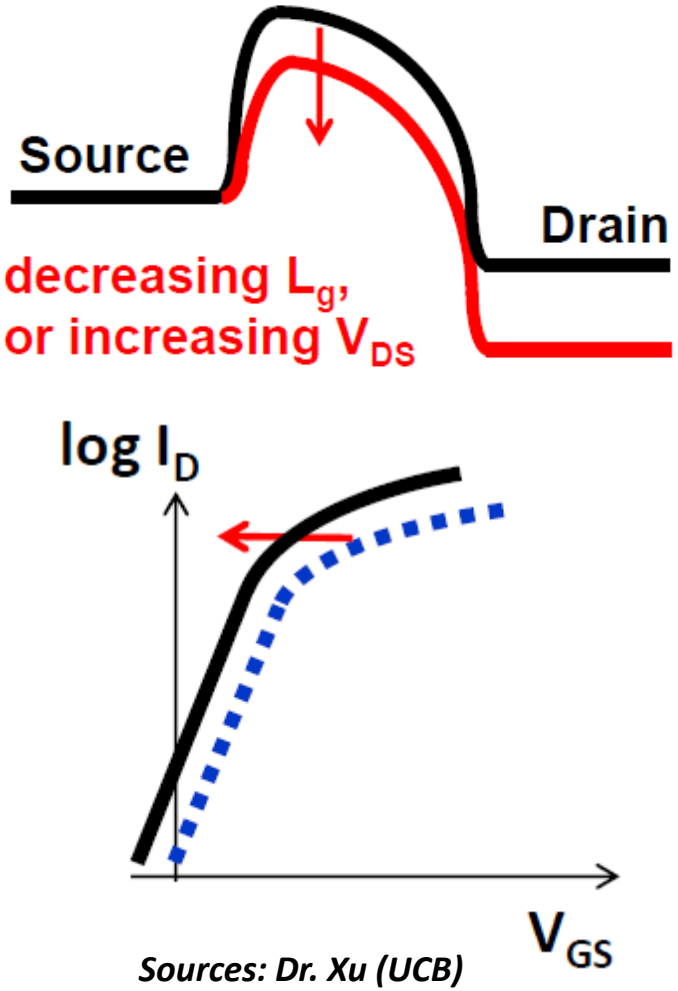


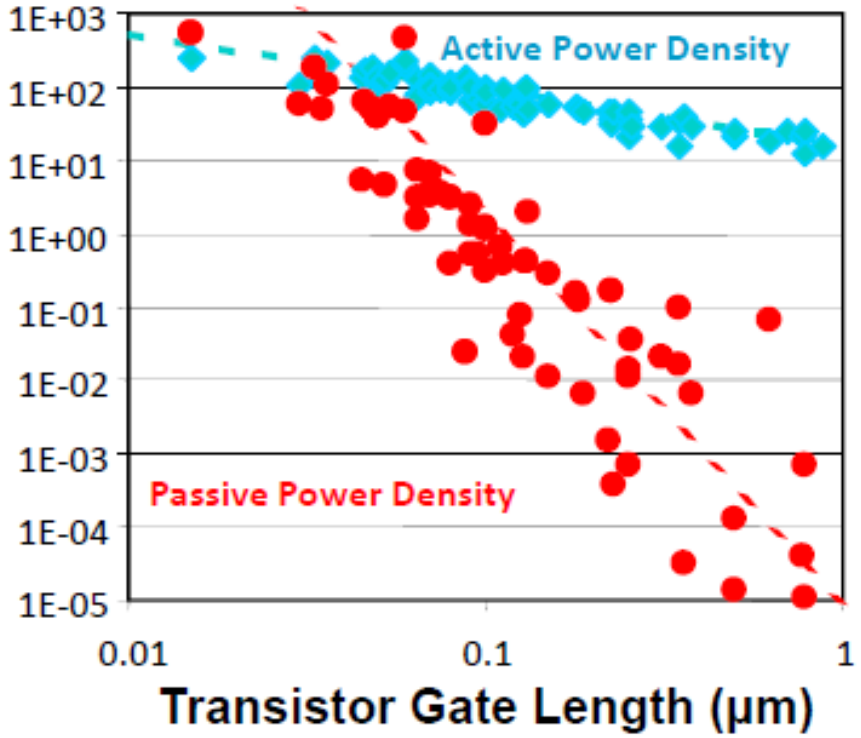
Challenges with Device Scaling

1959:Metal-Oxide-Semiconductor Field Effect Transistor



Drain Induced Barrier Lowering



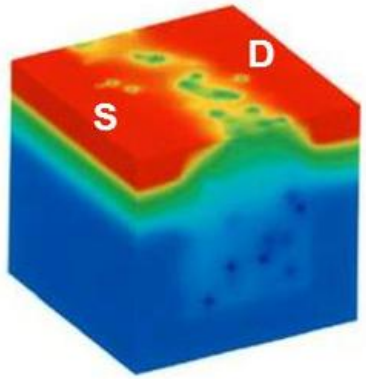


Source: B. Meyerson (IBM)
Semico Conf., January 2004

Sources: Dr. Xu (UCB)

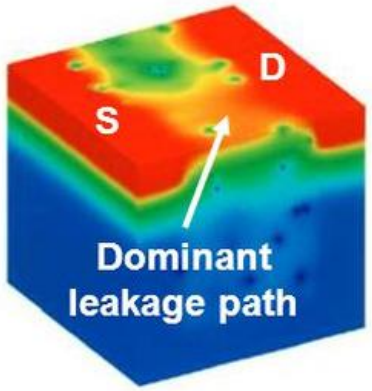
Challenges with Device Scaling

Random Dopant Fluctuation (RDF)



Evenly distributed dopants

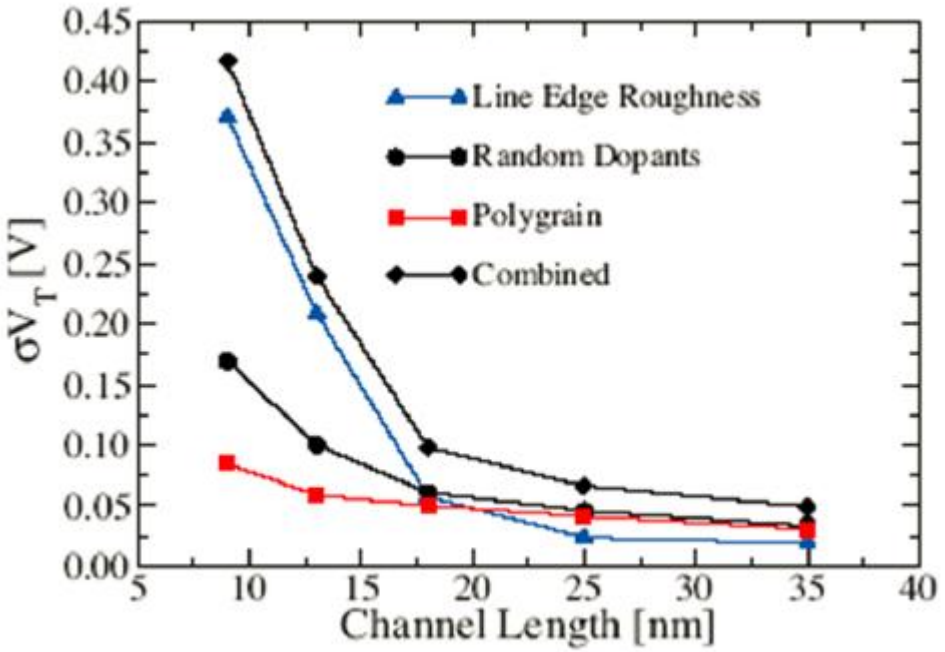
V_T=0.78V, 130 dopants, L_{eff} = 30nm



Unevenly distributed dopants

V_T=0.56V, 130 dopants, L_{eff} = 30nm

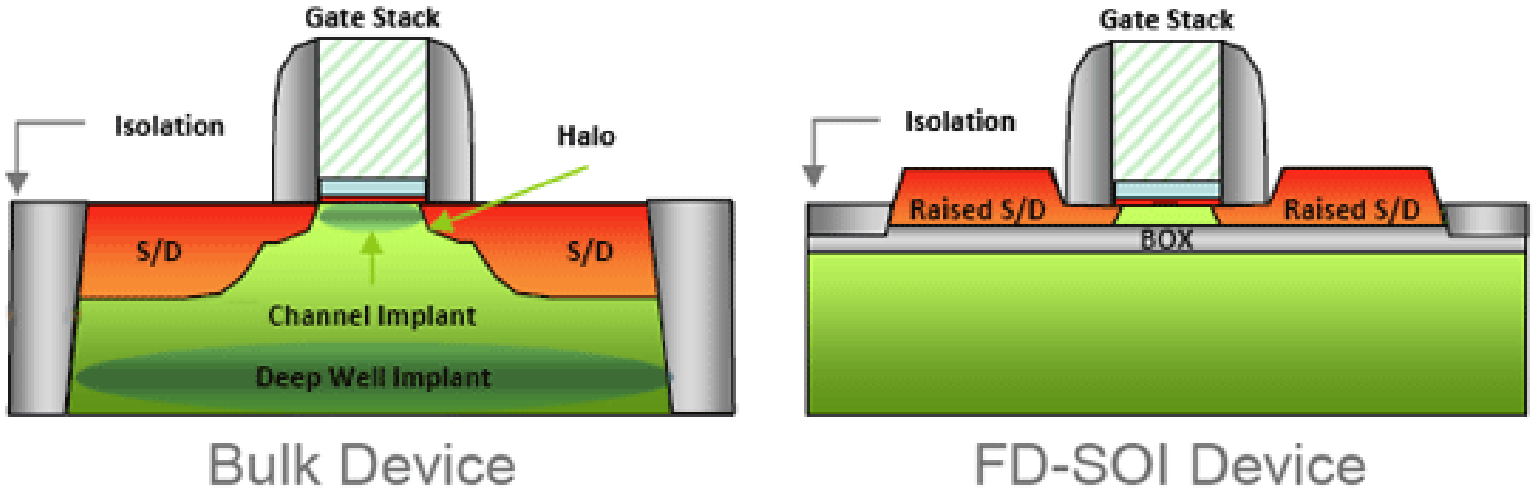
3D simulation results on surface potential A. Asenov, TED 1998



A. Asenov, *Symp. VLSI Tech. Dig.*, p. 86, 2007

Going from Bulk to FD-SOI

- Steps:
  1. Insert Buried Oxide (BOX) → Reduces leakage current
  2. Thin Body → Reduces leakage current
  3. Remove doping from channel (enabled by #2)
     - Reduces RDF
     - Enables “Fully Depleted Channel”



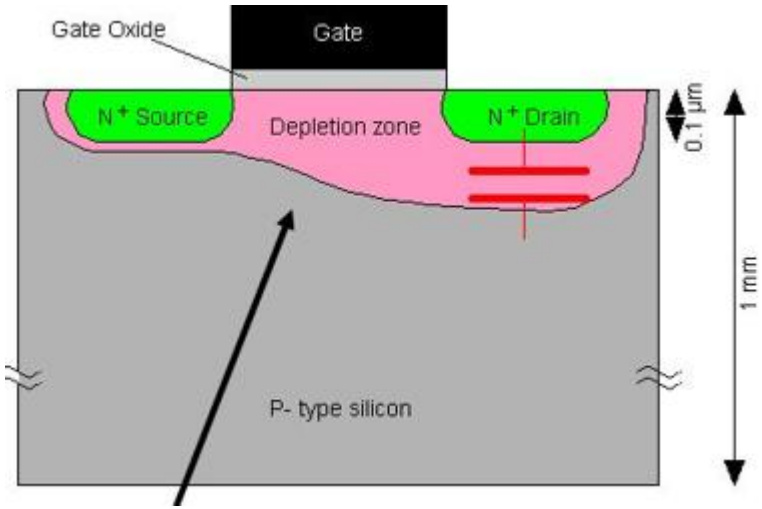
Bulk Device

FD-SOI Device

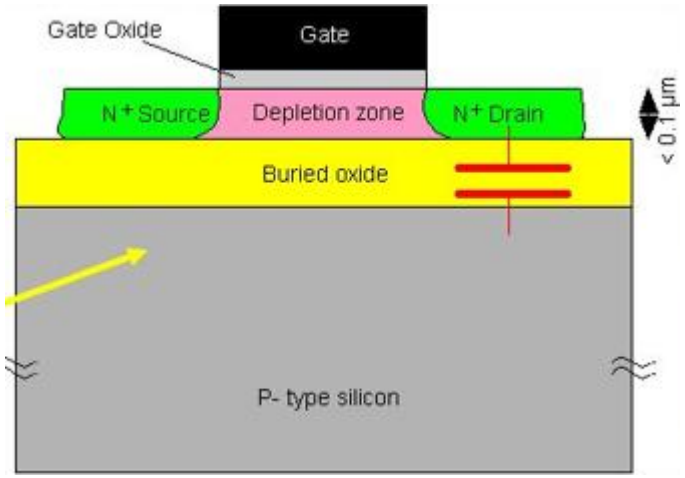
The fully depleted SOI transistor at 20 nm is significantly simpler than even a simplified version of the bulk CMOS transistor.

Sources: ARM Ltd

BULK

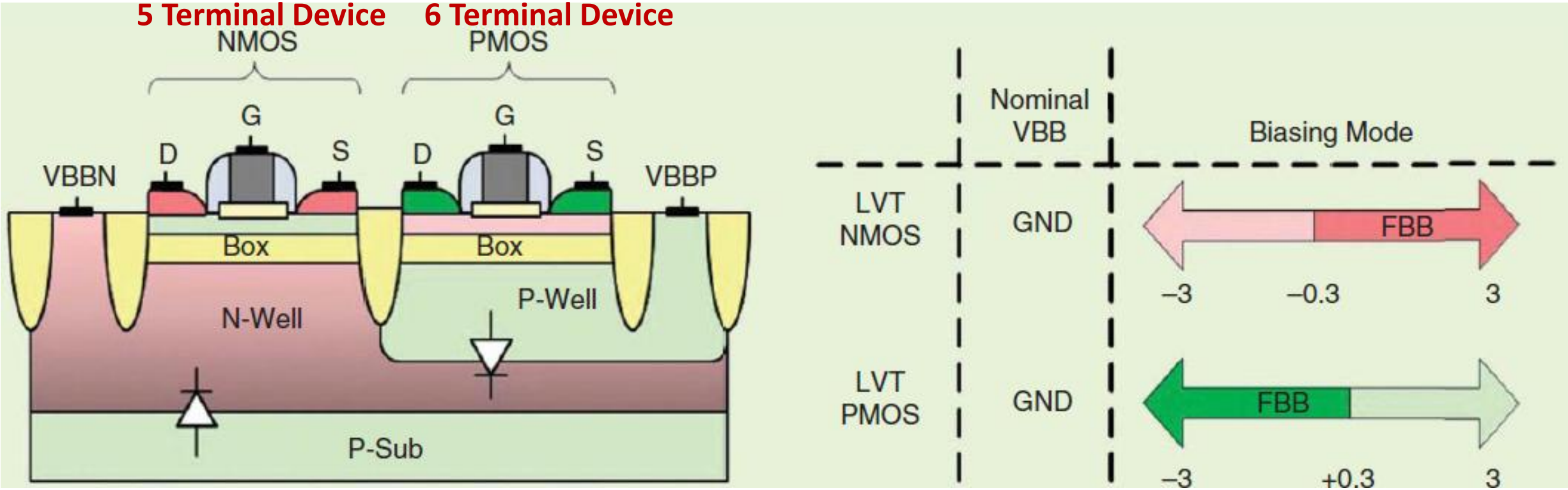


FD-SOI



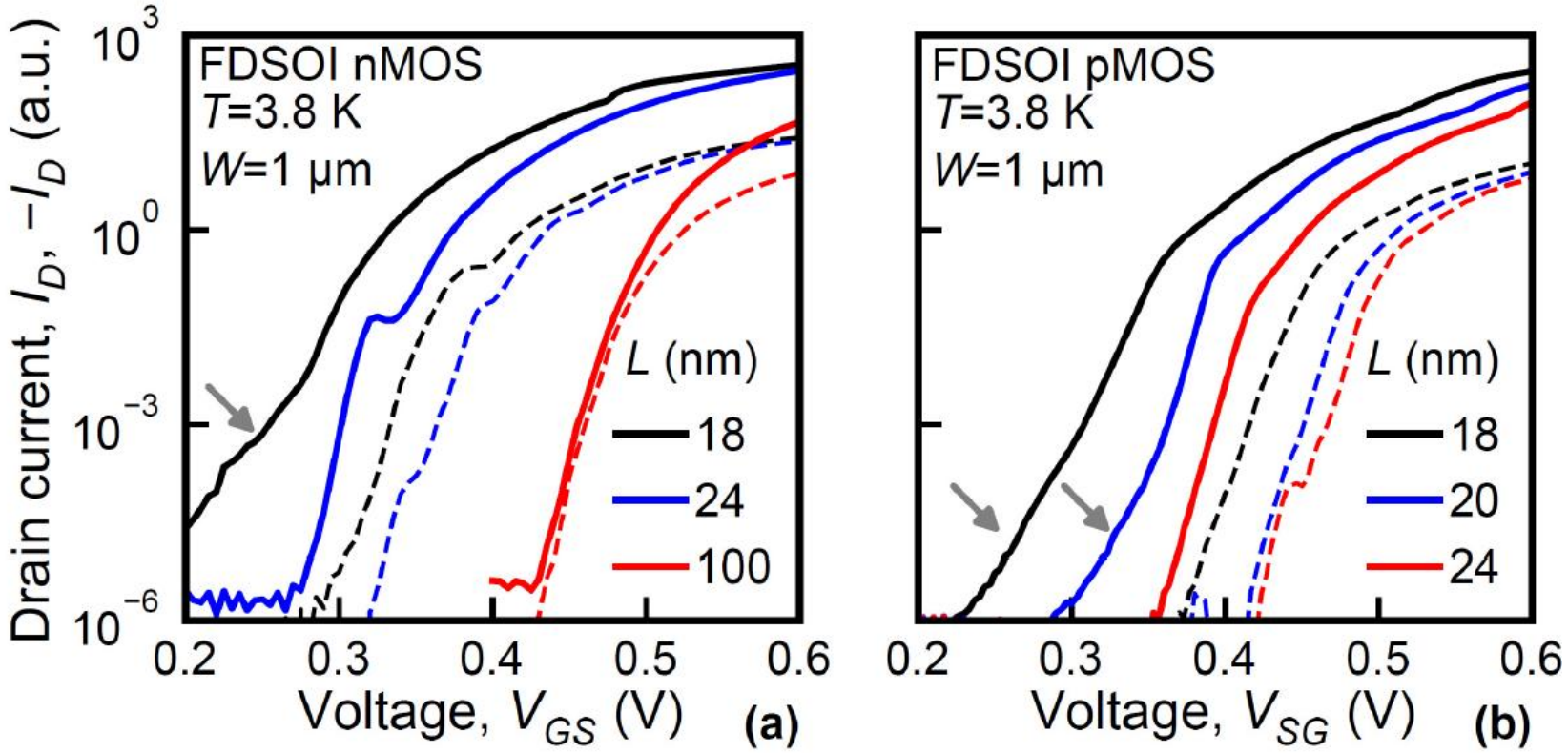
Source: J. P. Colinge, UC Davis

Fully Depleted SOI Transistor



[40]

Quantum Effects in Short Channel Devices



Dashed lines: $V_{DS} = 10\ mV$ (linear)
Solid lines: $V_{DS} = 0.8\ V$ (saturation)

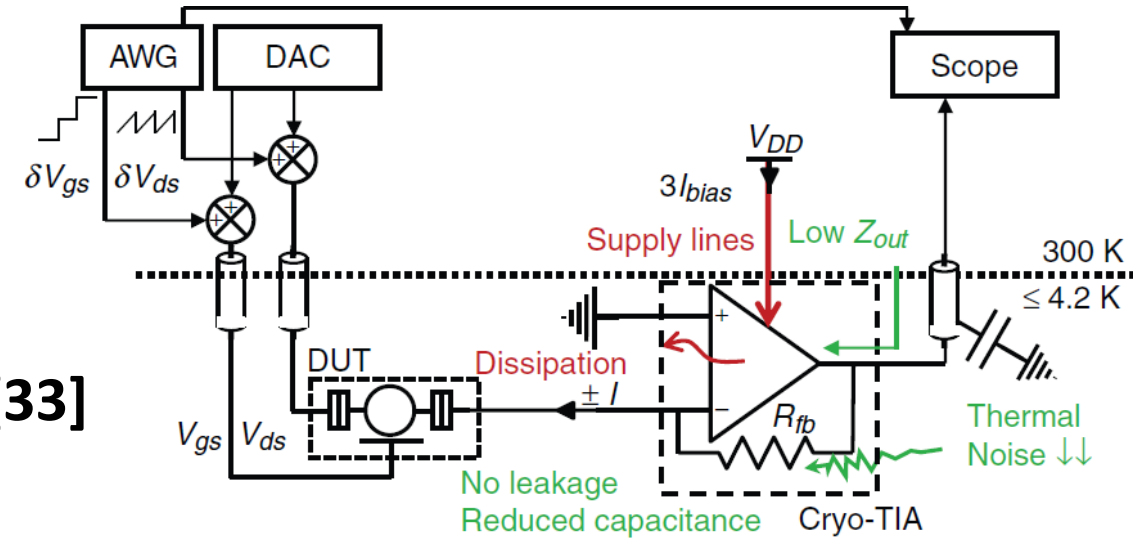
[42]

Part III: Cryogenic Control Electronics

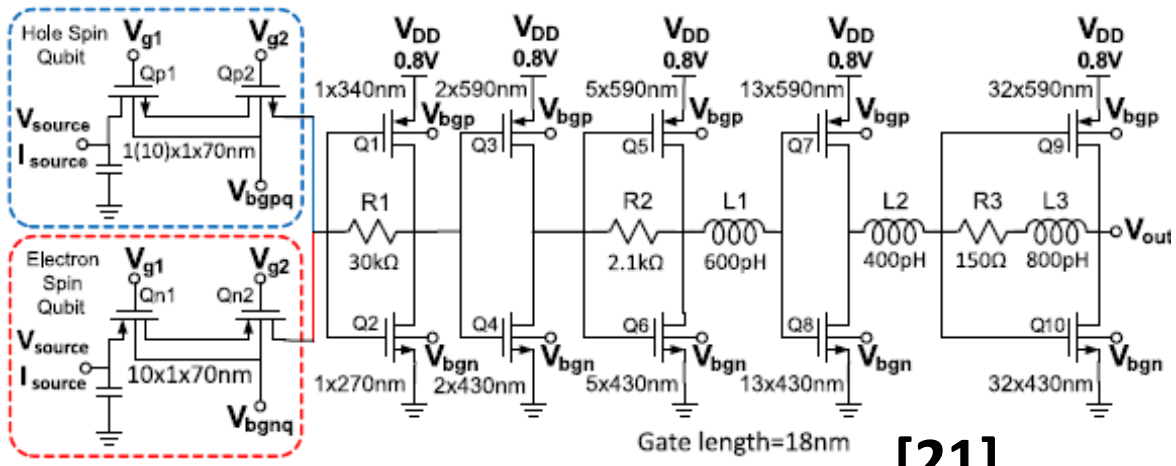
- Readout Chain Architecture
- Bias DACs
- Voltage Pulsers
- RF Waveform Generation
- Quantum Control & Readout SoC

RTIA Based Current Sensor

- Charge sensor is coupled to a RTIA
- Gain is set by resistive feedback
- Bandwidth limited due to stability



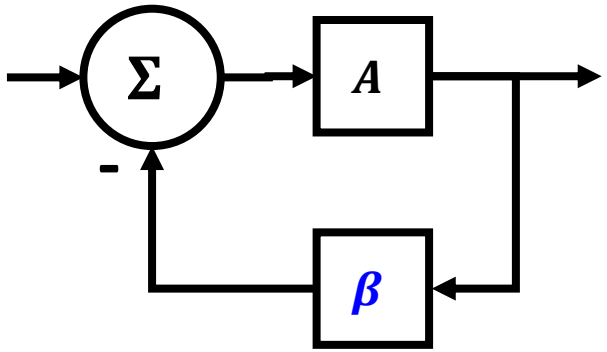
[33]



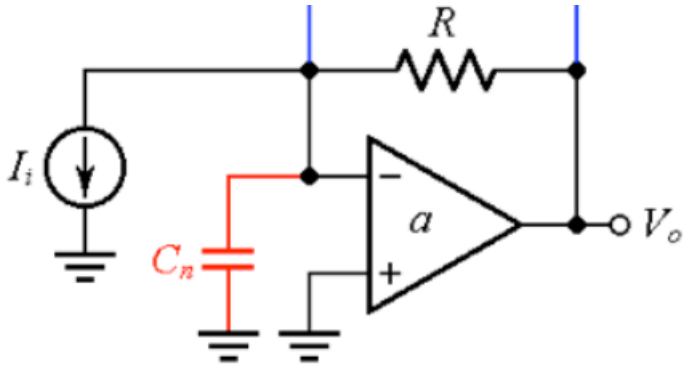
[21]

Stability and Bandwidth Trade-off

Barkhausen Criteria

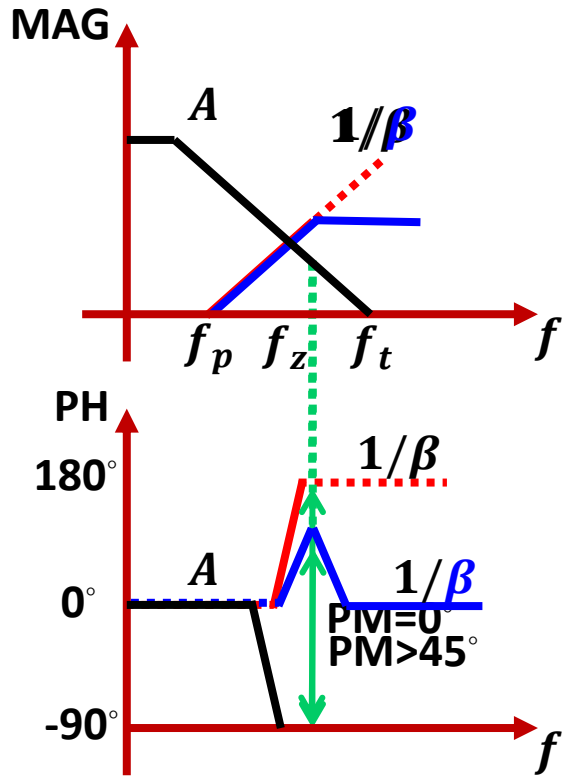


$$H = \frac{A}{1 + A\beta}$$



$$f_p = \frac{1}{2\pi R(C_n + C_f)}$$

$$f_z = \frac{1}{2\pi R C_f} \quad C_f = \sqrt{\frac{C_n + C_f}{2\pi R f_t}}$$



[34]

With high gain (R), C_f is small. Implementation challenge.

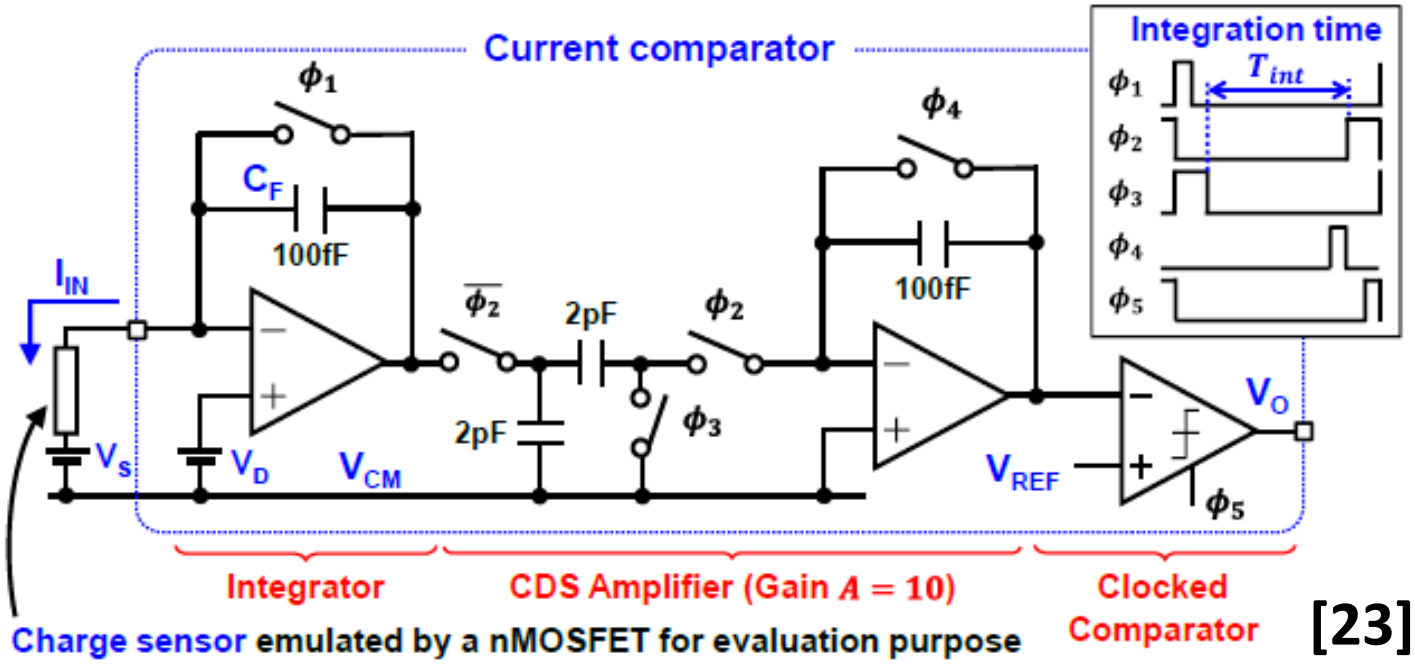
The RTIA design space with high R and C_n with the goal of achieving fast readout time is somewhat limited.

Is there a better alternative?

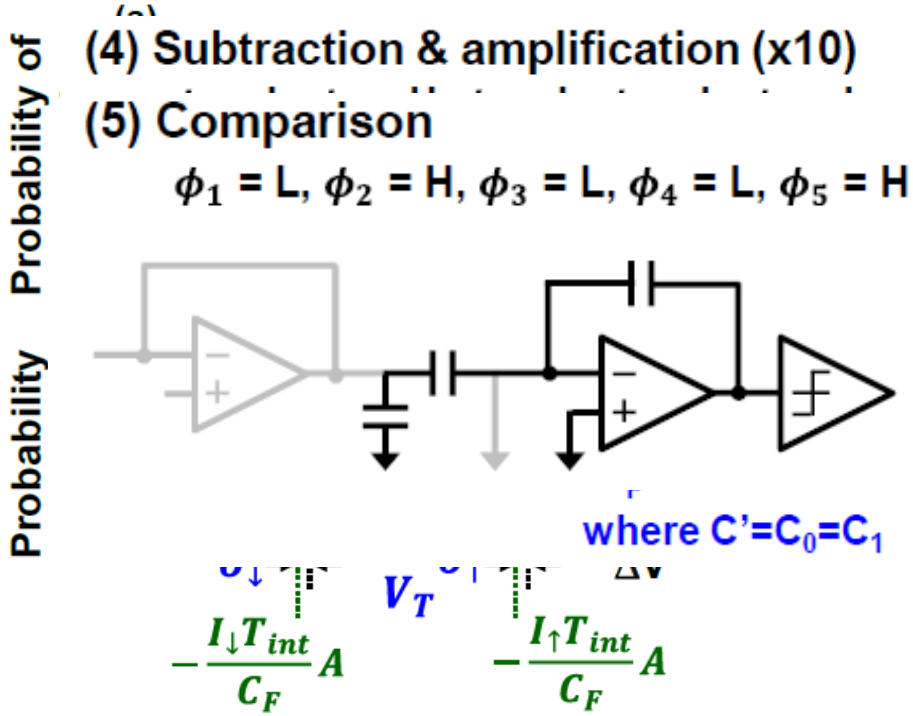
CTIA Based Current Sensor

- Maximum bandwidth equation simpler than RTIA

$$f_{max} \approx GBW \cdot \frac{C_F}{C_F + C_p}$$

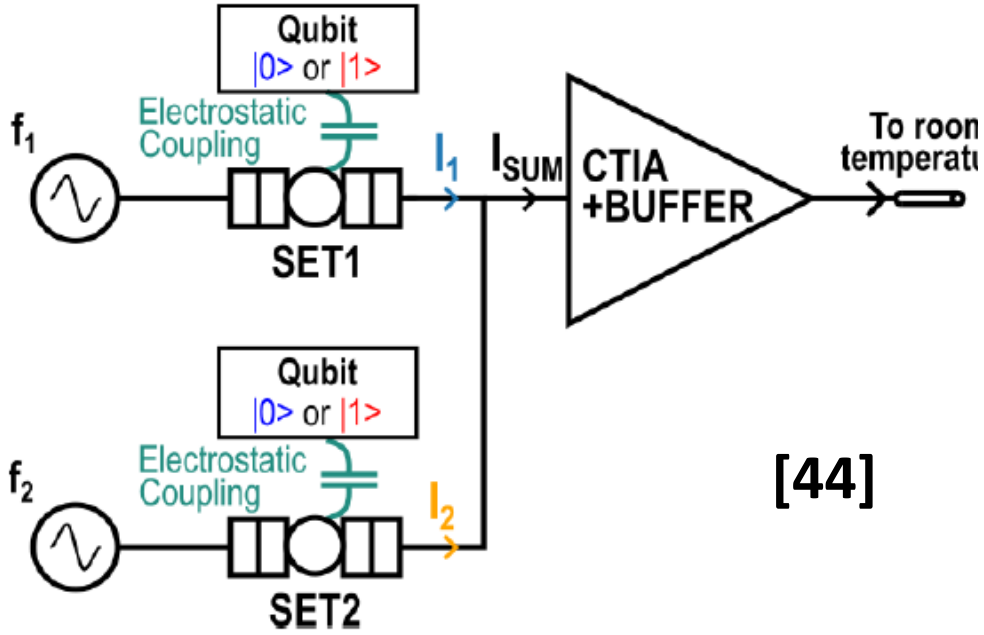


[23]

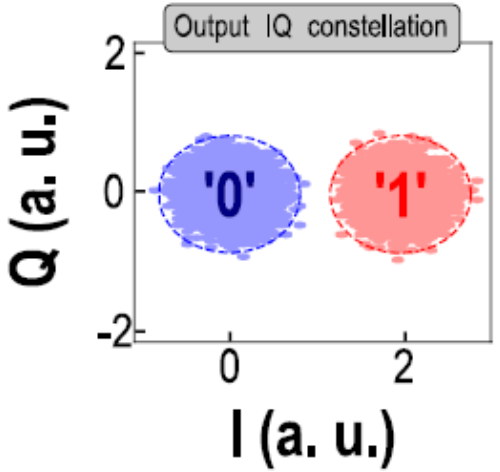


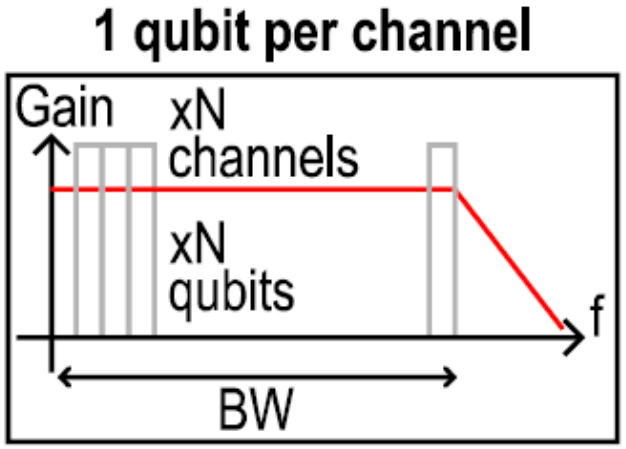
equal1

CTIA with Multiplexing



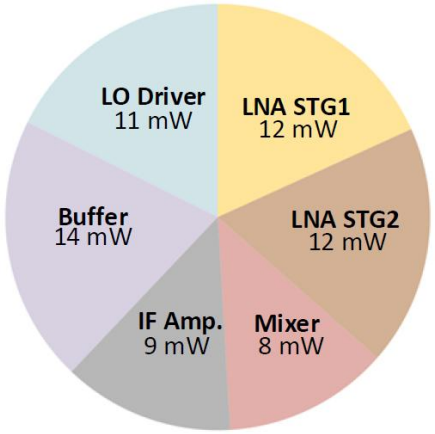
[44]





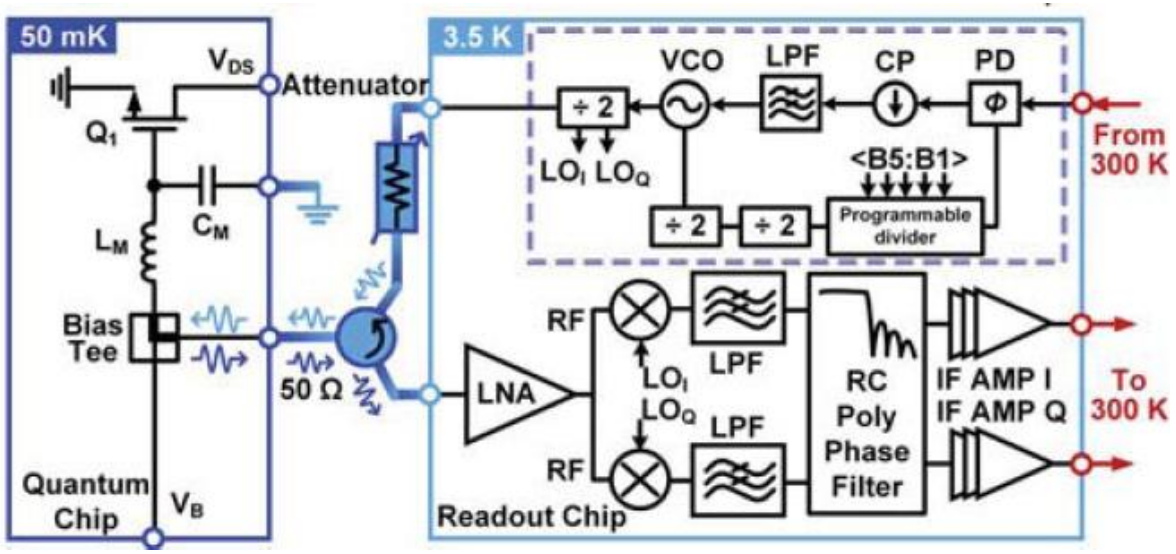
RF Reflectometry Based Receivers

- External components: superconducting resonator and coupler
- Qubit readout are frequency division multiplexed
- Requires large number of frequency tuned resonators in the QPU
  - Not suitable for large scale integration



[35]

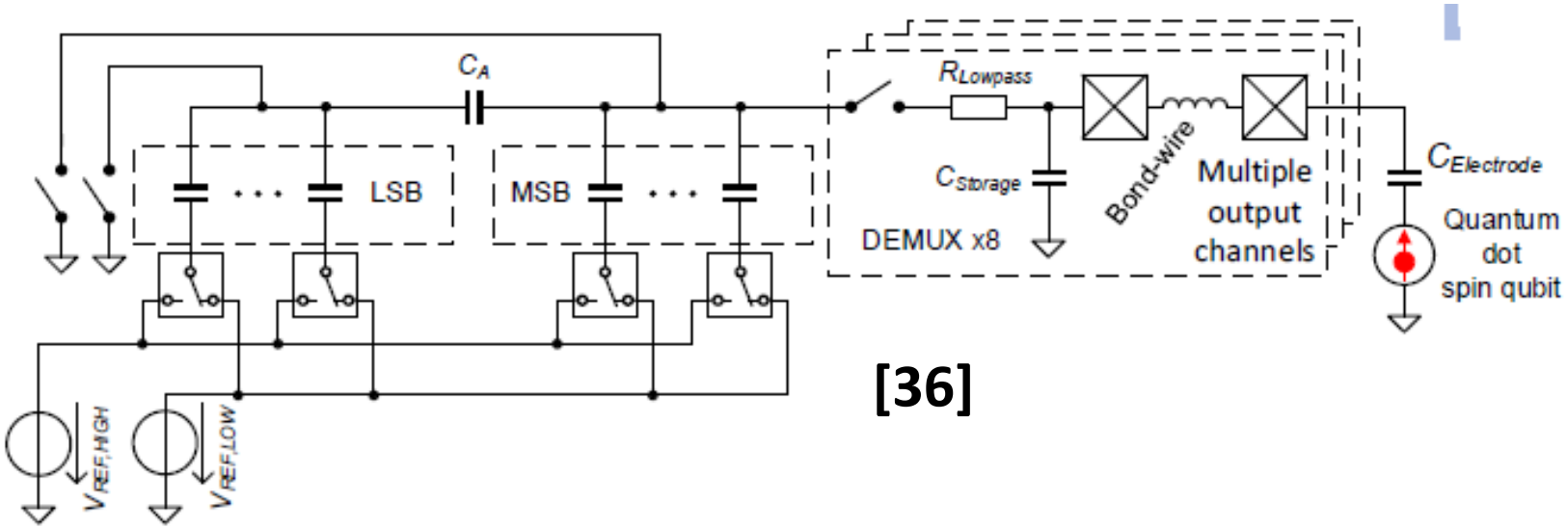
- Total power of 66mW at 4K



[20]

Voltage Pulsers

- Generate voltage pulses using charge re-distribution

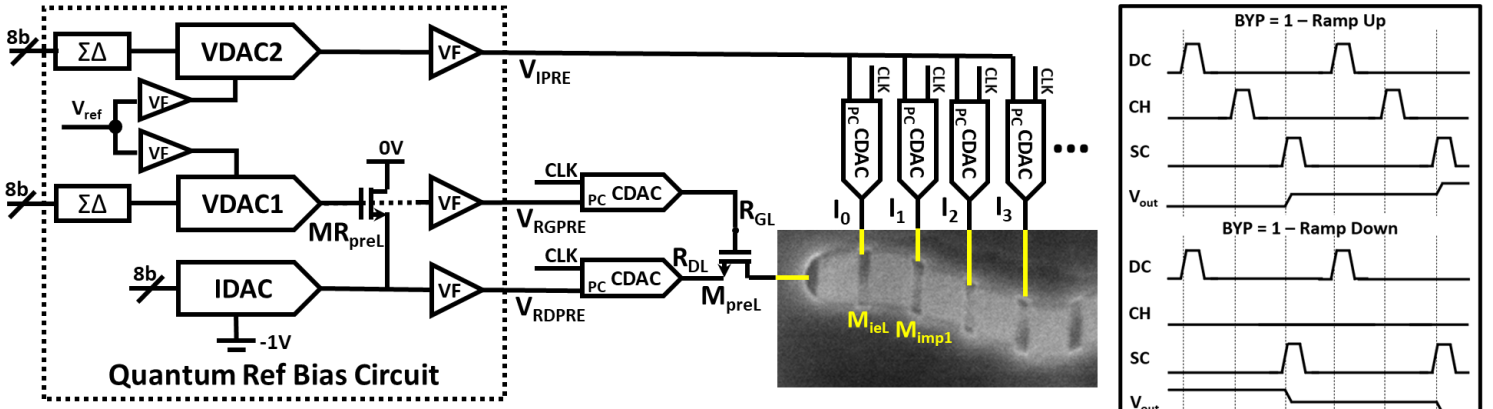


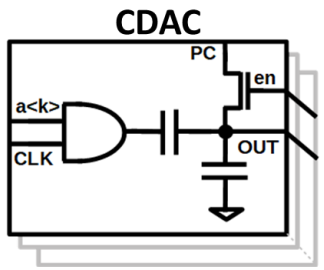
[36]

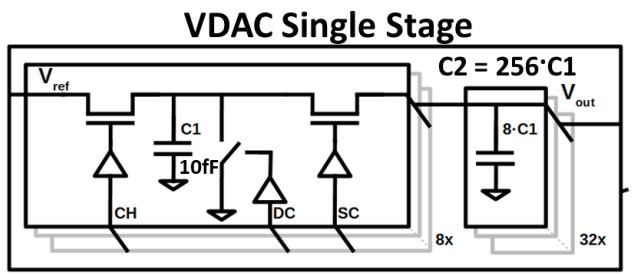
Characteristic	Specification
Output channels	8
Voltage range	0V to 1V
Resolution	13 Bit
Step size	~ 122 µV
Consumption	30 - 40 µW

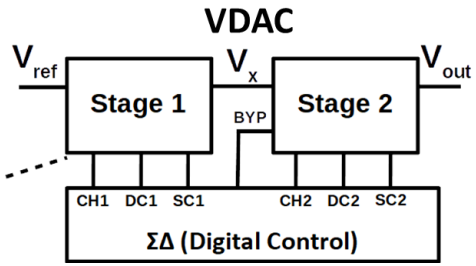
Bias DACs

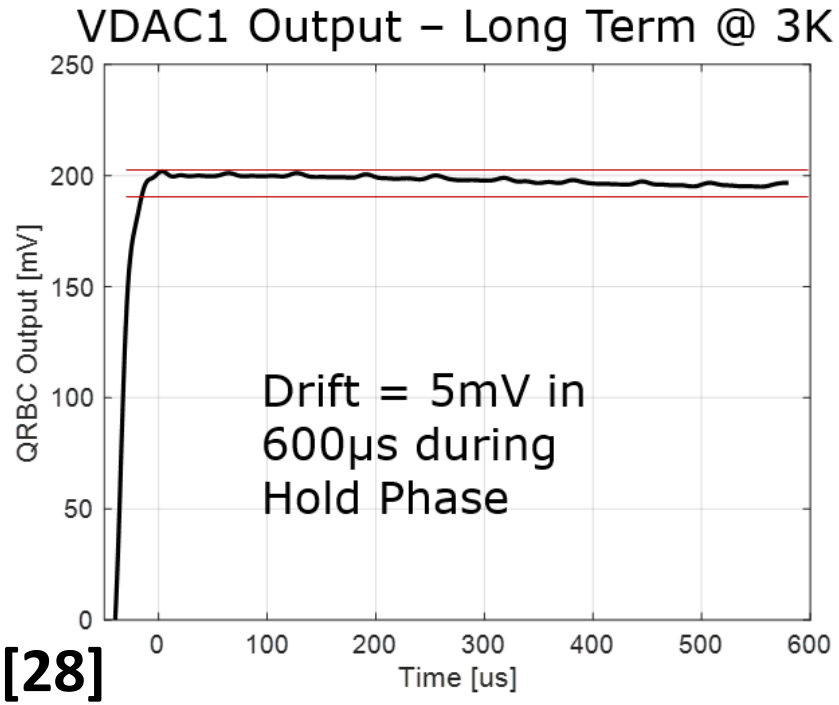
- VDAC1 and VDAC2 generates pre-charge for M_{pre} gate (R_{GL}) and all imposers from a single reference V_{ref}
- A replica pre-charge device MR_{pre} and 8-b IDAC generates M_{pre} source bias (R_{DL})
- The digital ΣΔ drives the switch capacitor network and ceases shortly before the quantum experiment







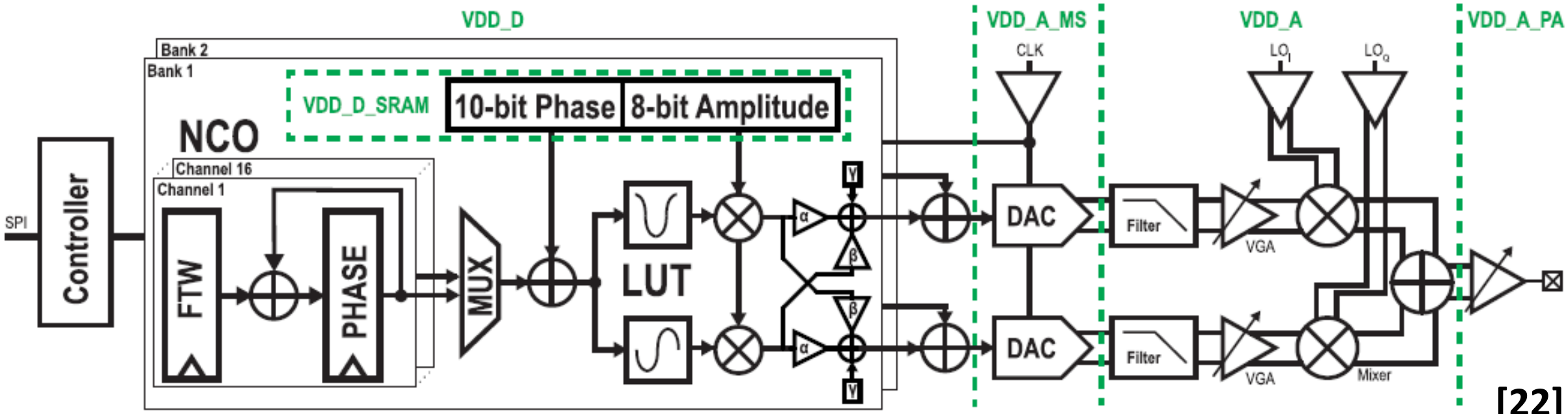




[28]

RF Waveform Generation

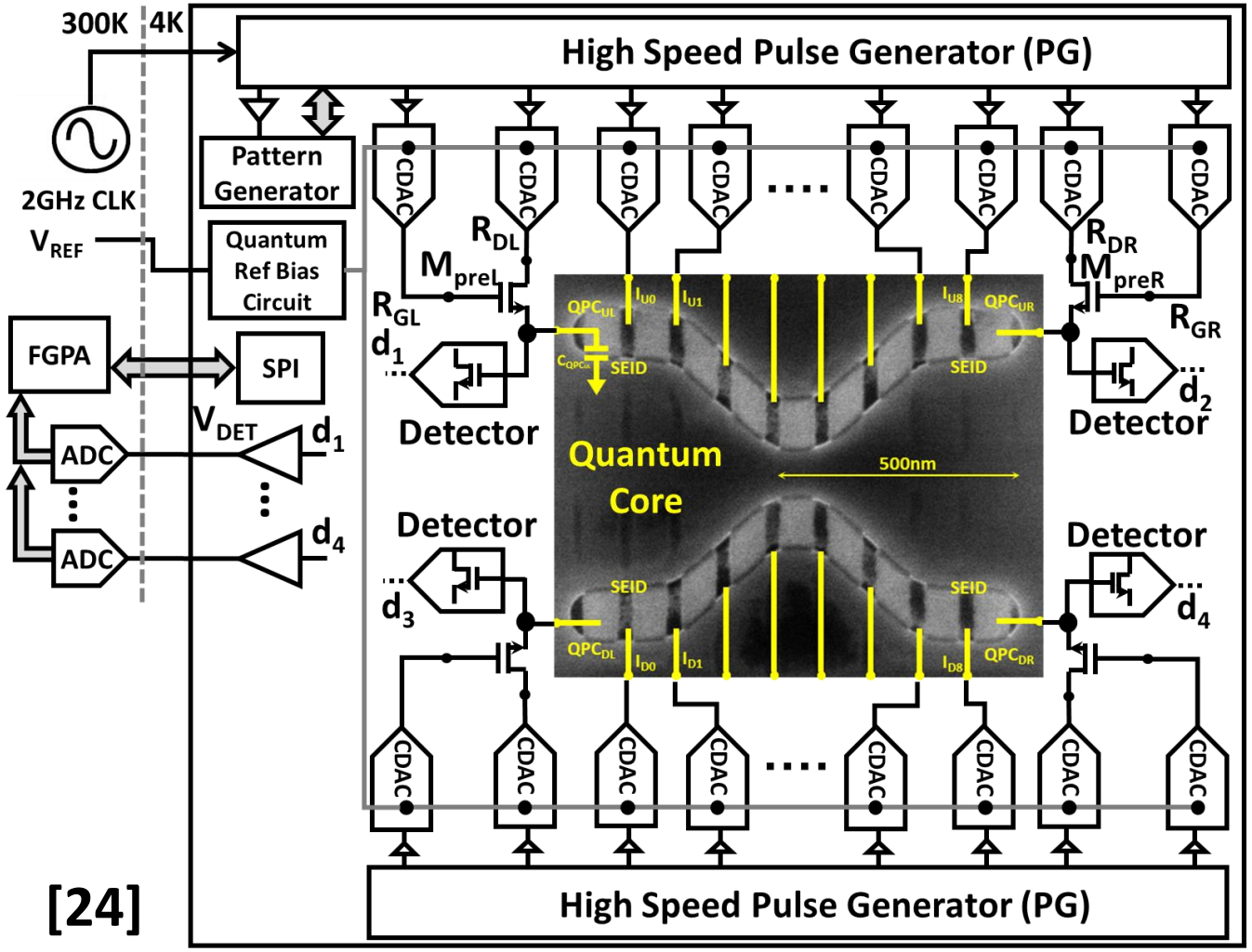
- MIMO transmitter design
- Includes DPLL, Baseband DACs, VGA, Mixer, Power Amplifier



[22]

Quantum Control & Readout SoC

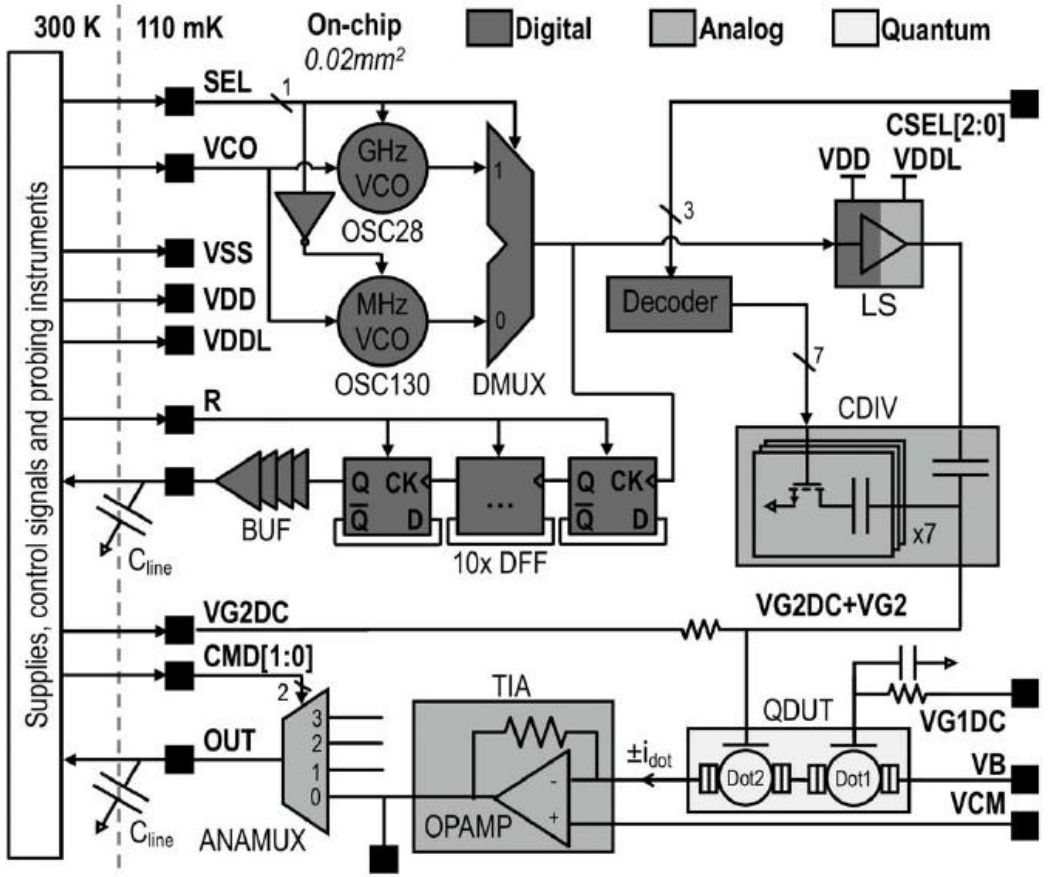
- Fully integrated Quantum Processor Unit comprising a Quantum Core co-located with control + detection circuitry
  - Qubits: 6 (min); 240 (max)
  - Up-to 32 CDAC injectors
  - Up-to 8 detectors
  - High Speed Pulse Generator with 8 concurrent pulse synthesizing blocks
  - Quantum Reference Bias Circuit generates all biases for the quantum structure from a single input reference
  - Pattern Generator as command-and-control for all electronics in the QPU



[24]

Quantum Control & Readout SoC

- Monolithically integrated double quantum dot with control + detection circuitry
  - Capacitive DAC for pulsing
  - TIA detector for current sensing
  - Pulse generation digital logic



[19]

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