IC Design Tutorial

HEPIC Summer Week

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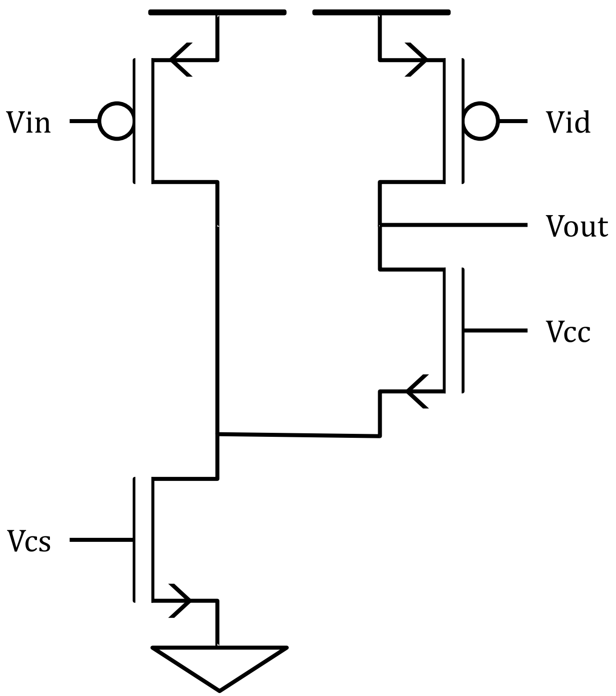
2025

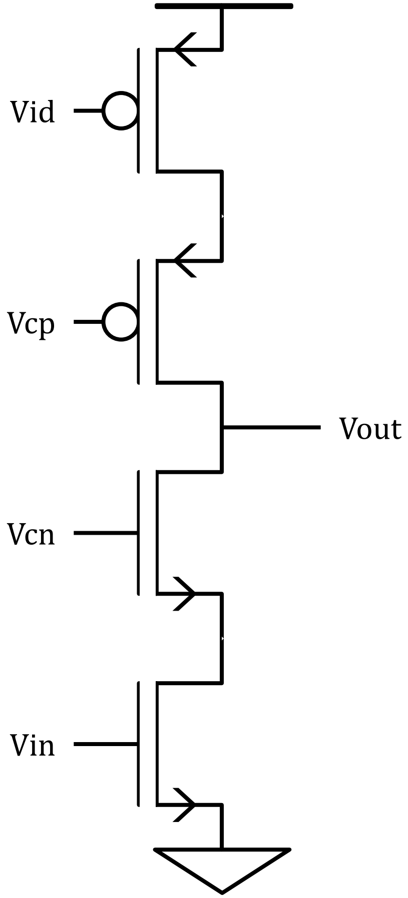
SLAC NATIONAL ACCELERATOR LABORATORY

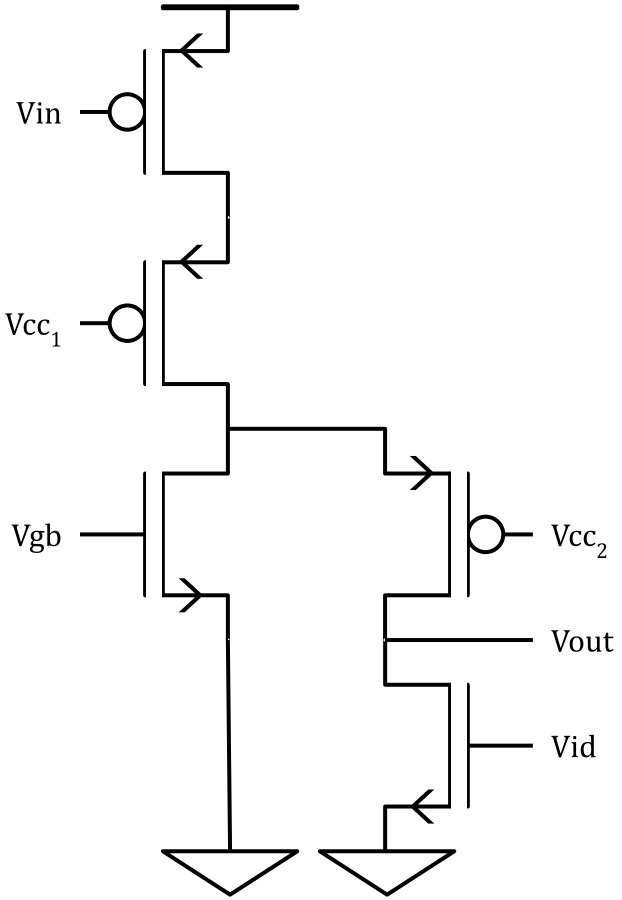
Stanford University | U.S. DEPARTMENT OF ENERGY

The End Goal

Look at these circuits and intuitively understand what they do

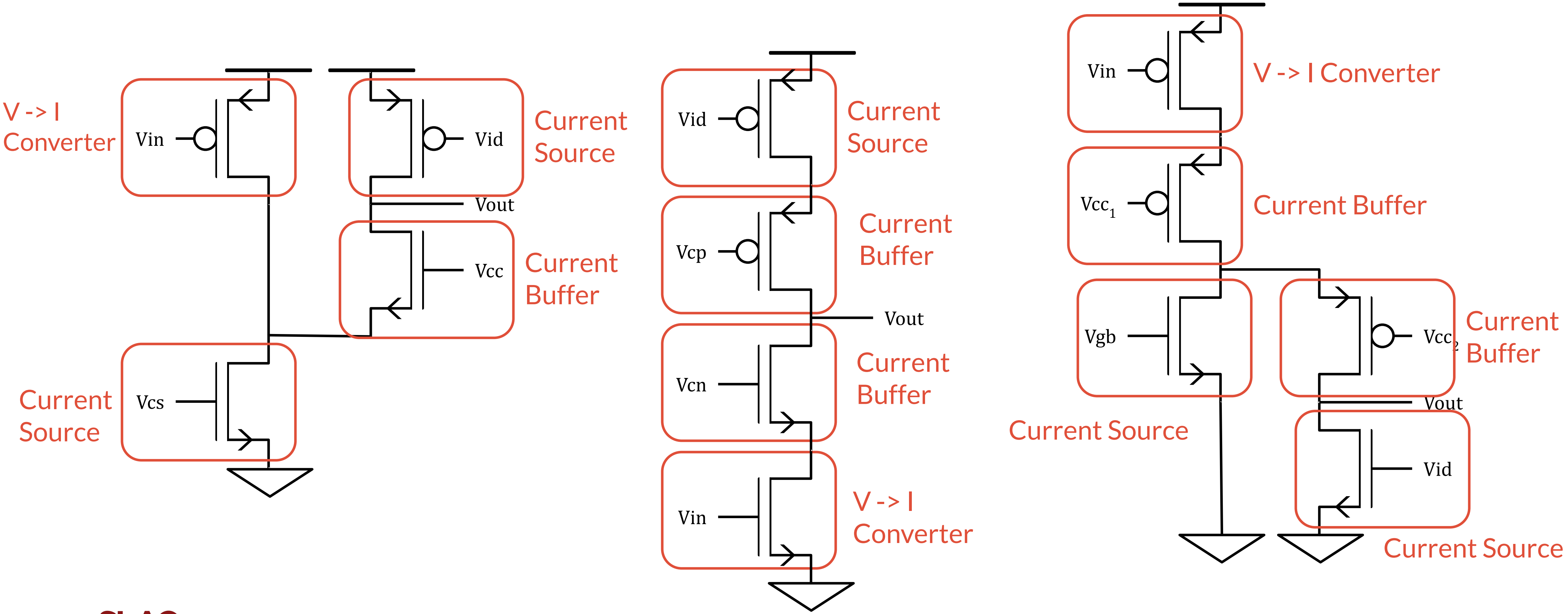






The Approach

Break circuits down into modular blocks



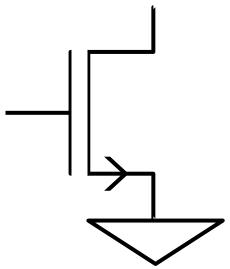
The Steps

1. Small Signal DC Analysis
    a. The three types of building blocks
        i. I → V and V → Converters
        ii. Impedance Transformers
    b. How to quickly solve any circuit with no feedback loops
    c. Designing circuits with building blocks
2. DC Biasing And Sizing Transistors
    a. Device equations and gm/Id
    b. How to size transistors to get a desired gm
    c. Current sources
3. AC Analysis And Feedback
    a. Charge-sensitive amplifiers and diode readouts
    b. The open-loop intrinsic gain stage
    c. Adding capacitive feedback
    d. Working with multi-stage amplifiers

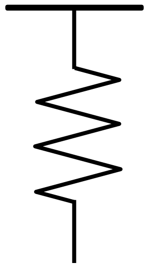
Small Signal DC Analysis

Three types of building blocks

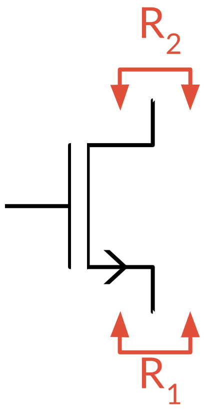
The Three Types of Building Blocks



V → I
Converters

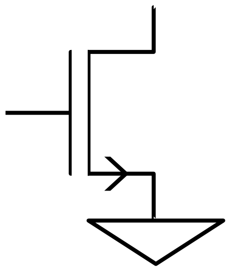


I → V
Converters

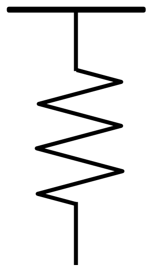


Impedance
Transformers

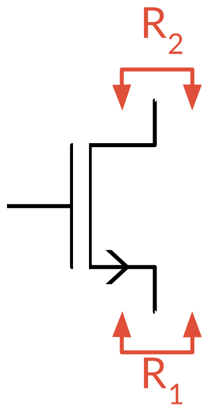
The Three Types of Building Blocks



V → I Converters

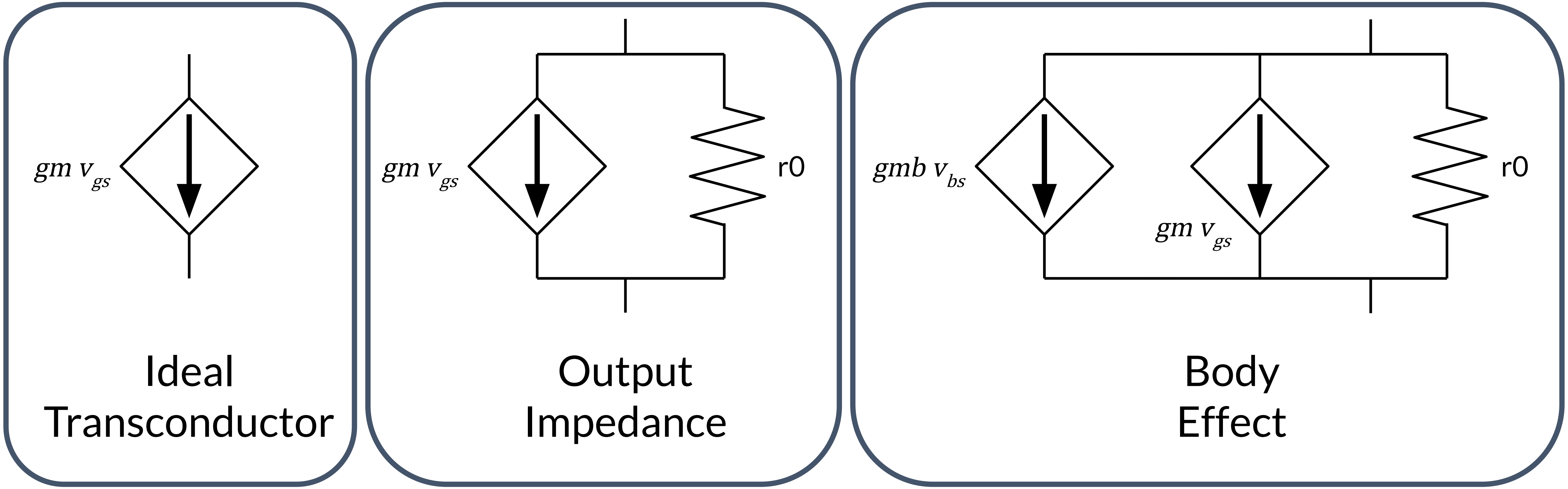


I → V Converters

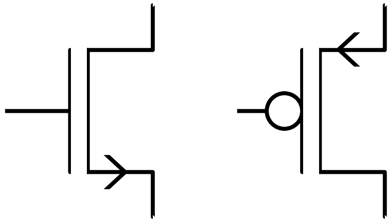


Impedance Transformers

MOSFET Small Signal Models

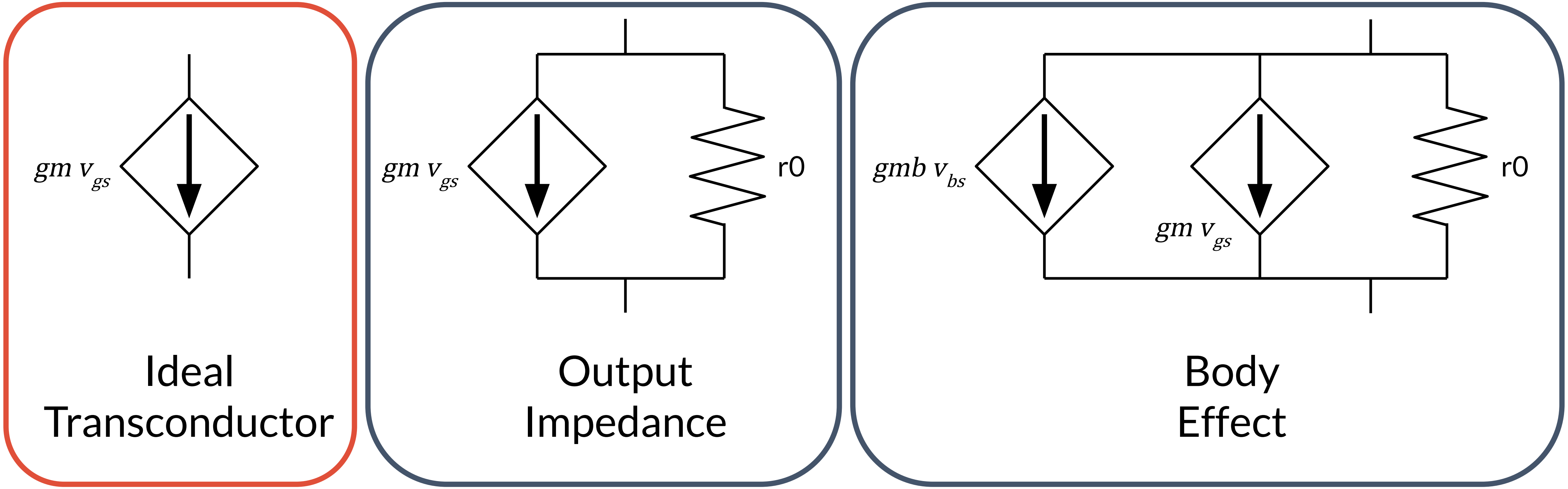


Same model for both:



MOSFET Small Signal Models

We'll start with ideal transconductor



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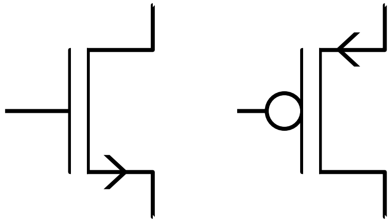
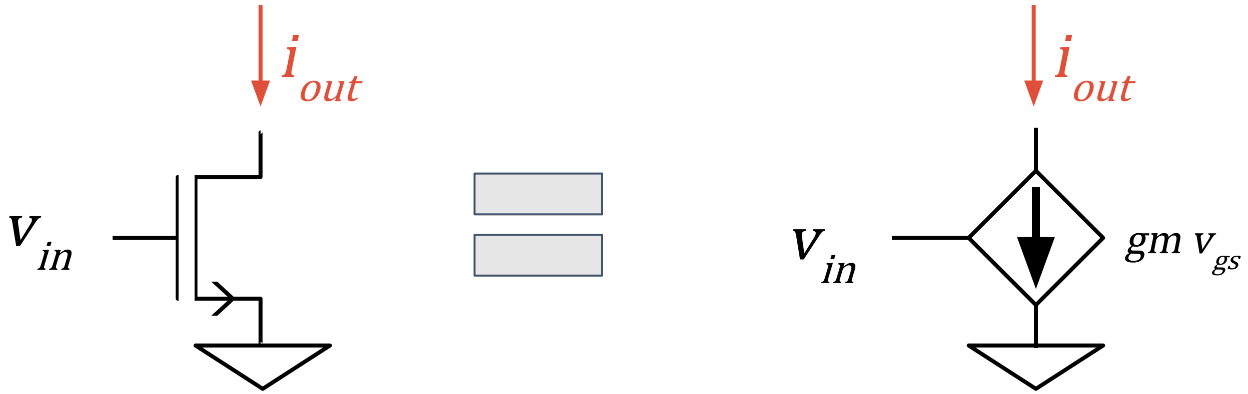


V → I Converters

A MOSFET in the common-source configuration is used as a voltage to curren converter.



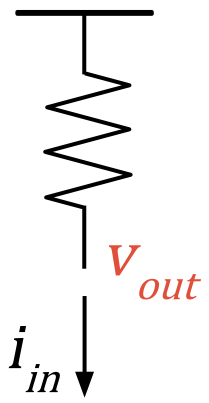
$$i_{out} = g_m \left(v_{gate} - v_{source}\right)$$

$$i_{out} = g_m \left(v_{in} - 0\right)$$

$$i_{out} = g_m v_{in}$$

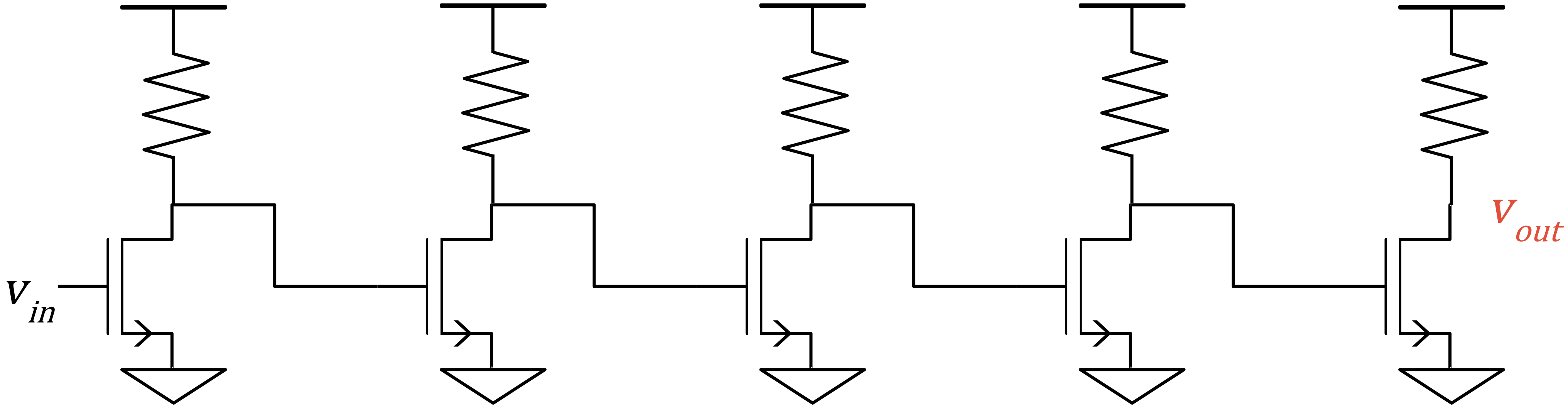
I → V Converters

A resistor is commonly used when we need to convert a current back into a voltage.



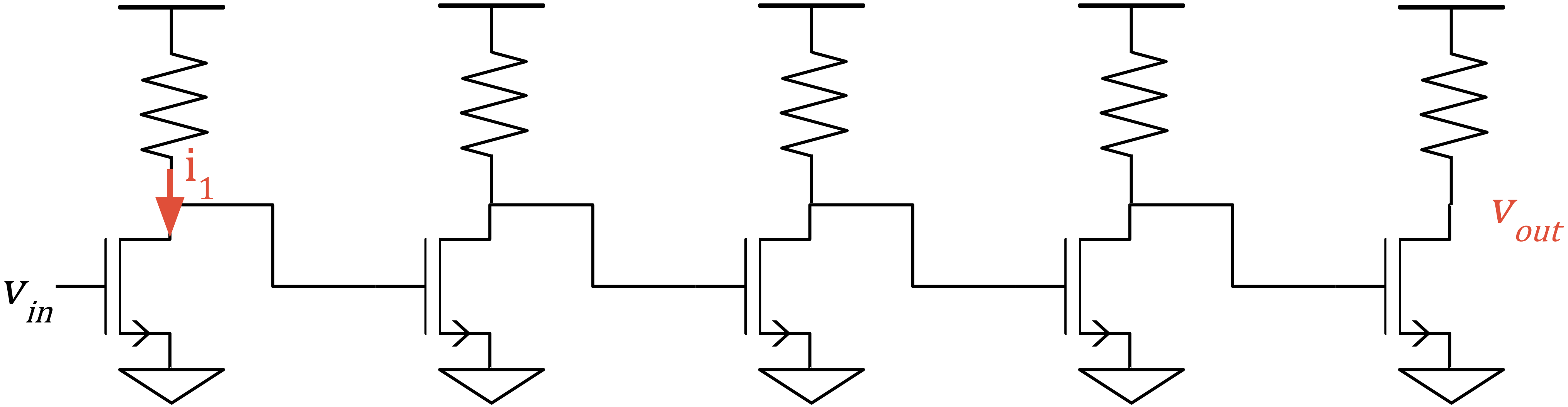
$$v_{out} = i_{in} R$$

Chaining stages together



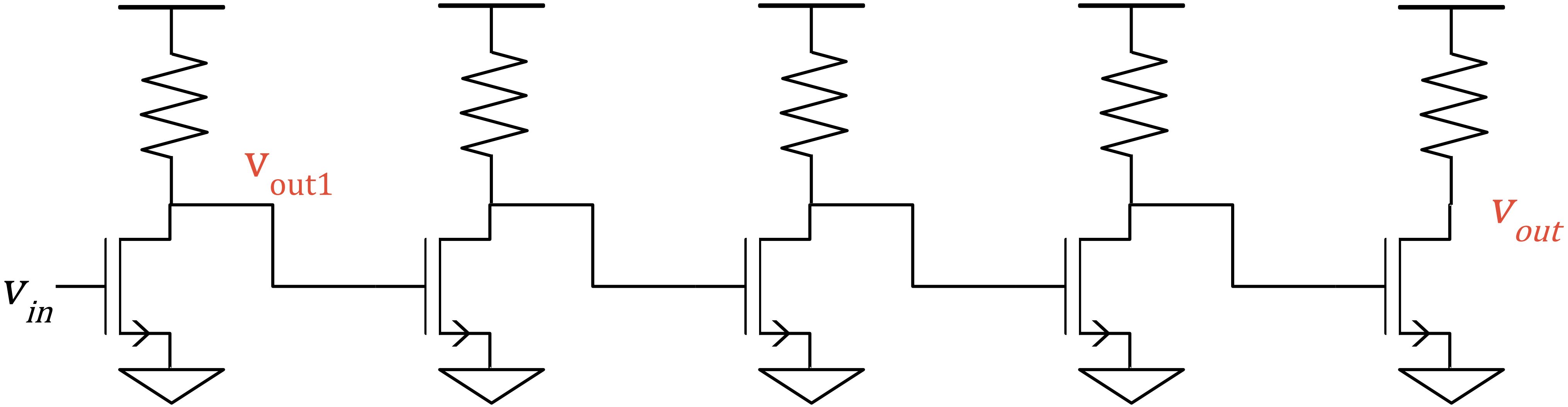
Chaining stages together

$$i_1 = g_{mn1} V_{in}$$



Chaining stages together

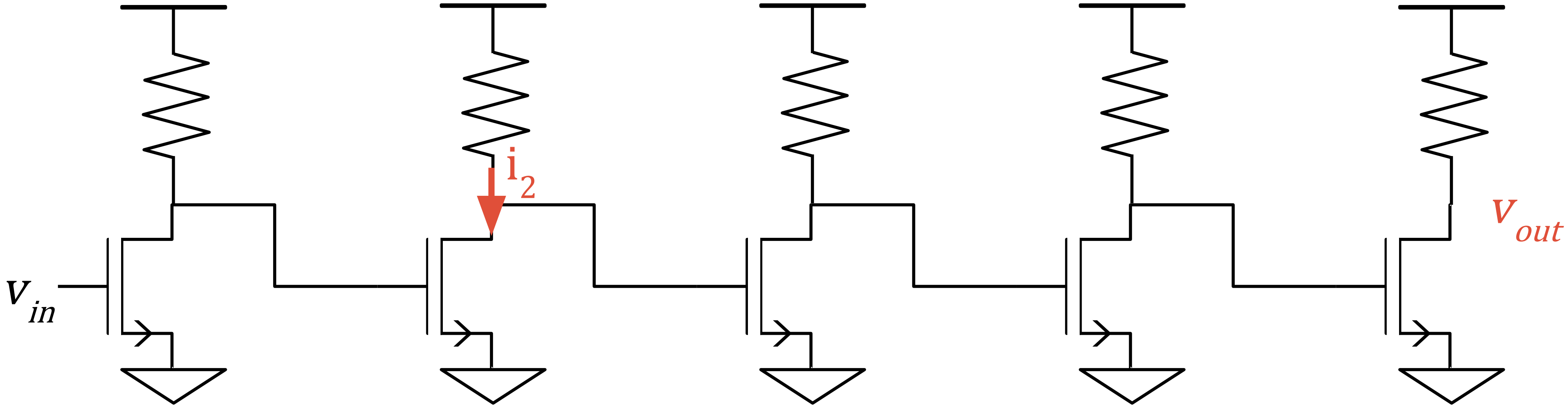
$$i_1 = g_{mn1} V_{in}$$



$$v_{out1} = i_1 R_1 = g_{m1} R_1 v_{in}$$

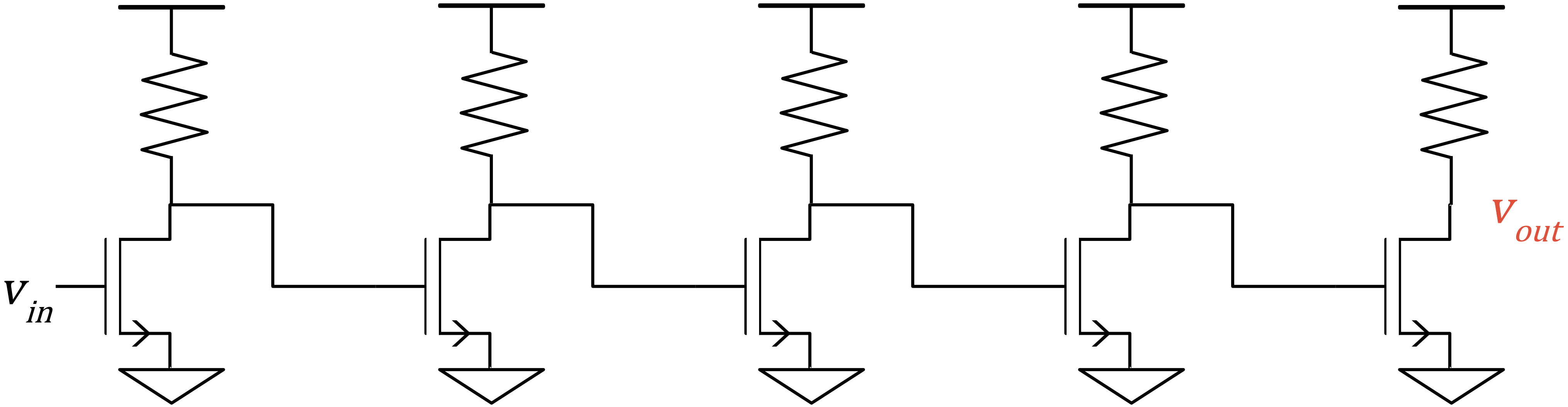
Chaining stages together

$$i_1 = g_{mn1} V_{in} \quad i_2 = g_{m2} v_{out1} = g_{m1} R_1 g_{m2} v_{in}$$



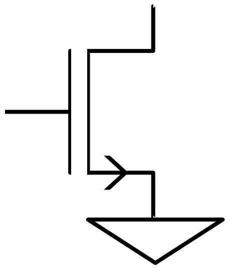
$$v_{out1} = i_1 R_1 = g_{m1} R_1 v_{in}$$

Chaining stages together

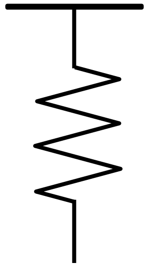


$$\frac{v_{out}}{v_{in}} = \prod_{i=1}^{N} g_{mi} R_i$$

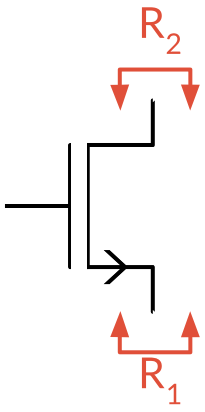
The Three Types of Building Blocks



V → I
Converters

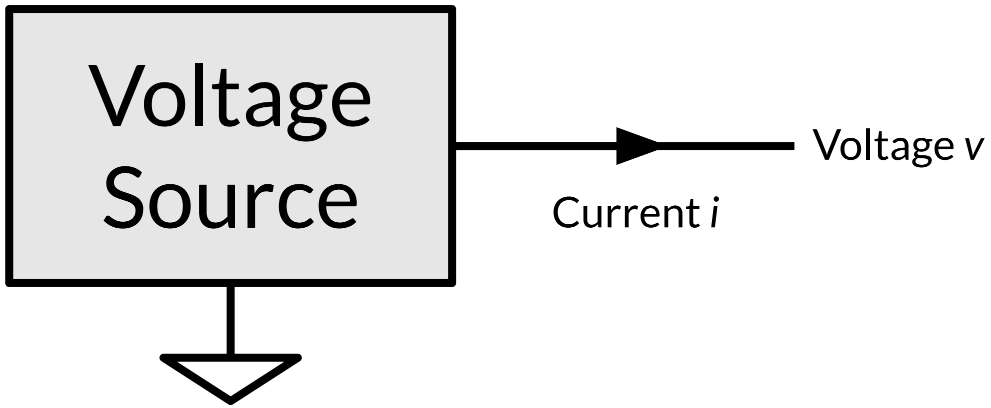


I → V
Converters



Impedance
Transformers

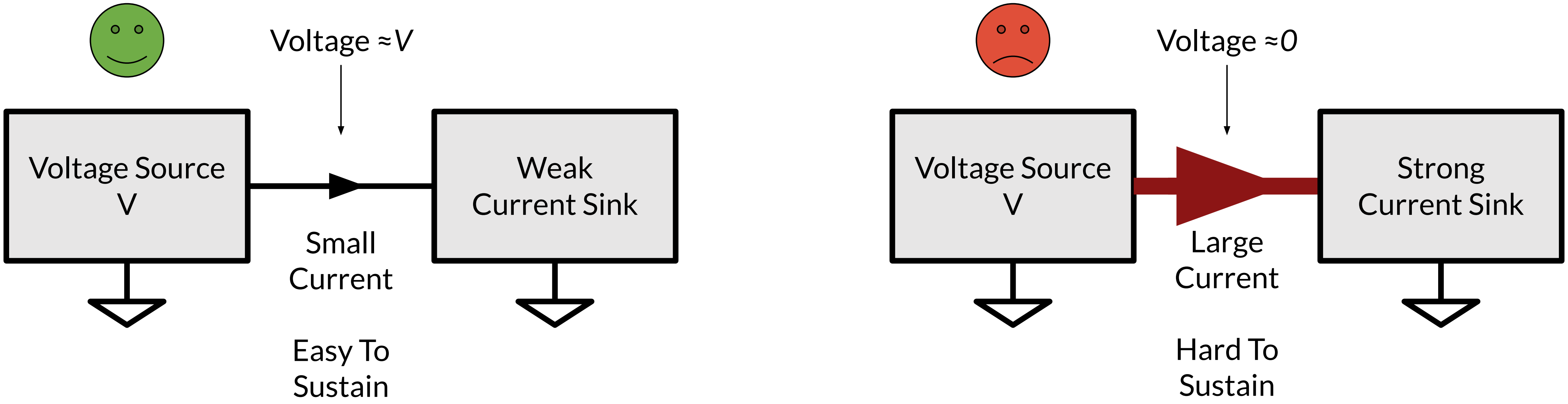
Consider a generic source of voltage



$$v = v(i) = v_0 + iR_{eq}$$

It takes "effort" to emit a current

The more current is taken from the voltage source, the more it struggles to maintain its voltage



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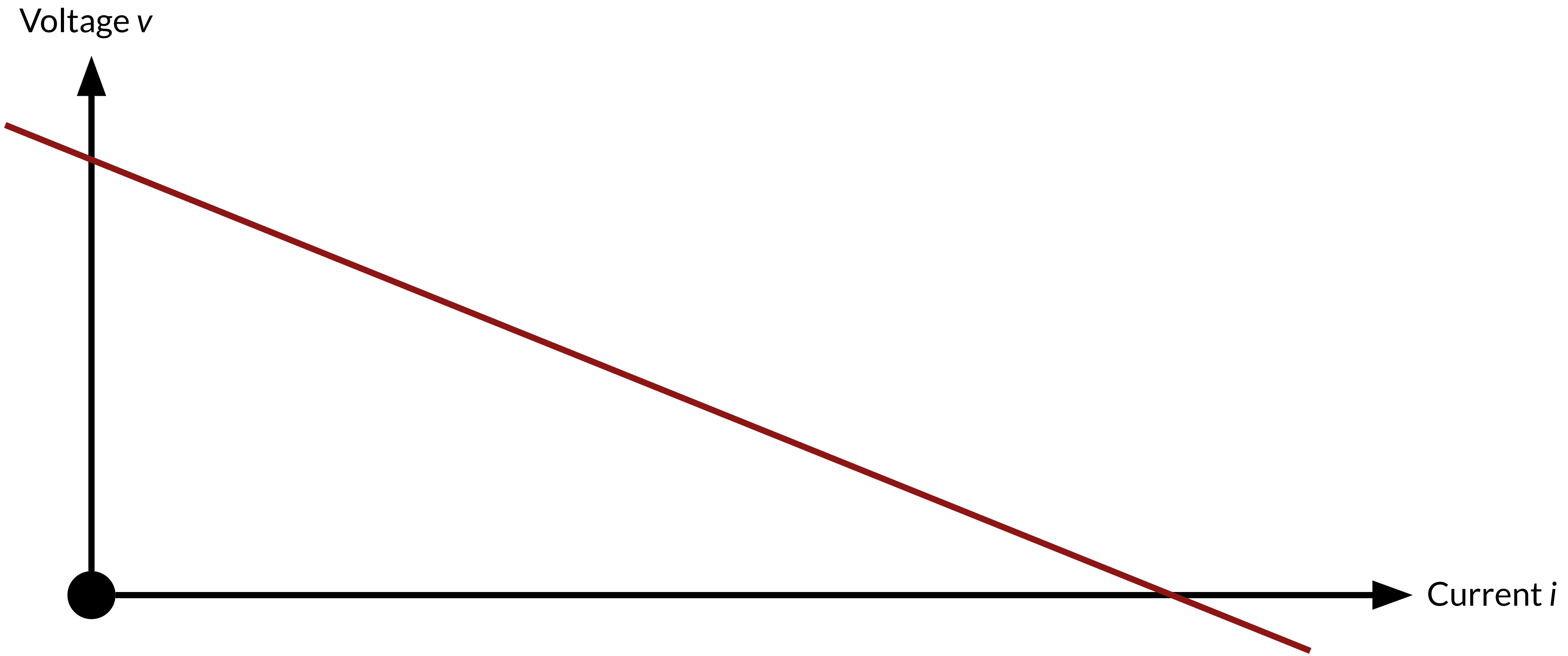
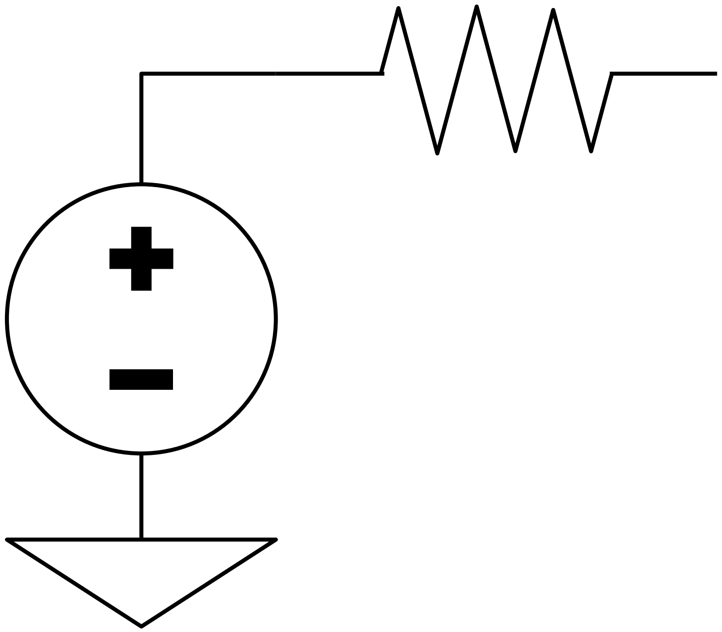


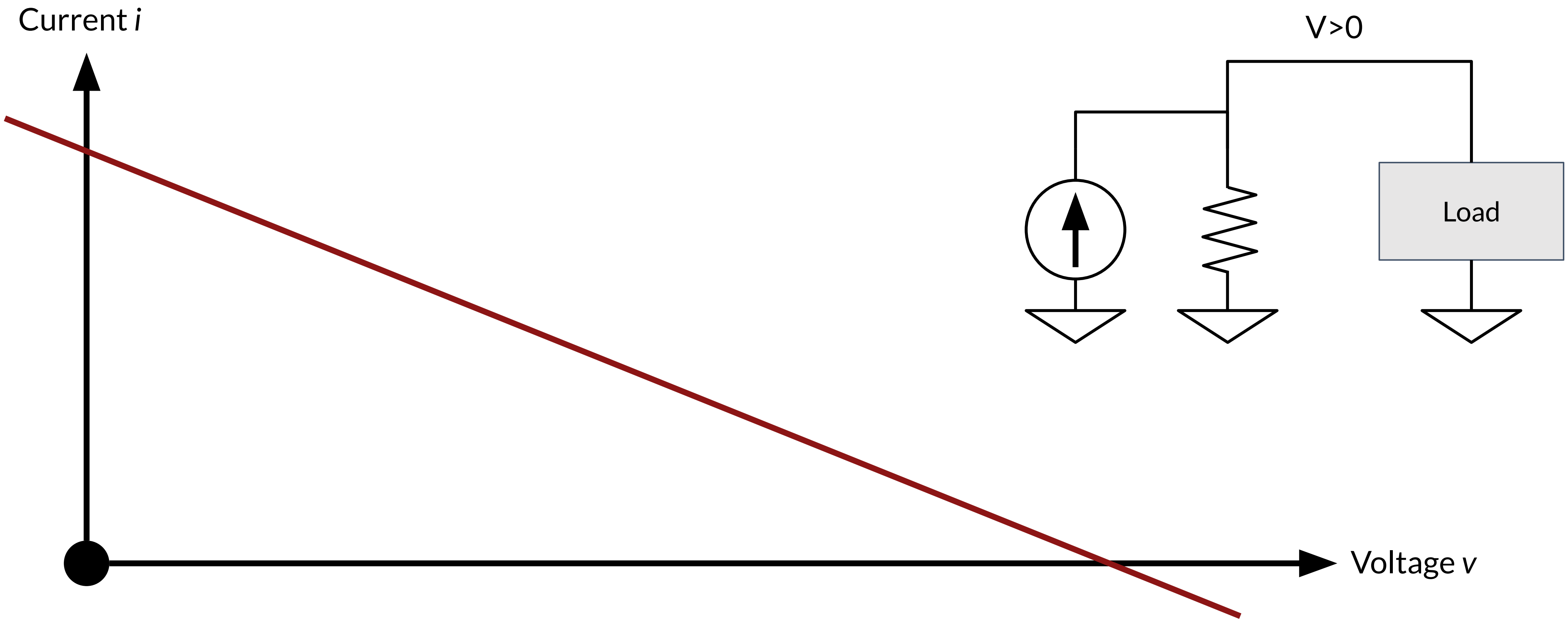
So a voltage source has some impedance

Once too much current is drawn from the voltage source, the resistor cancels it out



Similarly, it takes "effort" to maintain a voltage

The more voltage is needed, the more the source struggles to maintain it. Once too much voltage is applied, the current is controlled by the resistor, not the current source.

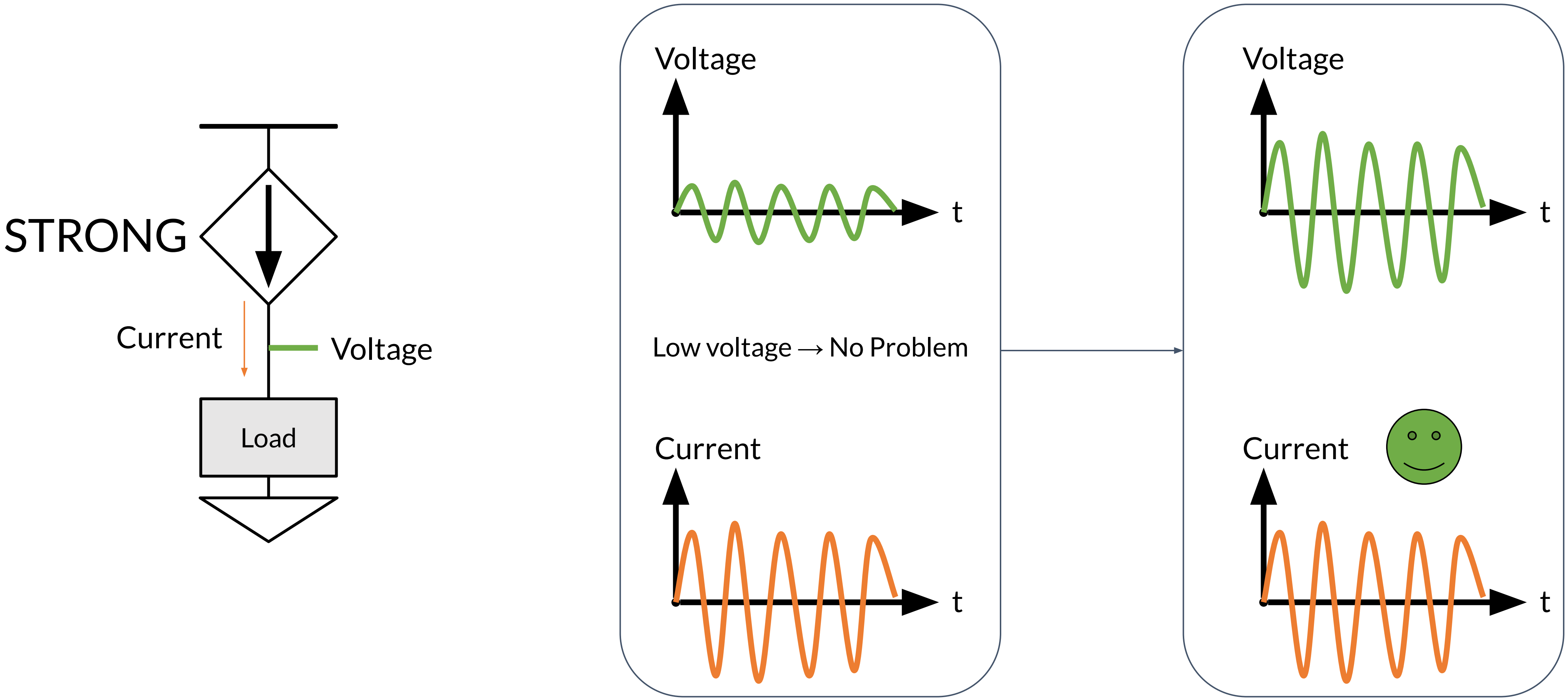


Sources of voltage and current are never ideal

Can we improve the “strength” of a current source?

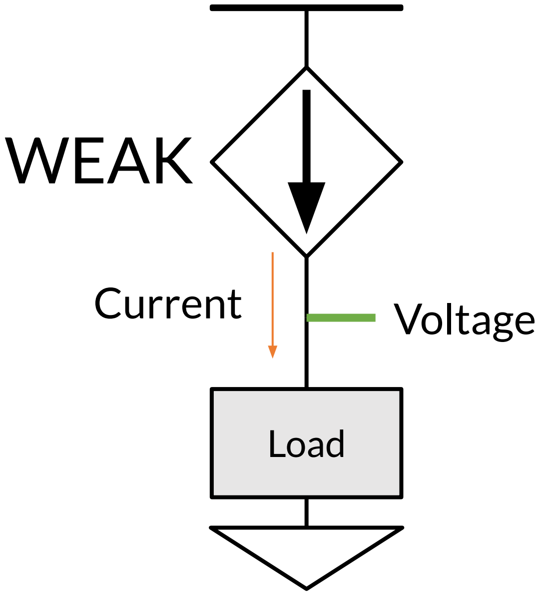
What is a “strong” source of current?

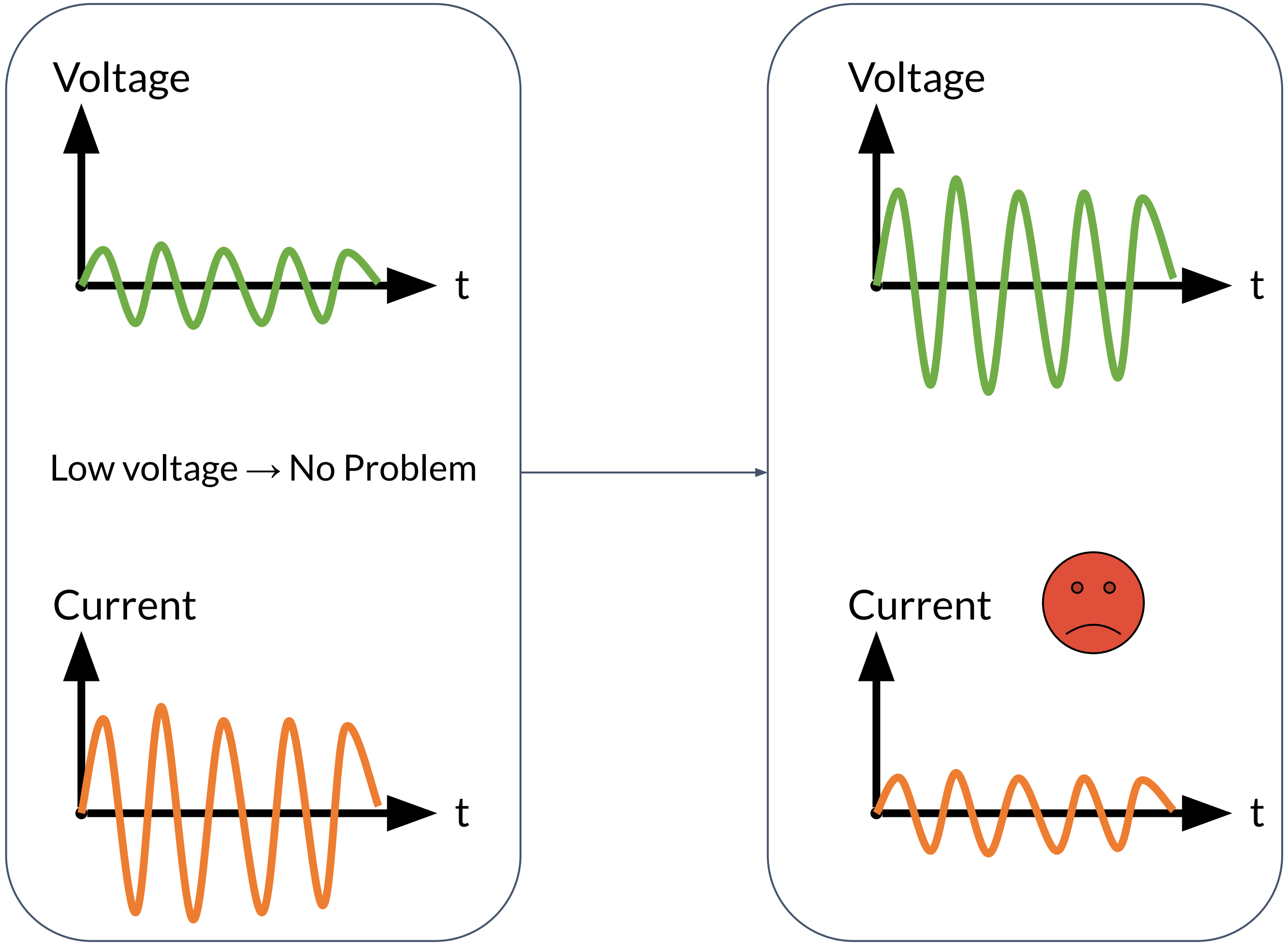
A strong source maintains a constant current at any voltage



What is a "strong" source of current?

A weak source is unable to maintain its current at high voltages

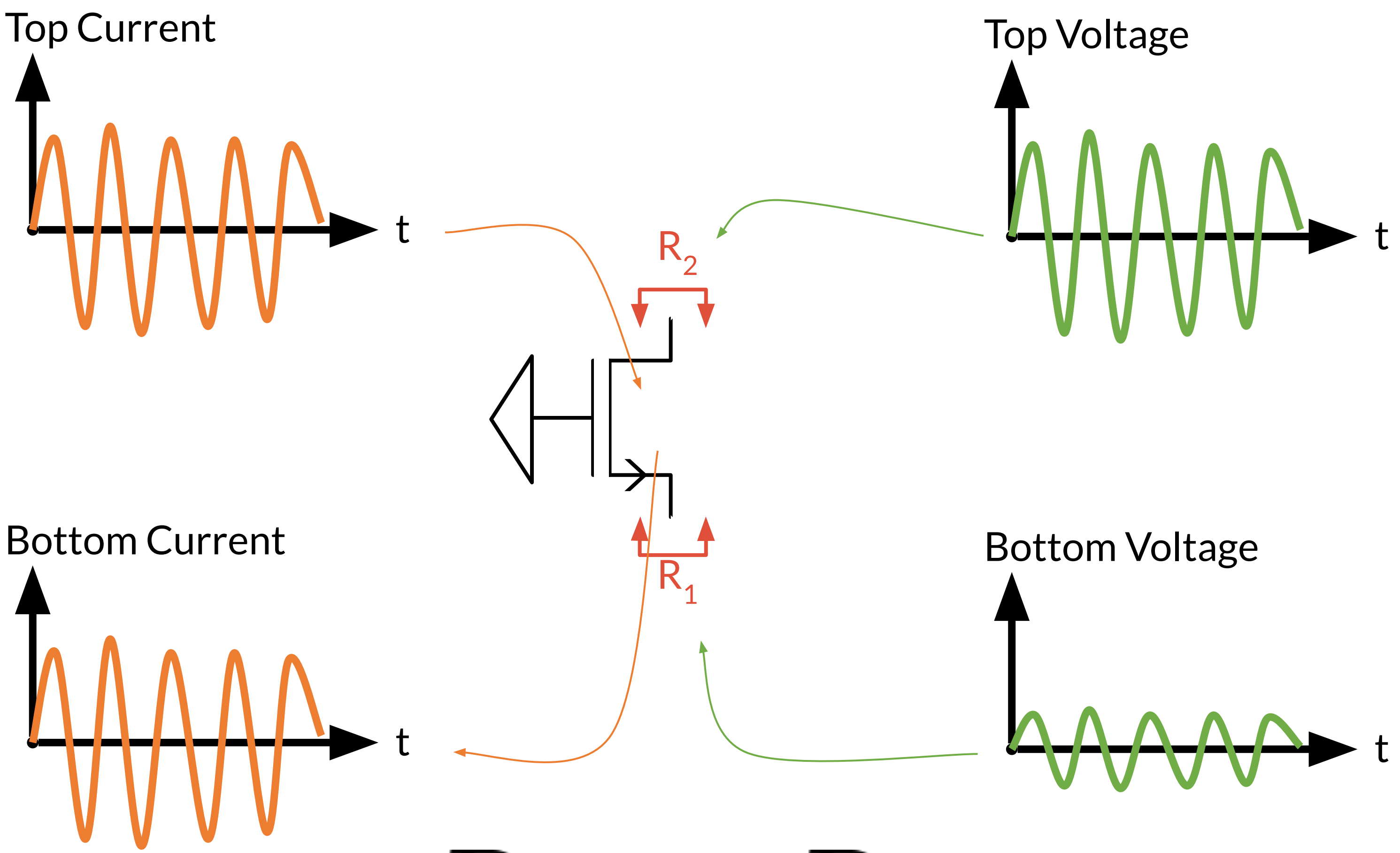




The common gate stage provides "isolation"

The drain of the transistor can freely "wiggle" while the source remains at a fixed voltage.

The current across the common gate stage is constant.



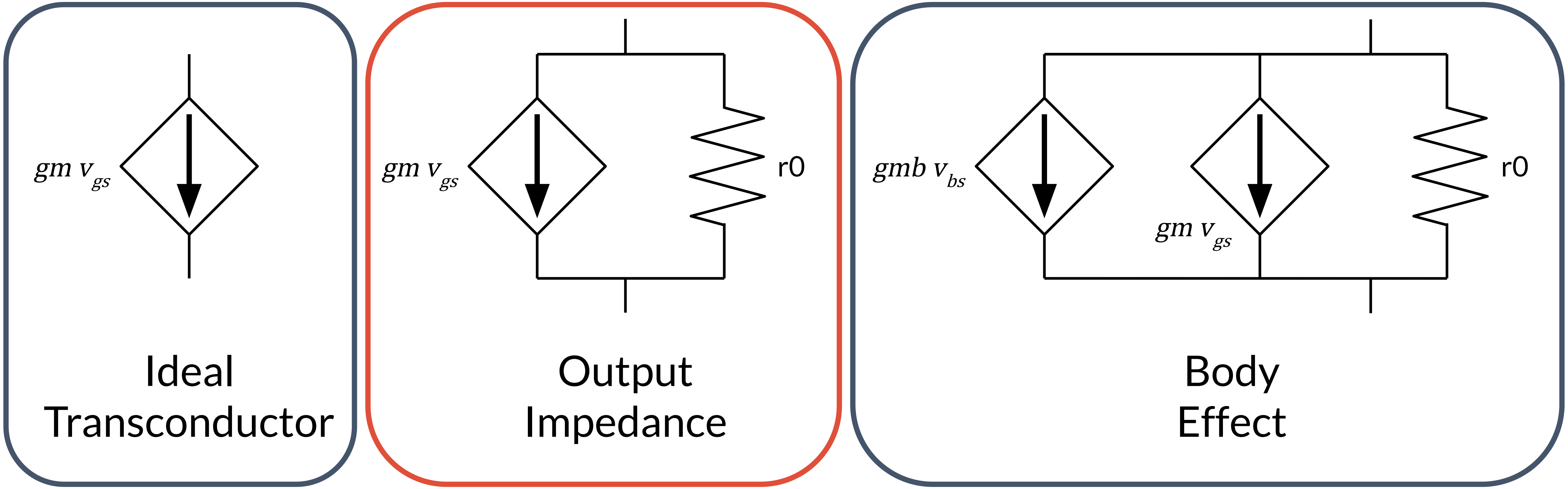
$$R_2 \gg R_1$$

Small Signal DC Analysis

How to quickly solve circuit problems without feedback

MOSFET Small Signal Models

We’ll start with ideal transconductor



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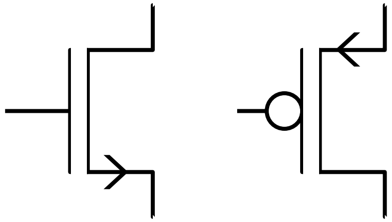
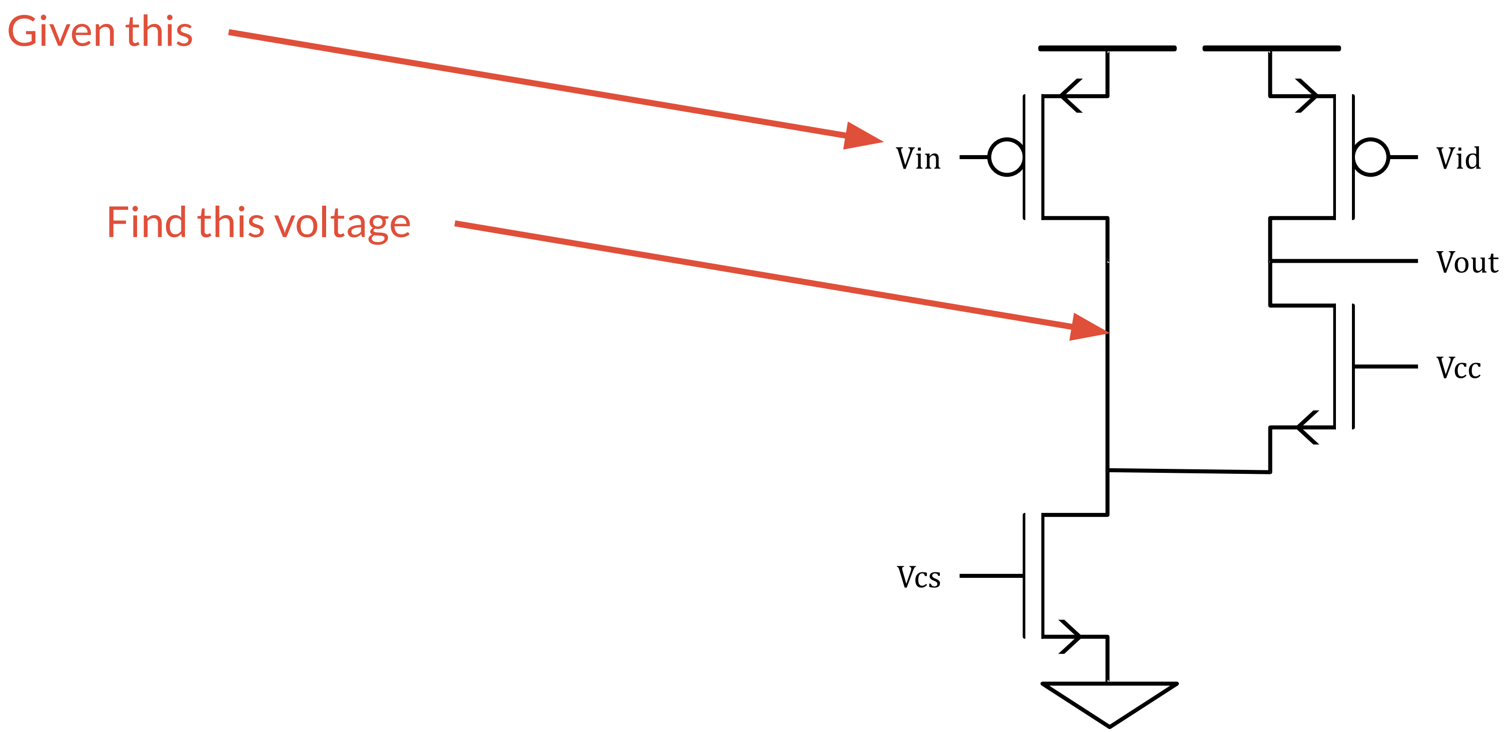
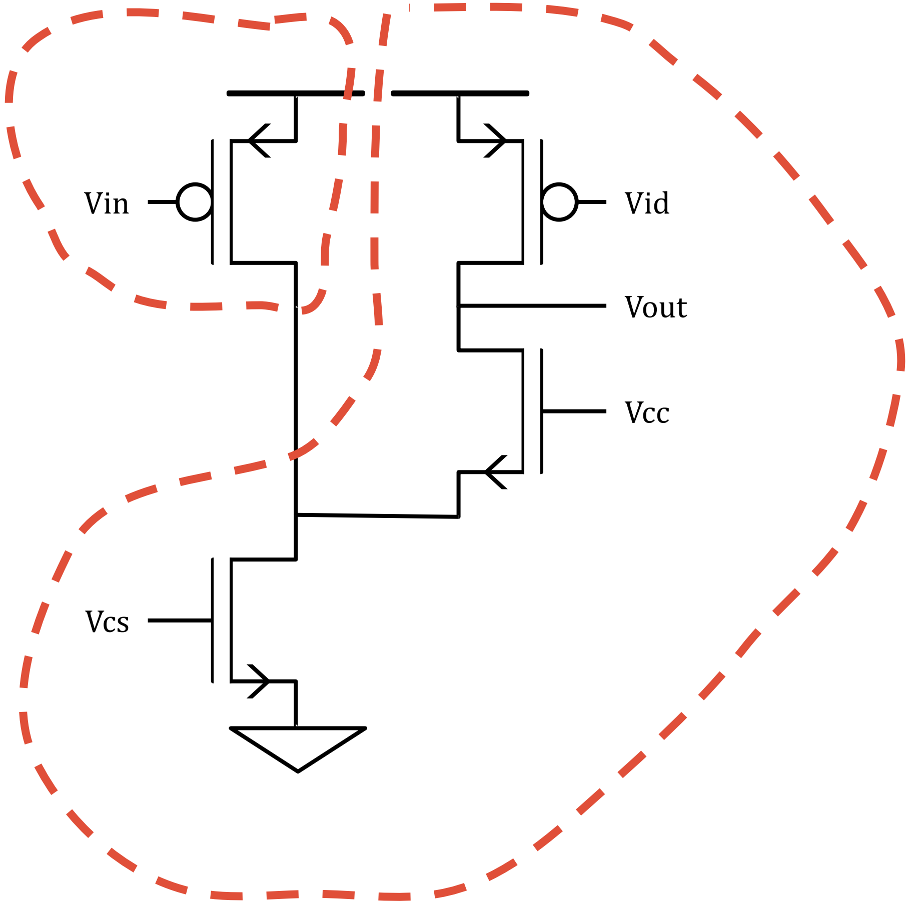


What can we do?



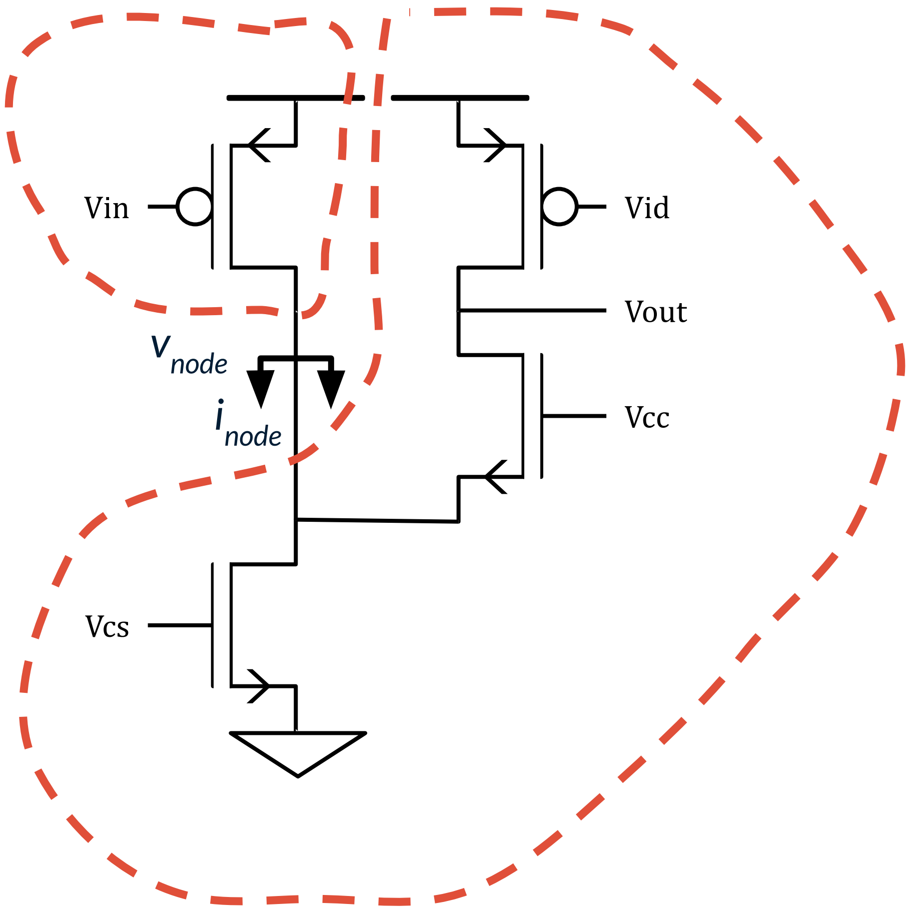
What can we do?

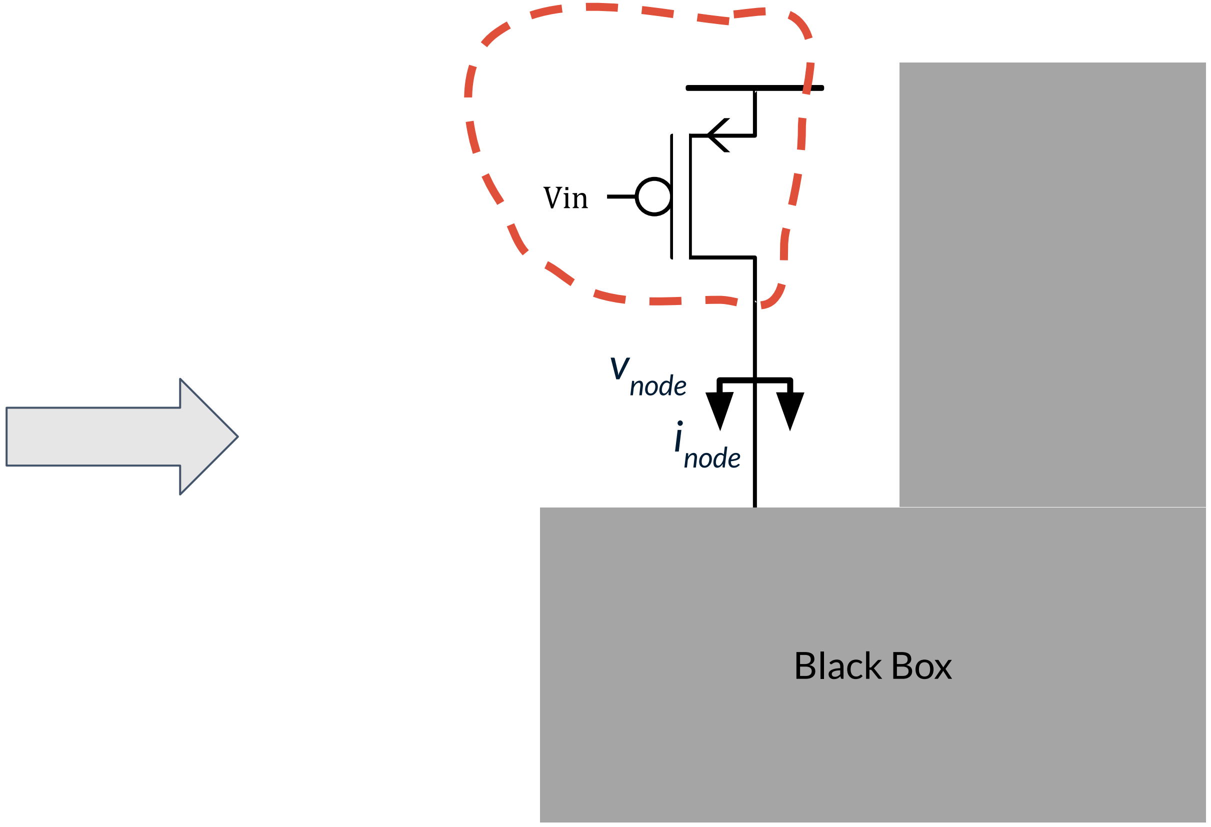
These two halves of the circuit only connect in one point!



What can we do?

Let's split the circuit into two





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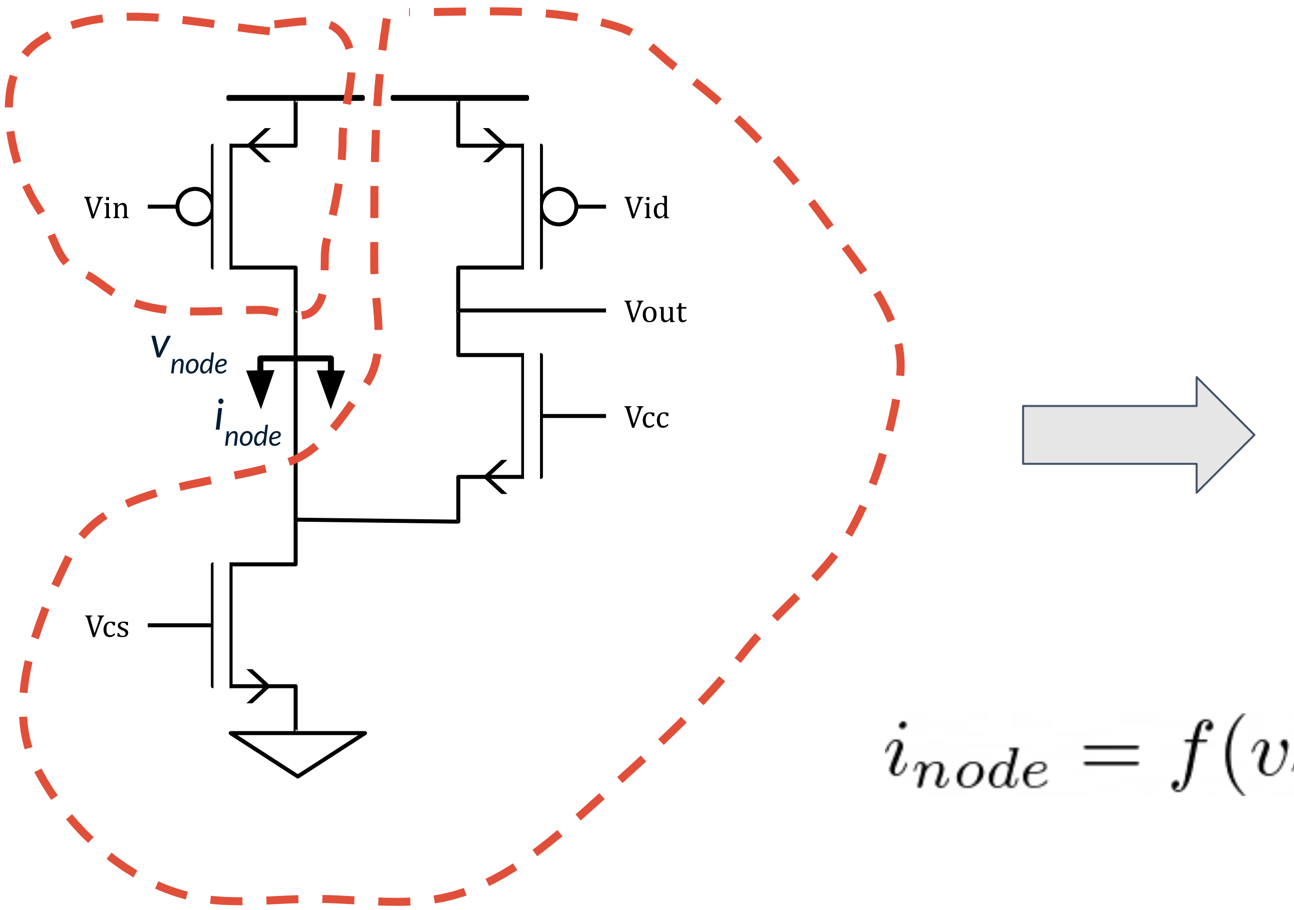
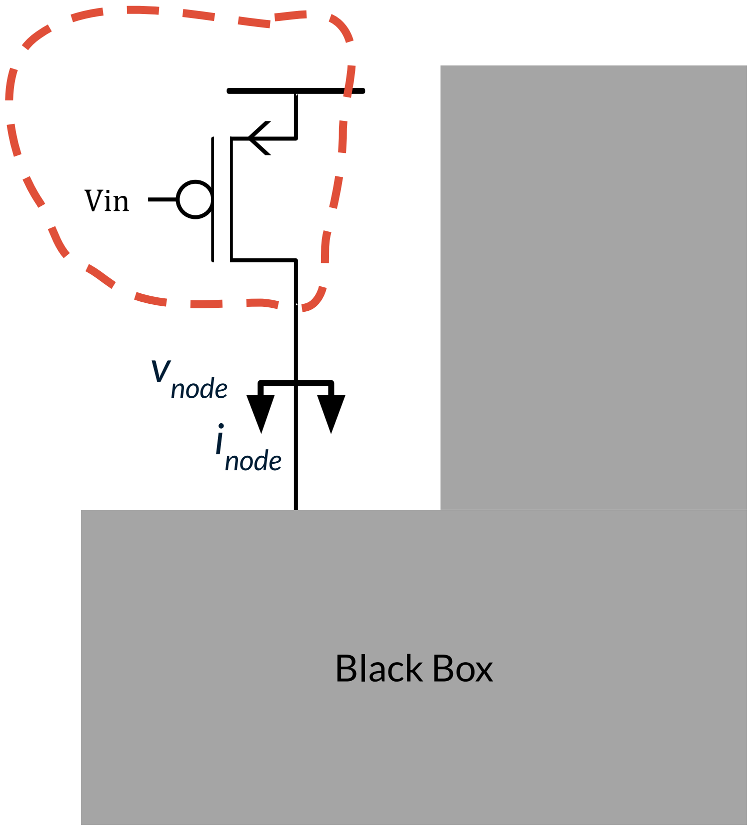


$$i_{node} = f(v_{node})$$



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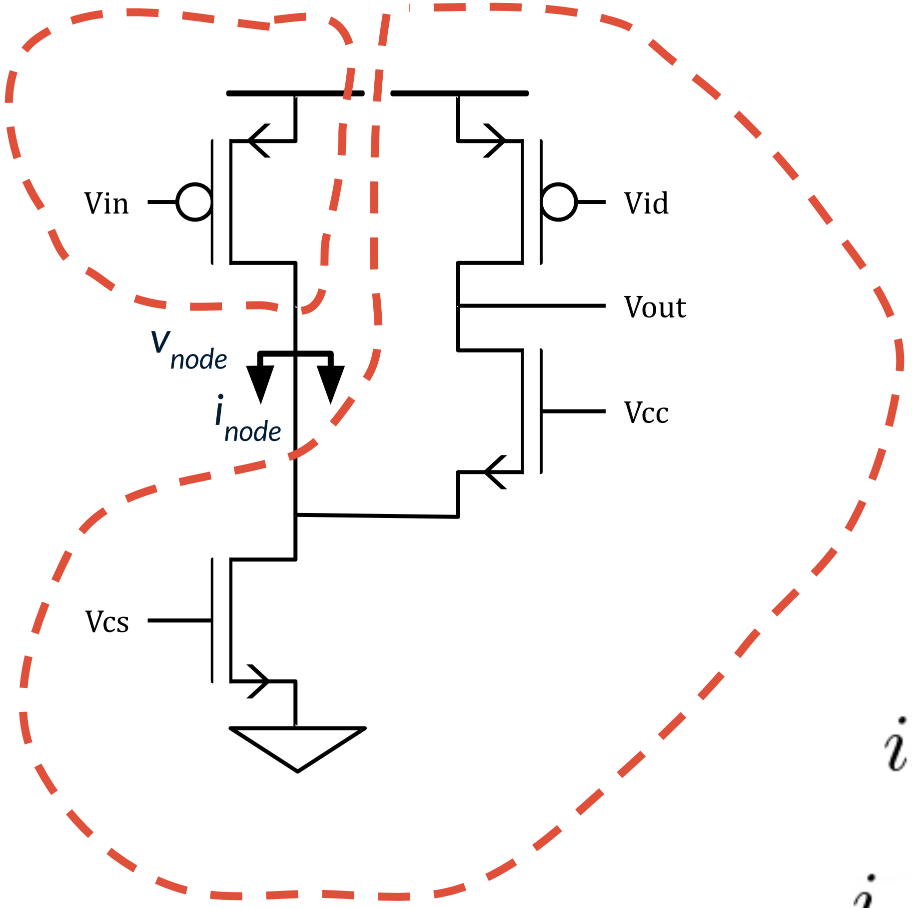
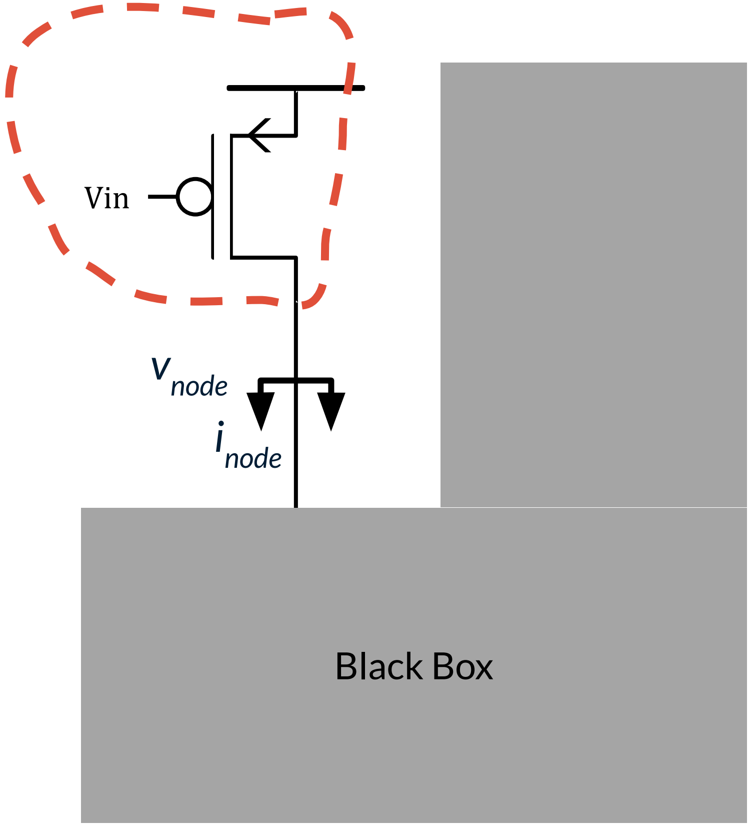


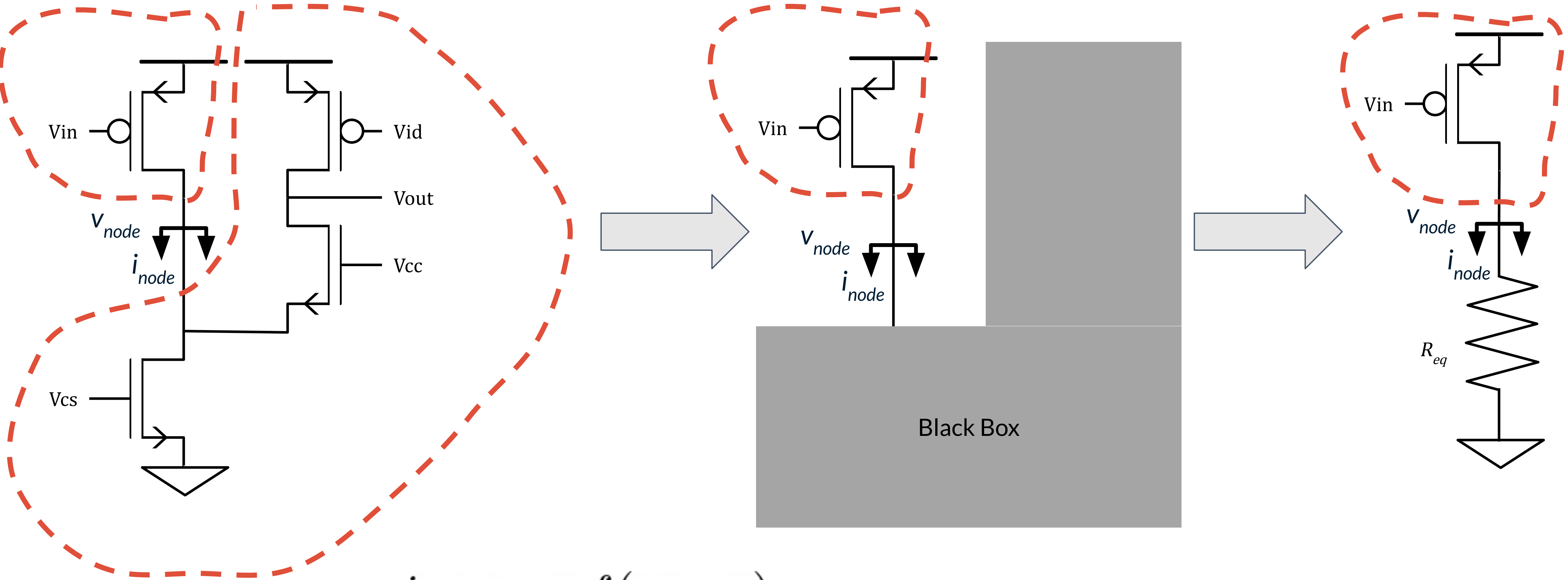


$$i_{node} = f(v_{node})$$

$$i_{node} = v_{node}/R_{eq}$$

What can we do?

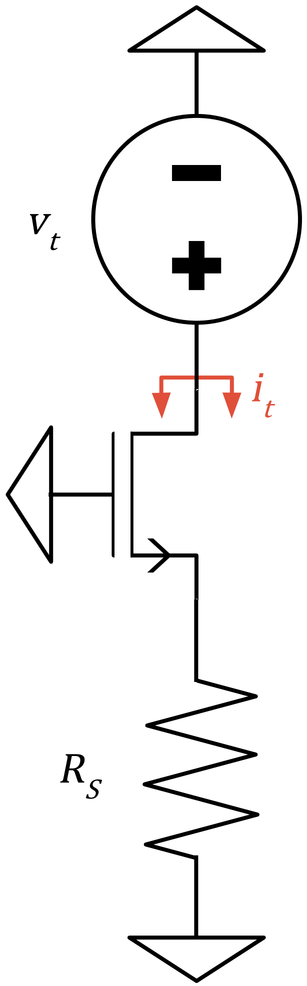
Let's split the circuit into two

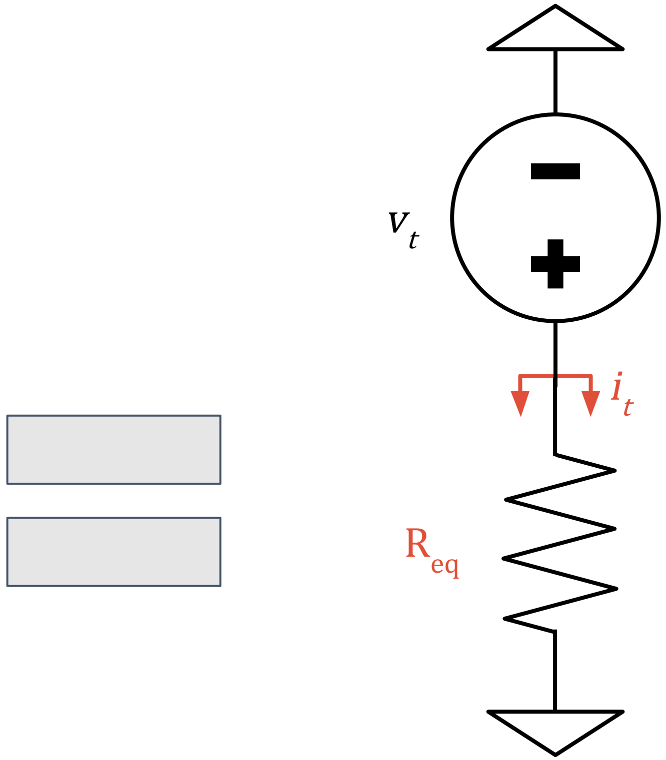


$$i_{node} = f(v_{node})$$
$$i_{node} = v_{node}/R_{eq}$$

SLAC

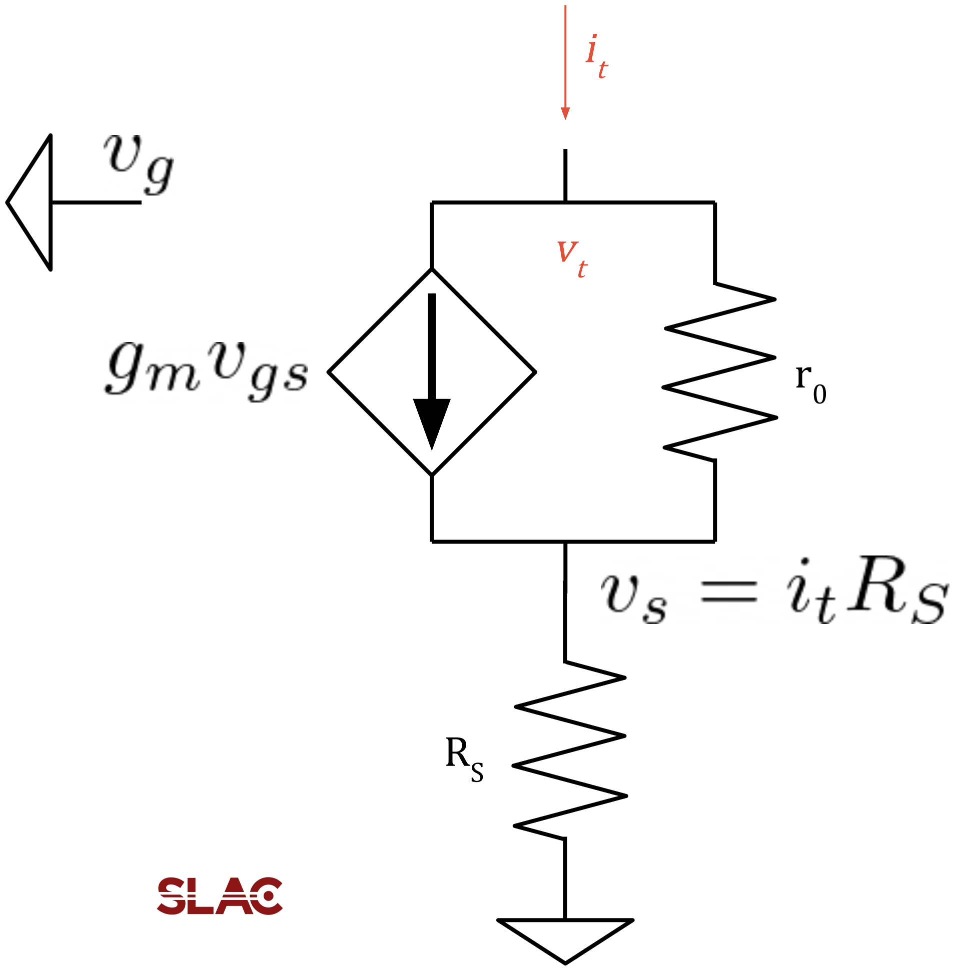
Deriving the drain impedance of a current buffer





$$R_{eq} = \frac{v_t}{i_t}$$

Deriving the drain impedance

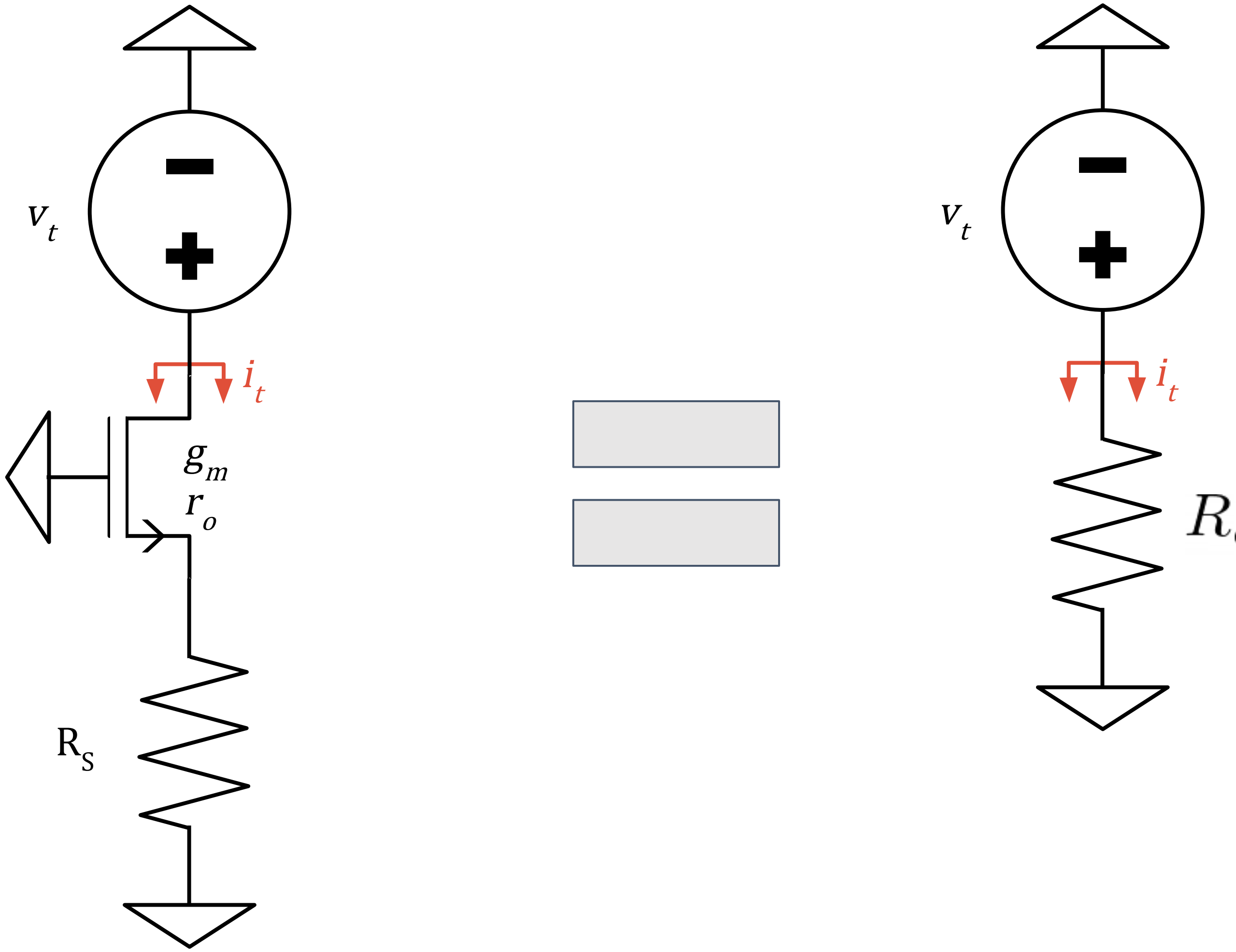


$$i_t = g_m v_{gs} + \frac{v_t - v_s}{r_o}$$

$$i_t = -g_m R_S i_t + \frac{v_t - R_S i_t}{r_o}$$

$$R_{eq} = \frac{v_t}{i_t} = R_s + r_o + g_m r_o R_S$$

The result



$$R_{eq} = R_S + r_o + g_m r_o R_S$$

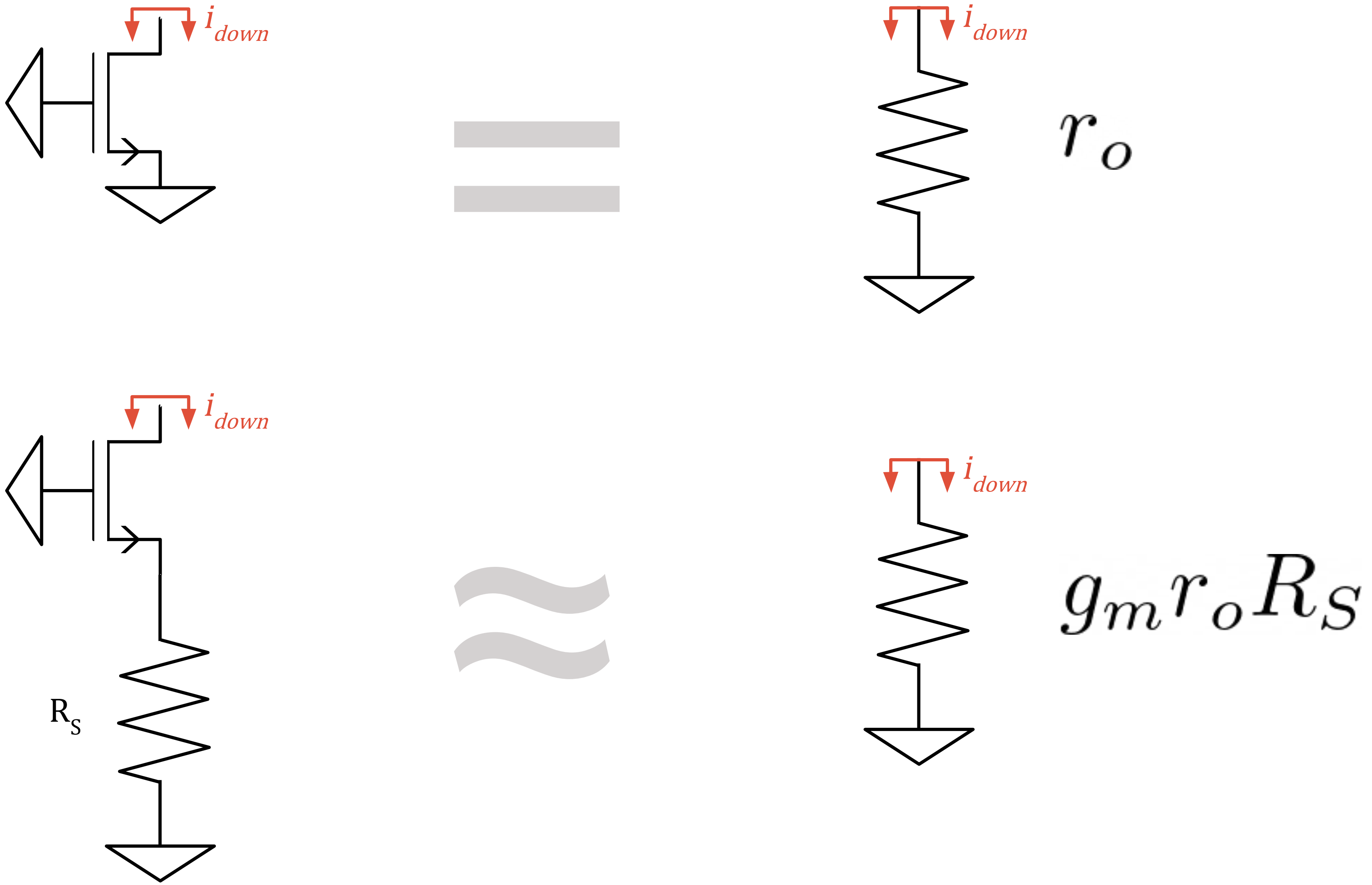
Taking Limits

$$R_{eq} = R_S + r_o + g_m r_o R_S$$

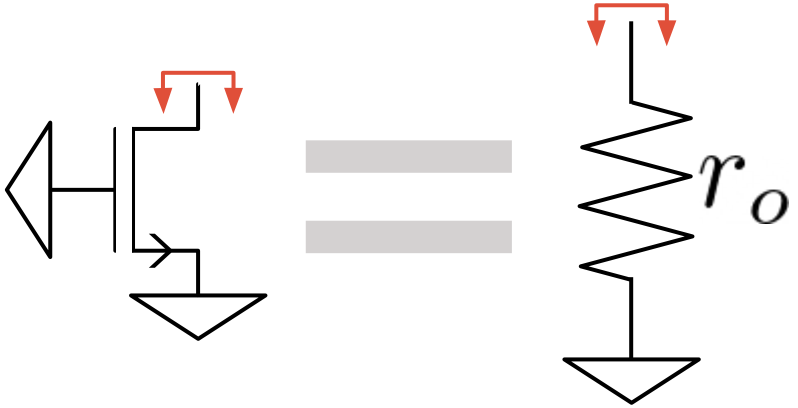
$R_S = 0 \longrightarrow R_{eq} = r_o$

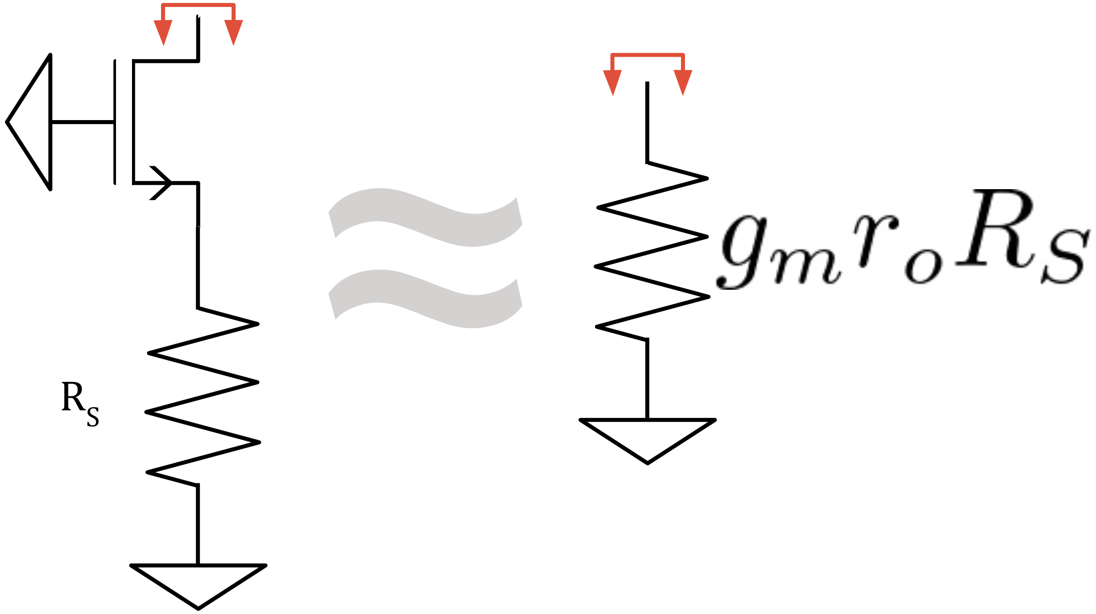
$g_m r_0 \gg 1 \longrightarrow R_{eq} \approx g_m r_o R_S$

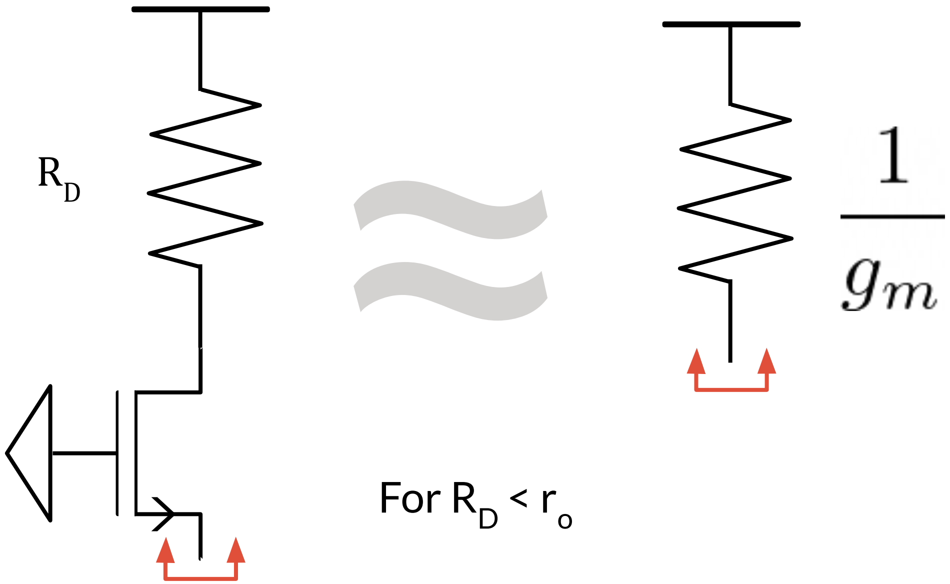
The Result

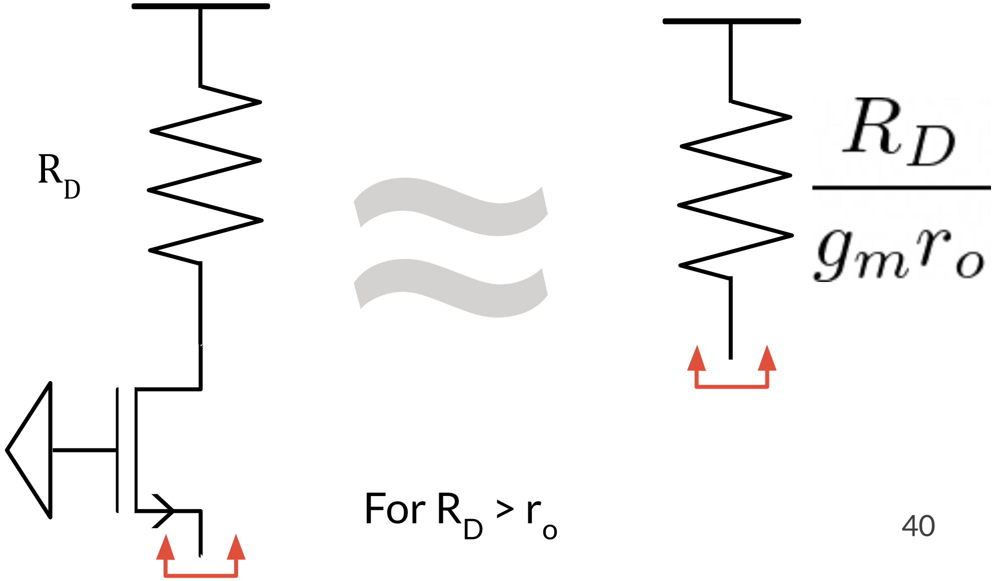


Transistor cheat-sheet (assuming $g_m r_0 \gg 1$)









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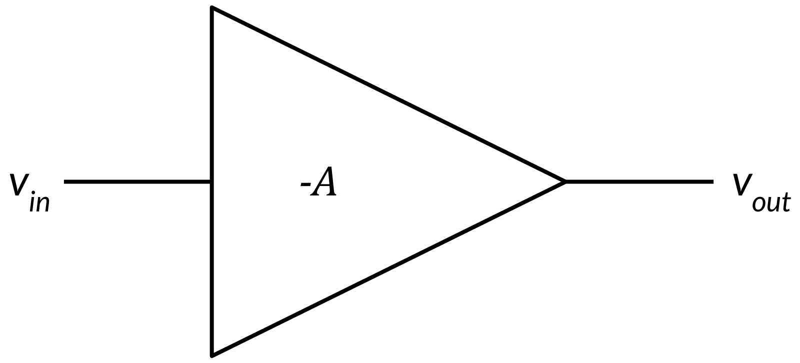
Small Signal DC Analysis

How can we use what we learned to design new circuits?

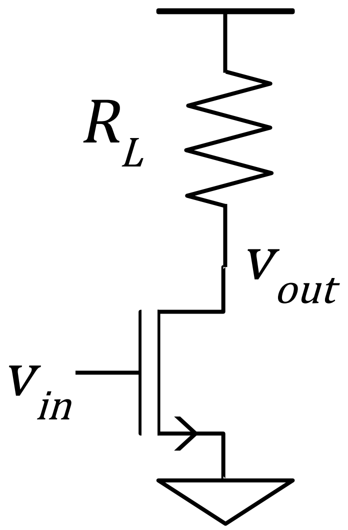
Let's Build A Voltage Amplifier!

We want to maximize $|v_{out} / v_{in}|$



The Simplest Amplifier There Is

Let's start with a common source amplifier.



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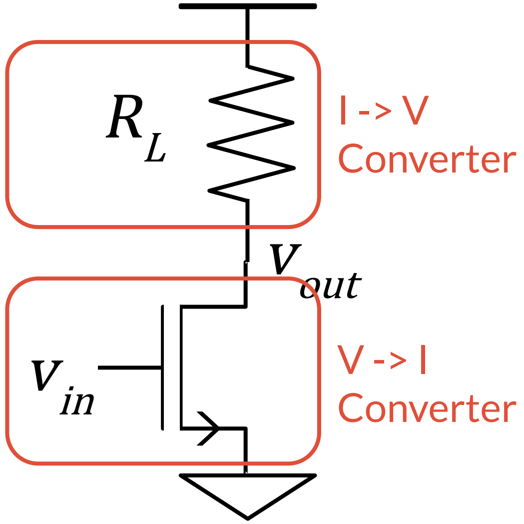
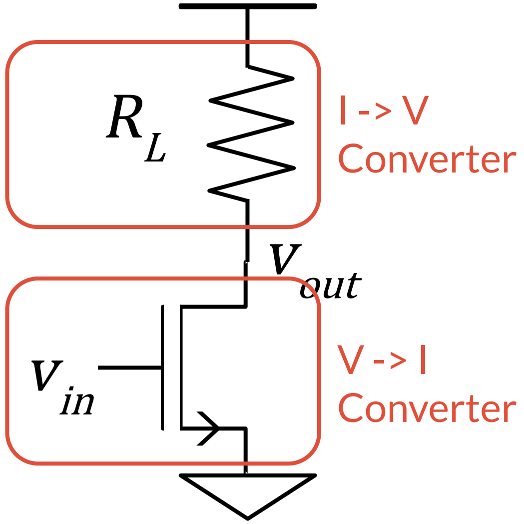


The Simplest Amplifier There Is

Gain should increase will load resistance

$$v_{out} = iR_L$$

$$i \approx -g_m v_{in}$$



$$\frac{v_{out}}{v_{in}} \approx -g_m R_L$$

The Simplest Amplifier There Is

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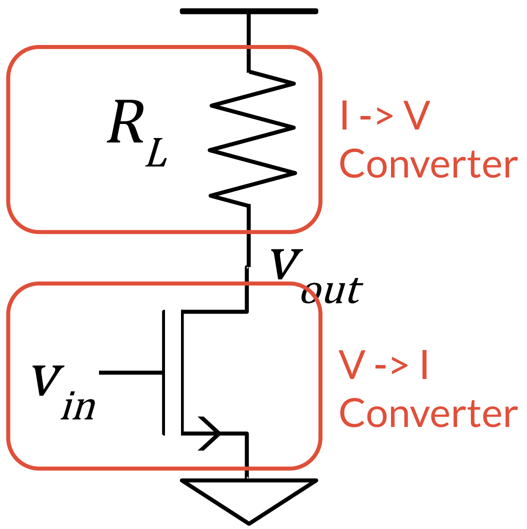
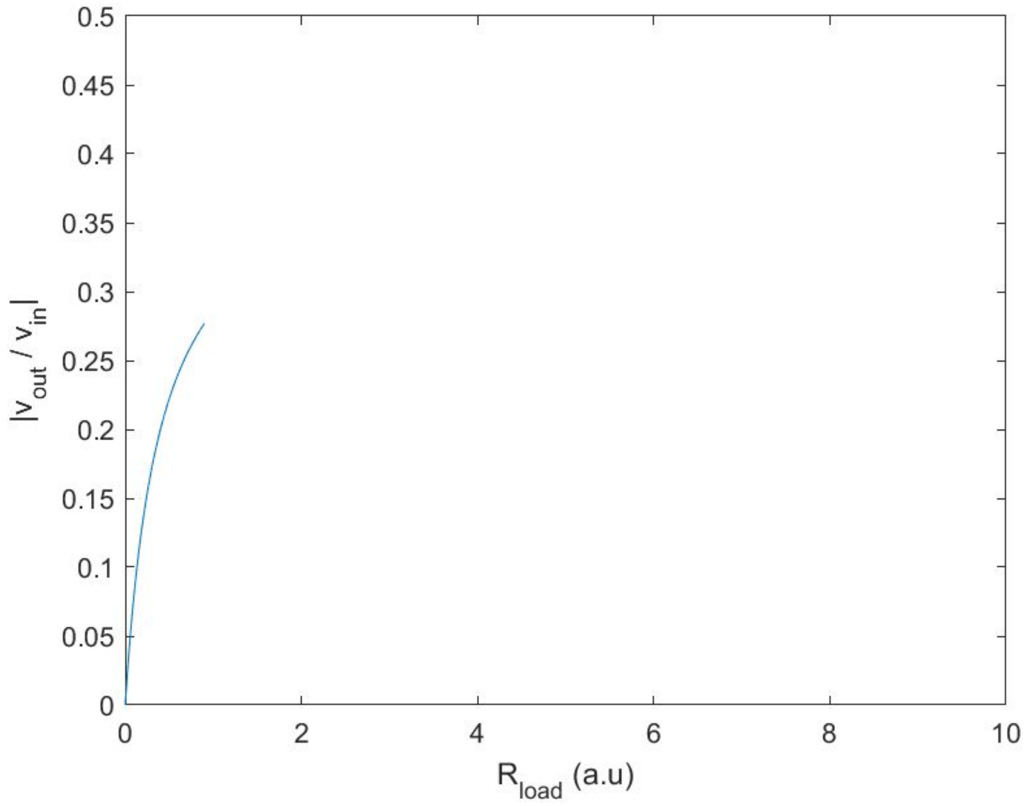
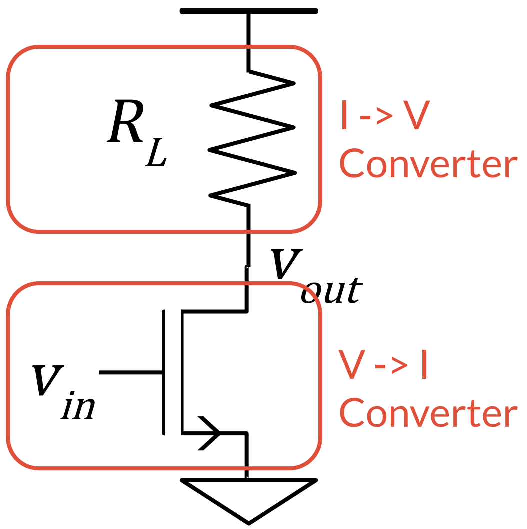


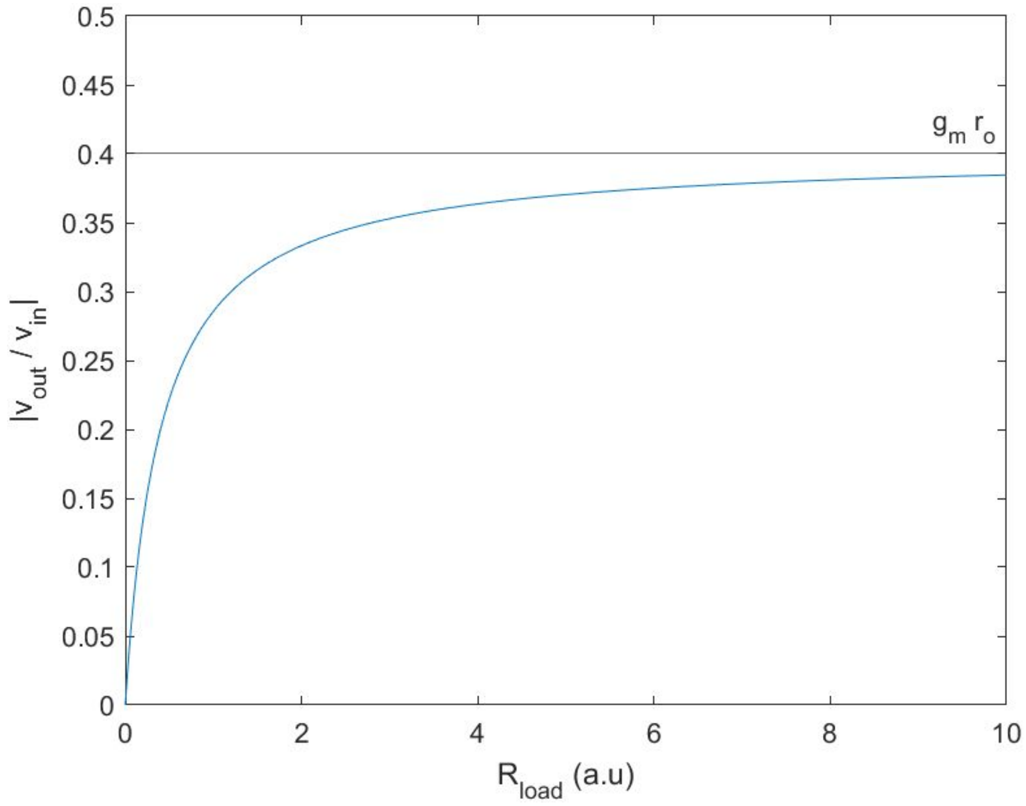


$$\frac{v_{out}}{v_{in}} \approx -g_m R_L$$

The Simplest Amplifier There Is

But the gain eventually flattens out!

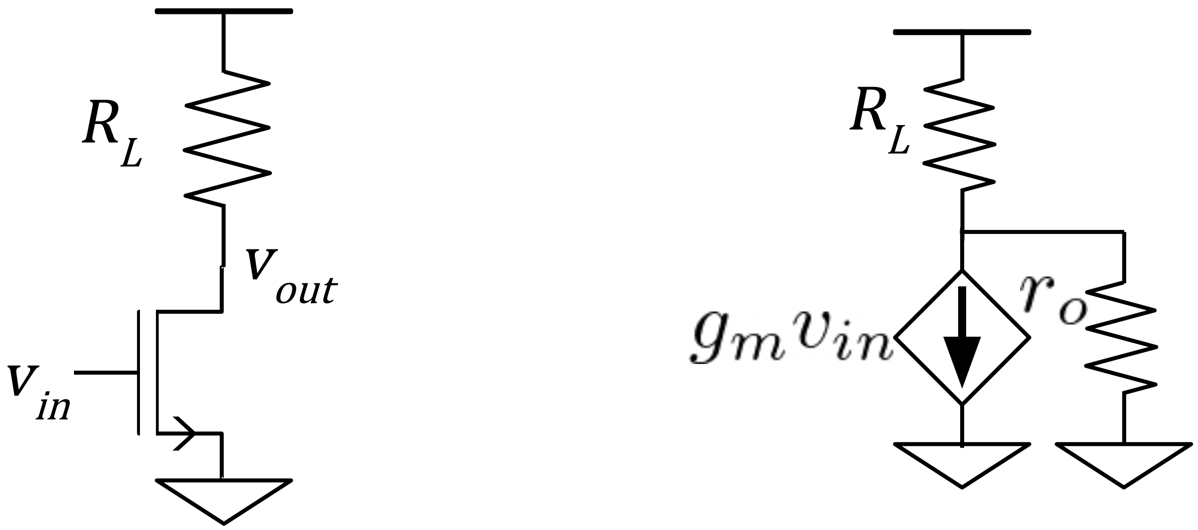




$$\frac{v_{out}}{v_{in}} \approx -g_m R_L$$

Why Does The Common Source Have Limited Gain?

Let's draw the full equivalent circuit



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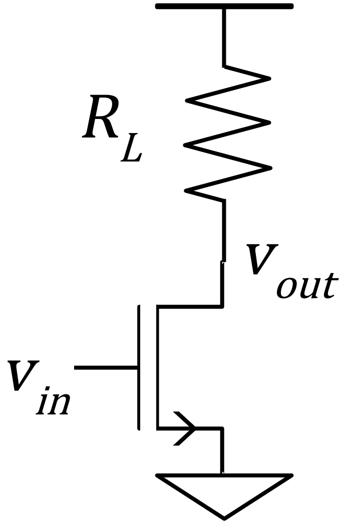
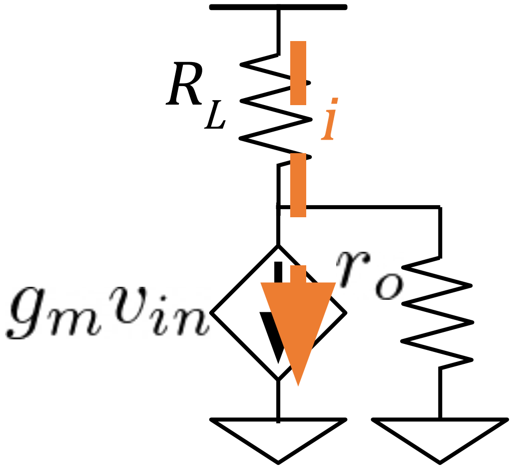
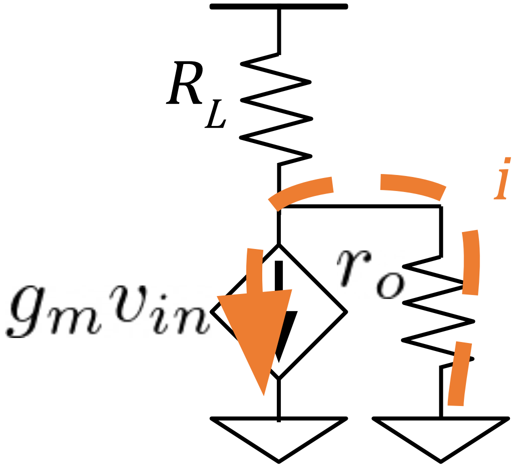


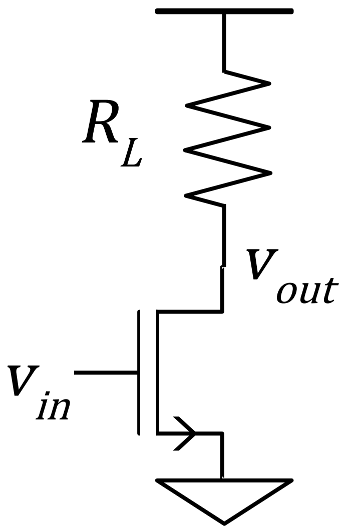
For $R_L < r_o$

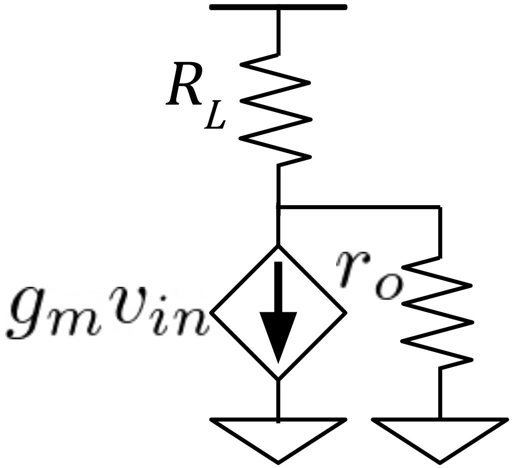


For $R_L > r_o$



The Most Gain We Can Get Out Of A CS Amplifier



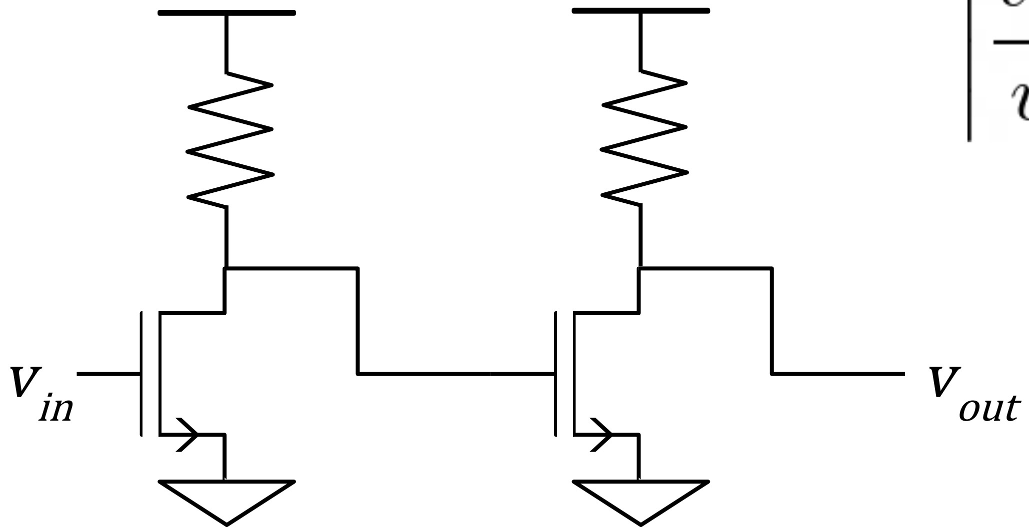


$$\frac{v_{out}}{v_{in}} = -g_m \left(R_L || r_o\right)$$

$$\left|\frac{v_{out}}{v_{in}}\right| \leq g_m r_o$$

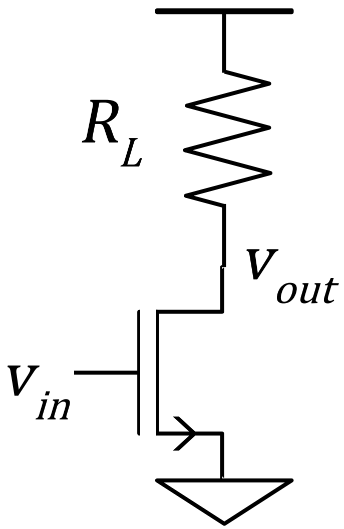
What if we need more gain?

We can square the gain, but double the power

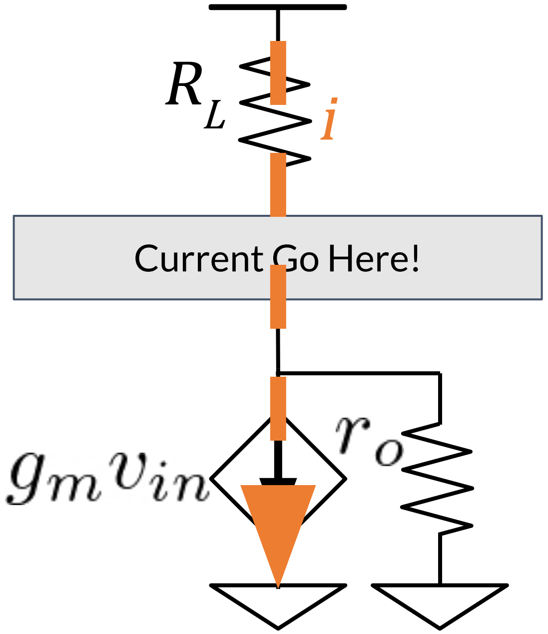


$$\left|\frac{v_{out}}{v_{in}}\right| \leq (g_m r_o)^2$$

Can We “Trick” The Current Into Going Into A Large Load?

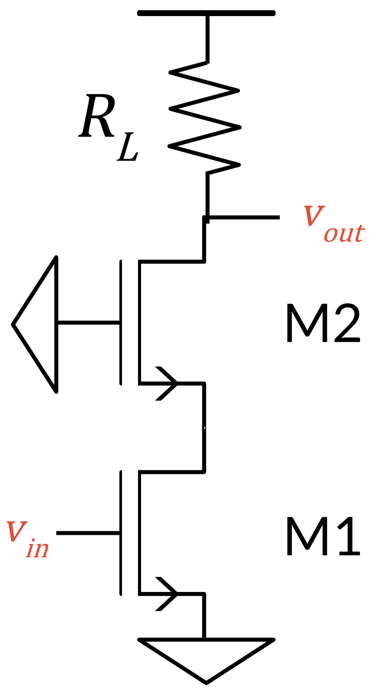


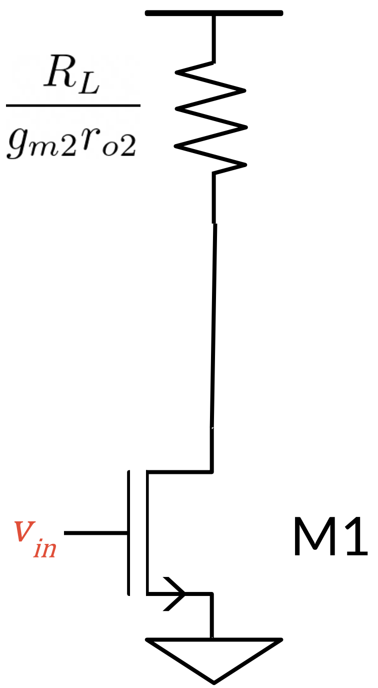
For $R_L >> r_o$

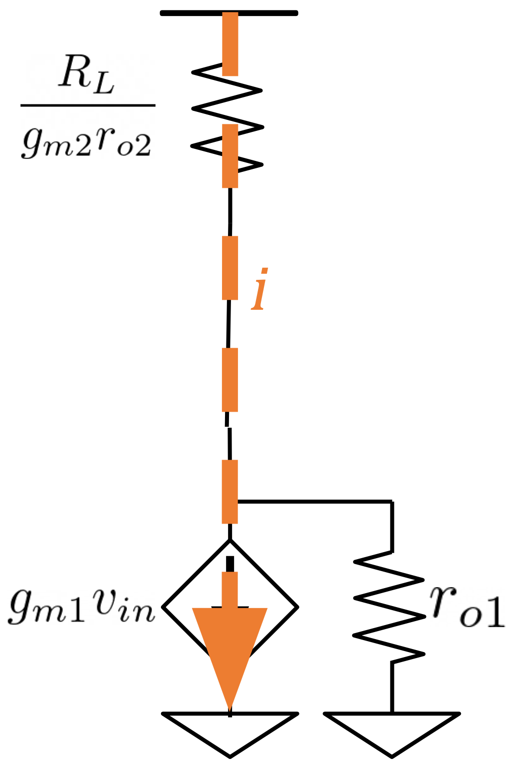


Can We “Trick” The Current Into Going Into A Large Load?

Yes we can!

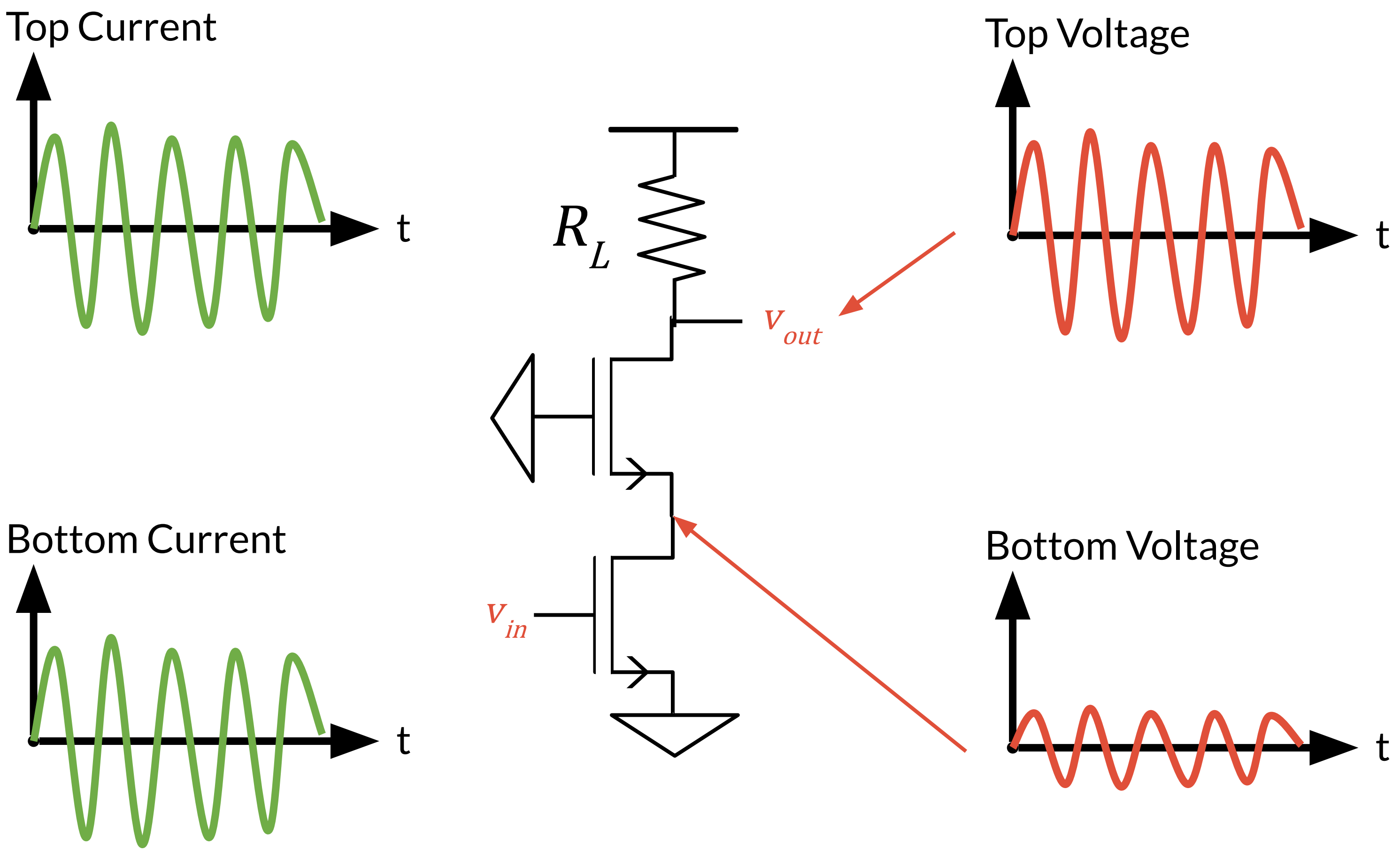






Can We "Trick" The Current Into Going Into A Large Load?

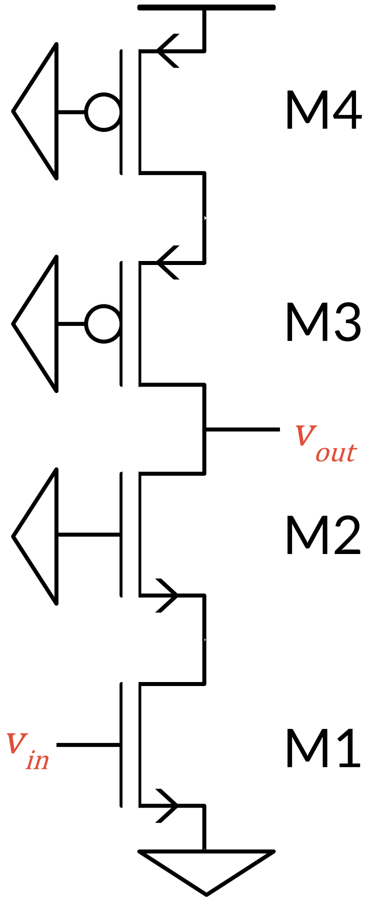
Yes we can!



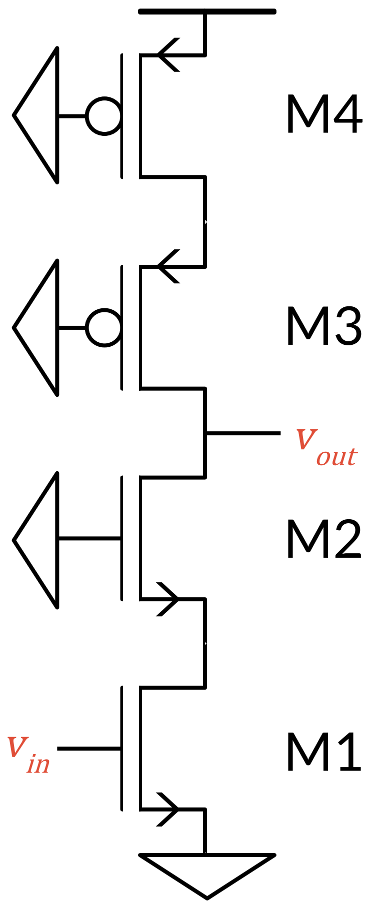
Small Signal DC Analysis

Let’s make it quantitative

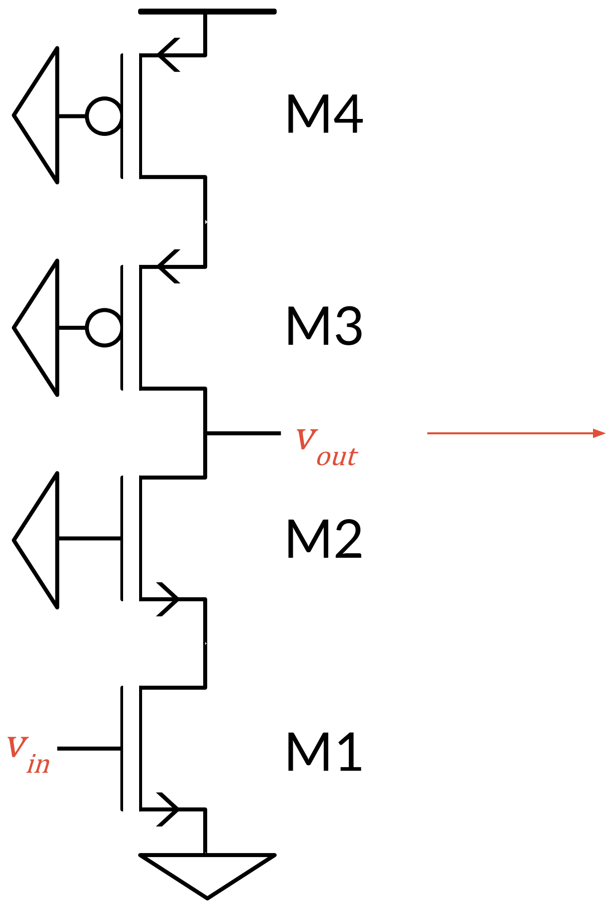
Quantitative walkthrough

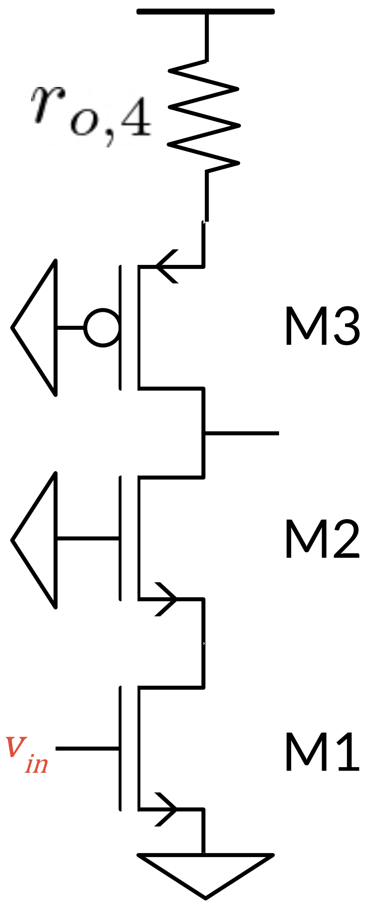


Quantitative walkthrough



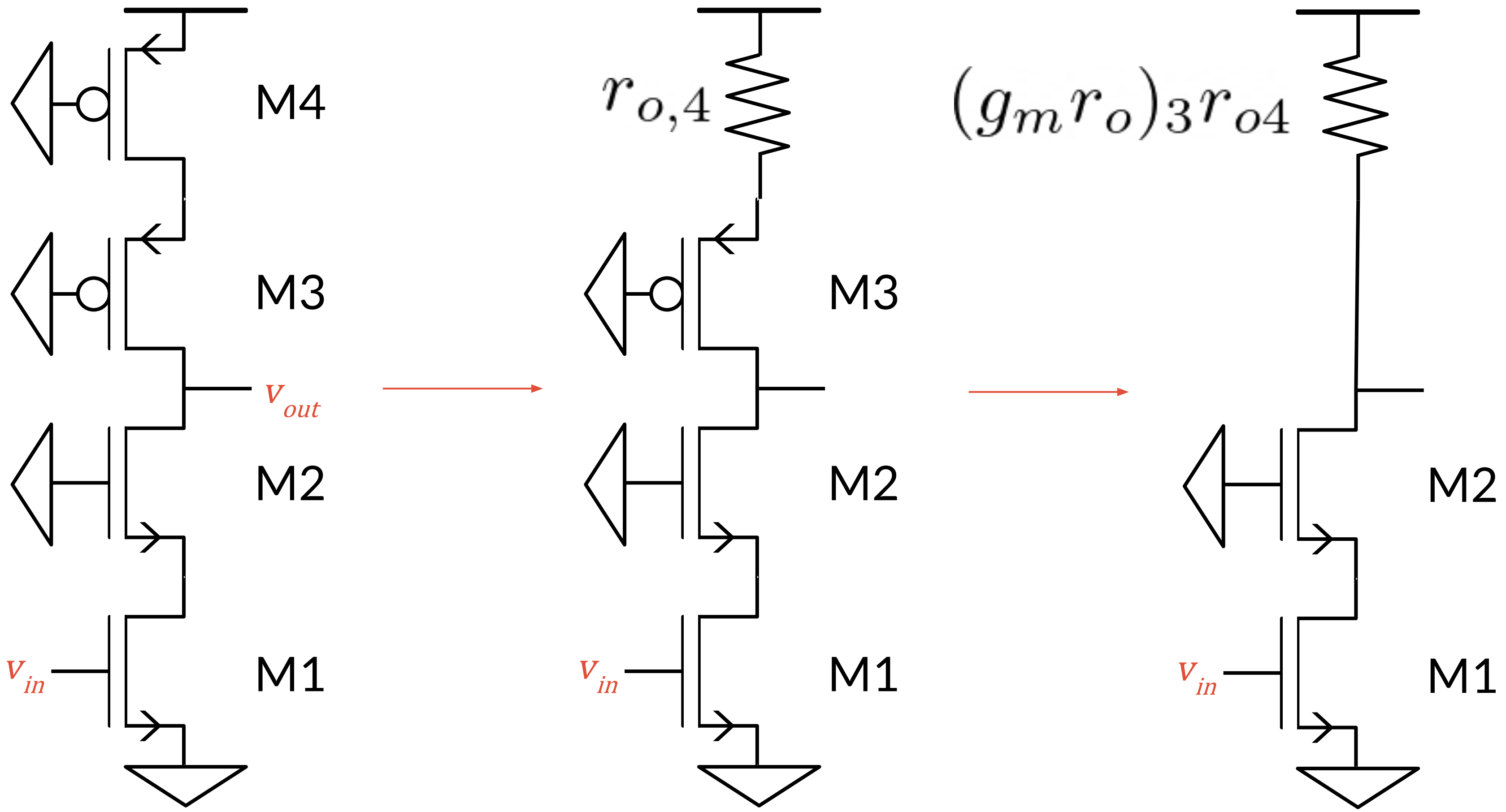
Quantitative walkthrough



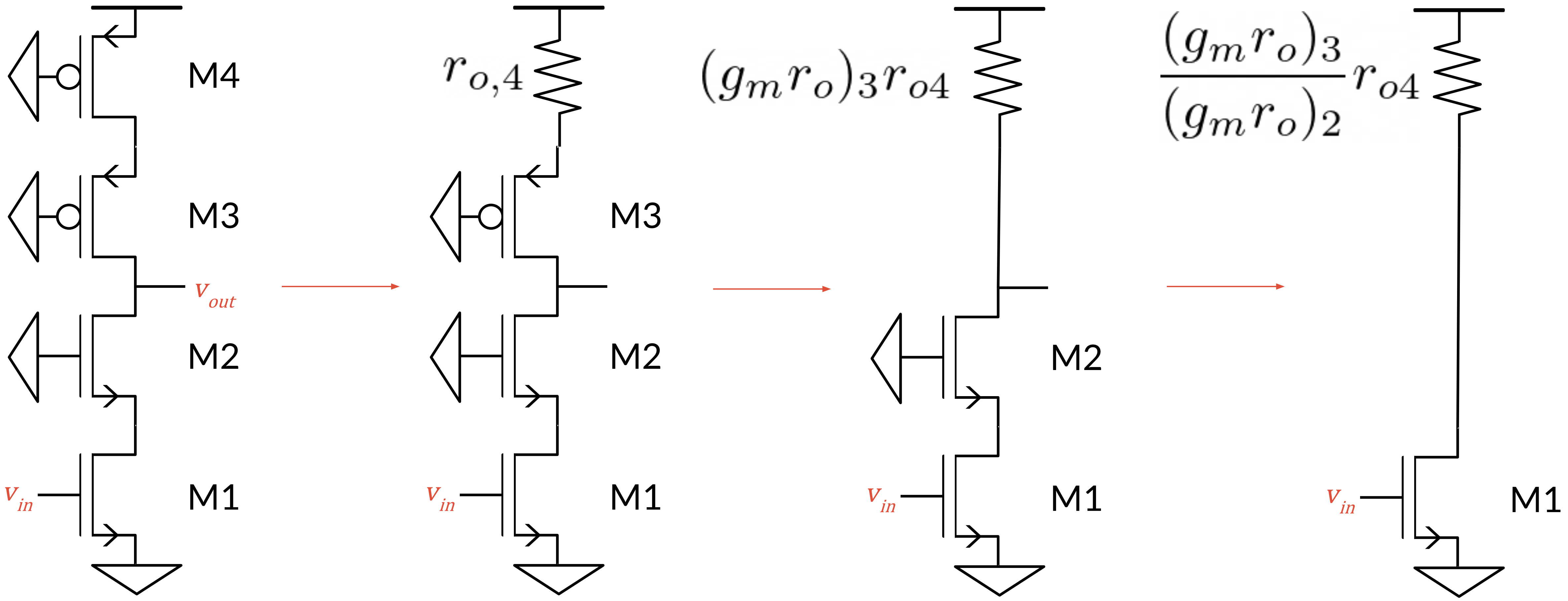


SLAC

Quantitative walkthrough



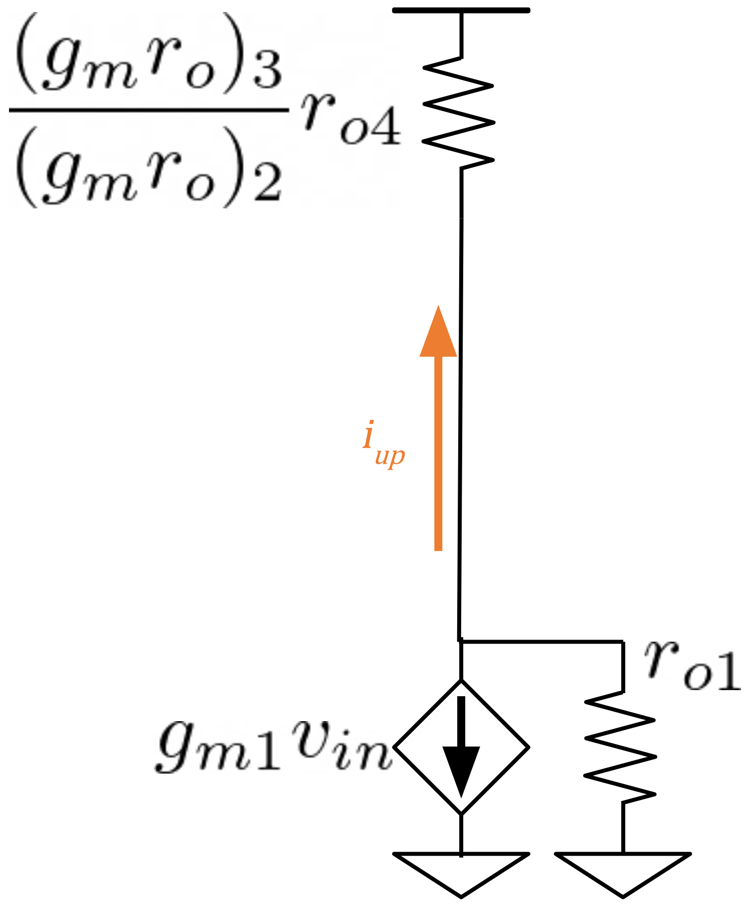
Quantitative walkthrough



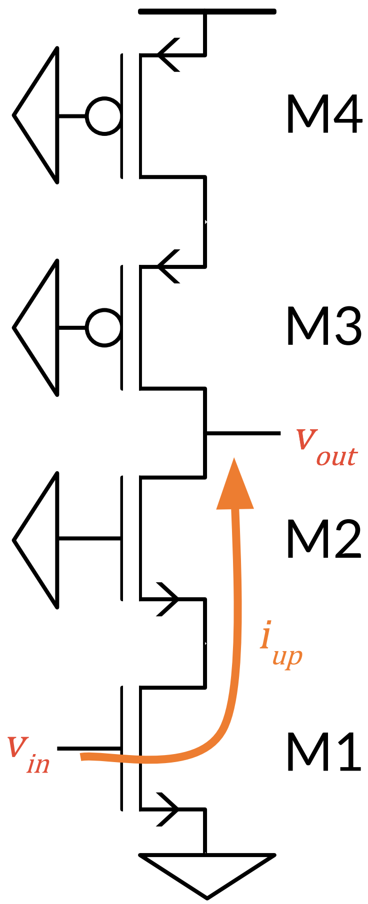
Quantitative walkthrough

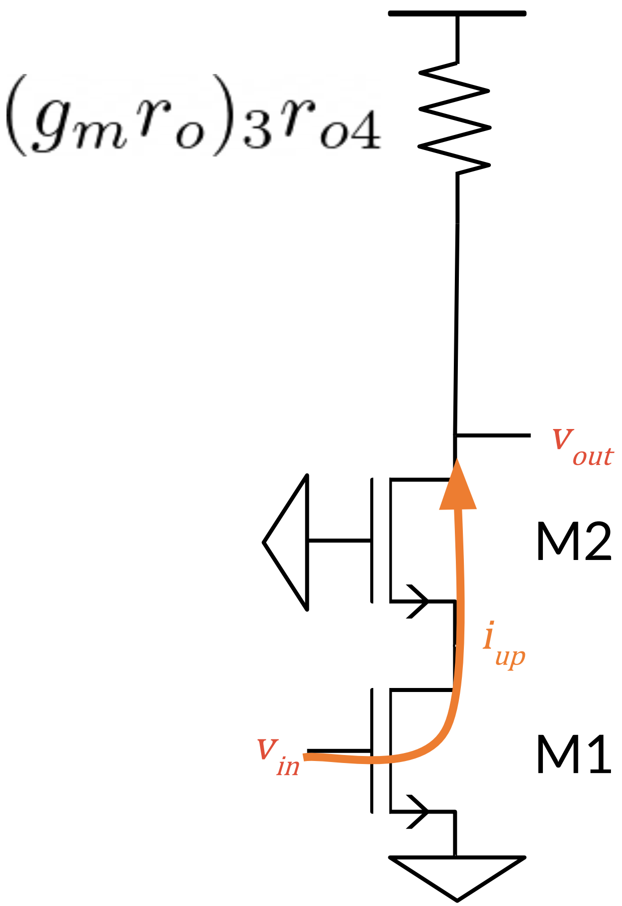
We have a current divider!

$$i_{up} = -\frac{r_{o1}}{r_{o1} + \frac{(g_m r_o)_3}{(g_m r_o)_2} r_{o4}} g_{m1} v_{in}$$



Quantitative walkthrough





$$i_{up} = -\frac{r_{o1}}{r_{o1} + \frac{(g_m r_o)_3}{(g_m r_o)_2} r_{o4}} g_{m1} v_{in}$$

$$v_{out} = (g_m r_o)_3 r_{o4} i_{up}$$

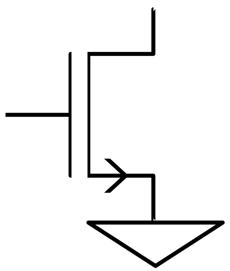
If we assume all transistors have the same gm, ro

$$\frac{v_{out}}{v_{in}} = -\frac{1}{2}(g_m r_o)^2$$

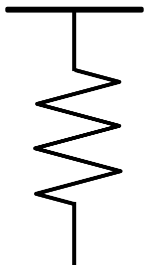
Small Signal DC Analysis

Summary: Designing circuits with building blocks

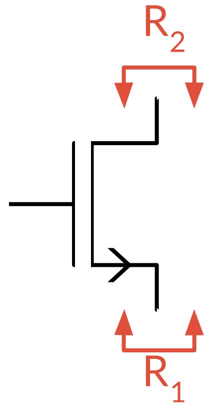
The Three Types of Building Blocks



V → I
Converters

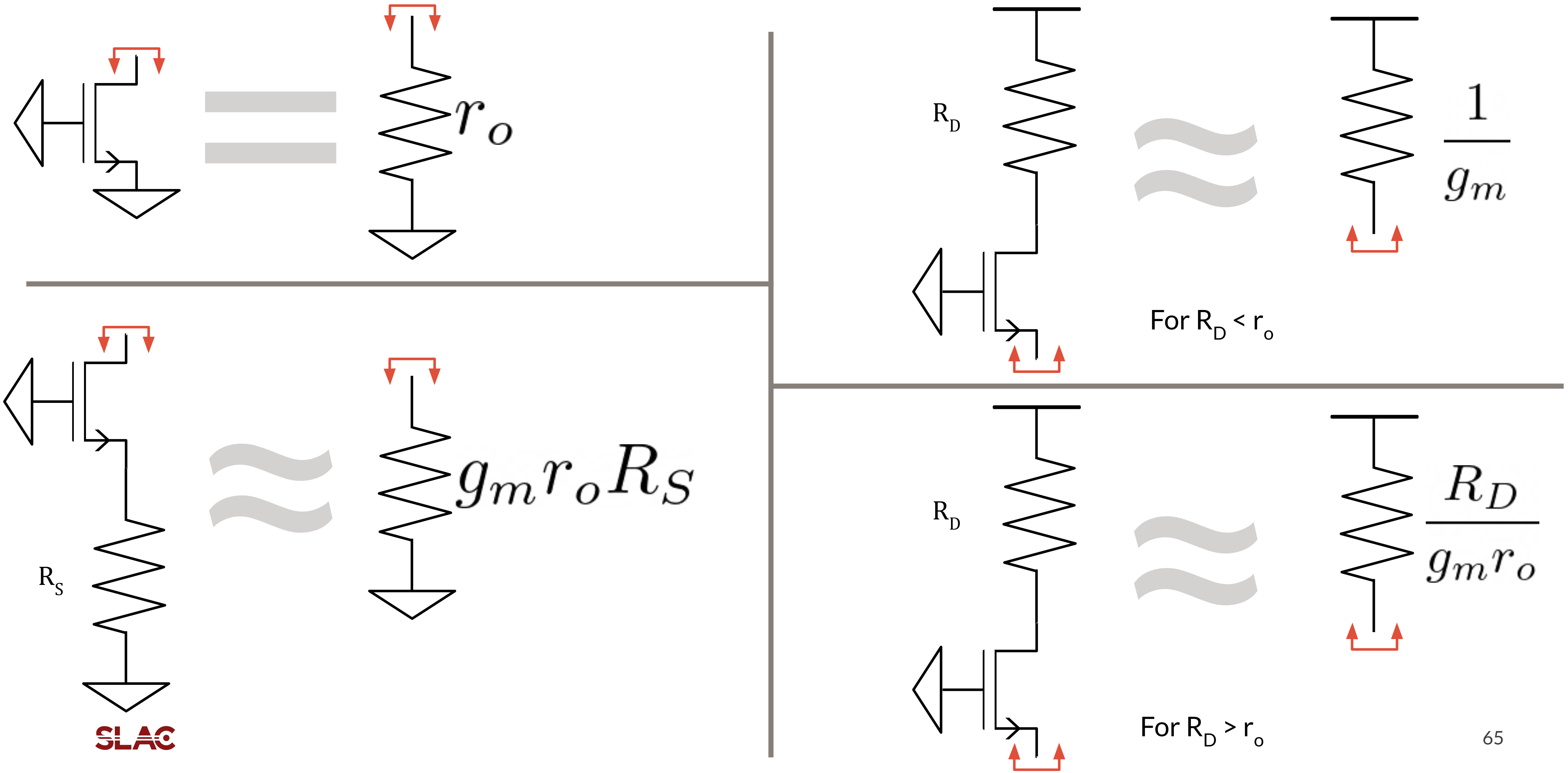


I → V
Converters



Impedance
Transformers

Transistor cheat-sheet (assuming $g_m r_0 \gg 1$)



SLAC

DC Biasing And Sizing Transistors

Device equations and gm/Id

Back to the MOSFET I-V equation

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{gs} - V_{th})^2$$

Key Observation

Current is linear in the width (intuitive)

$$I_D = W f\left(V_{gs}, L\right)$$

Consequences: gm/Id is independent of W!

$$I_D = W f\left(V_{gs}, L\right)$$

$$g_m = \frac{\partial I_D}{\partial V_{gs}} = W f'\left(V_{gs}, L\right)$$

$$\frac{g_m}{I_D} = h\left(V_{gs}, L\right)$$

Observation: Other Quantities Are Independent Of W

$$\frac{g_m}{I_D} = h\left(V_{gs}, L\right)$$

$$\frac{g_m}{C_{gg}} = h_1\left(V_{gs}, L\right)$$

$$\frac{I_D}{W} = h_2\left(V_{gs}, L\right)$$

We can express quantities independent of W in terms of gm/Id

$$\frac{I_D}{W} = f_\alpha\left(\frac{g_m}{I_D}, L\right)$$

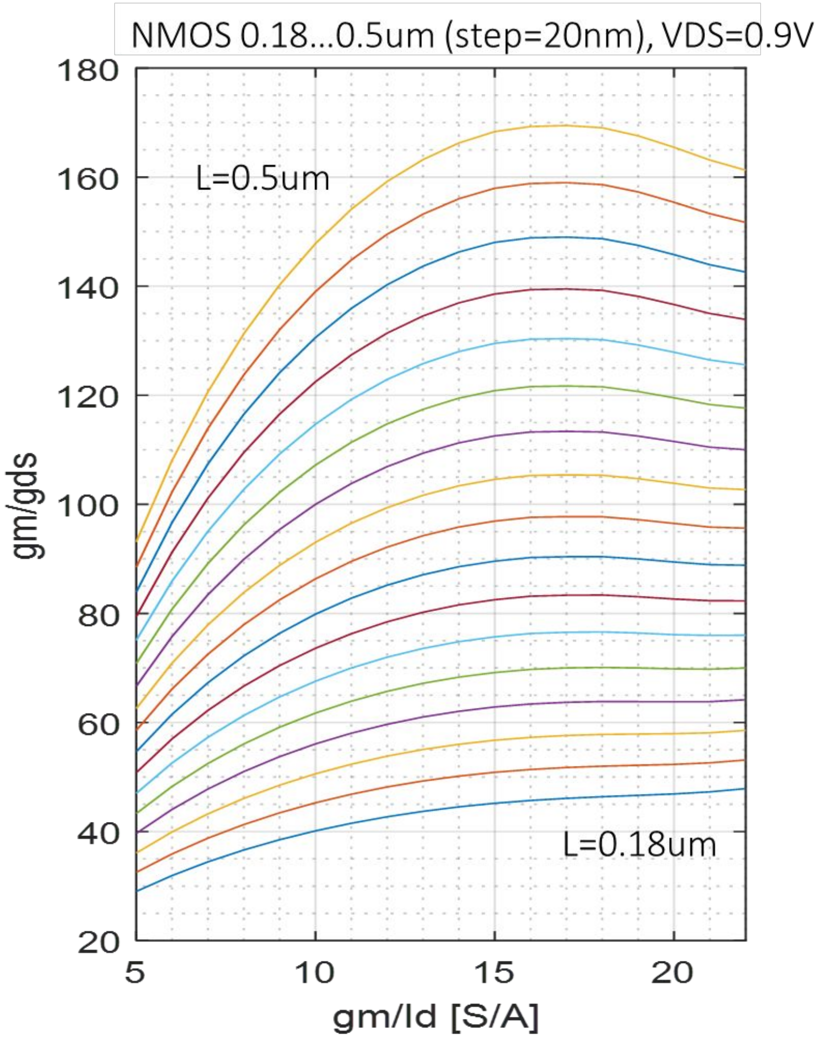
$$\frac{g_m}{C_{gg}} = \omega_T = f_\beta\left(\frac{g_m}{I_D}, L\right)$$

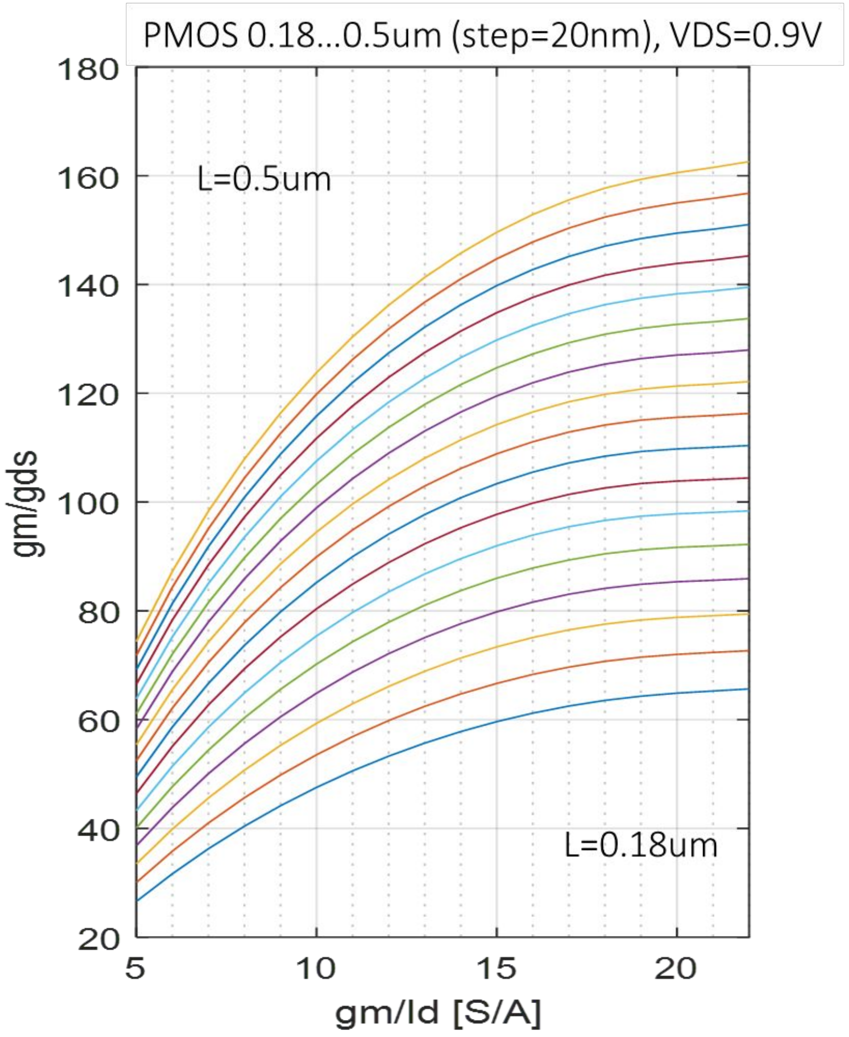
$$V_{gs} = f_\gamma\left(\frac{g_m}{I_D}, L\right)$$

Design Methodology

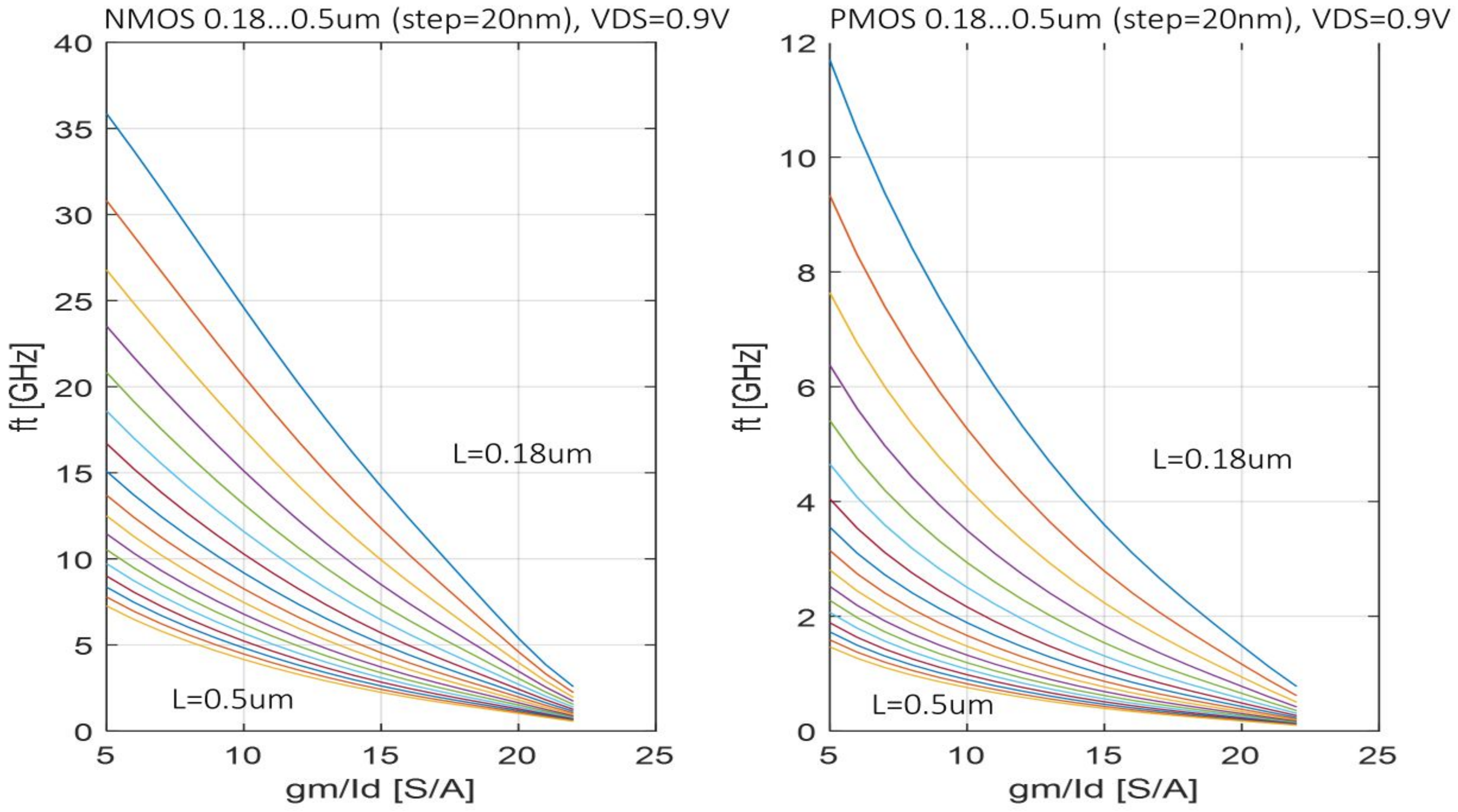
Use gm/Id to describe how a transistor is biased and operating

gm/gds = gm*ro → Intrinsic Gain Plots

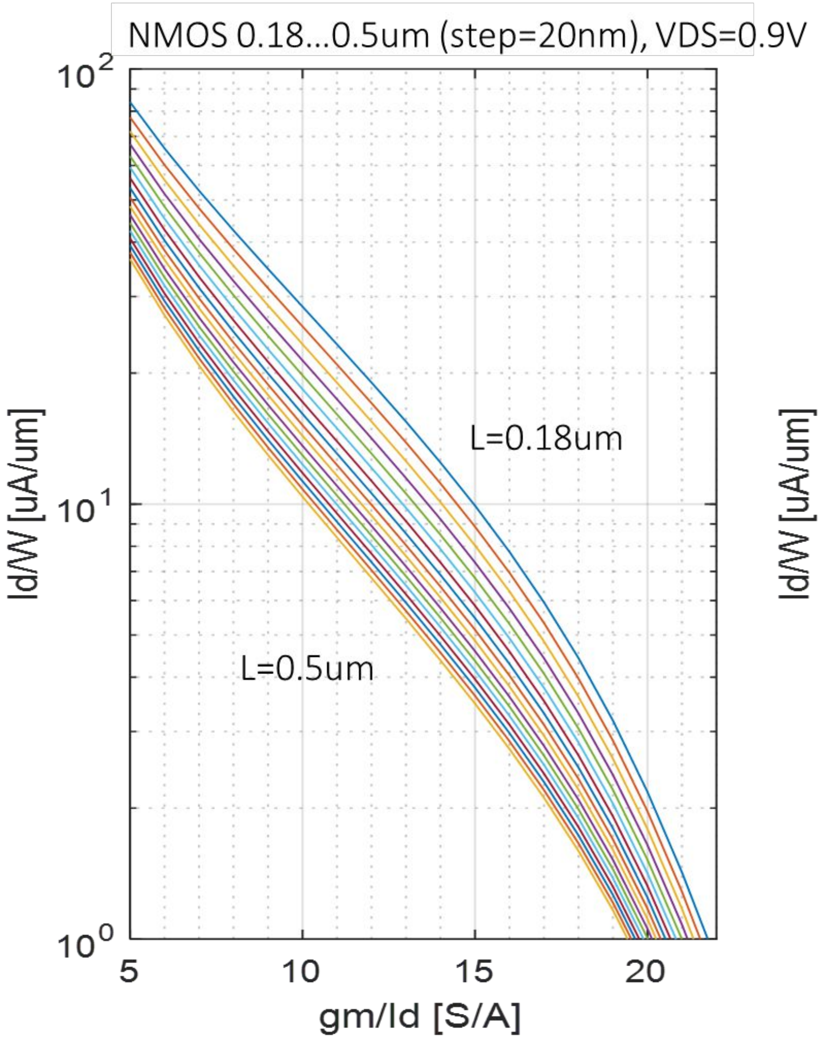


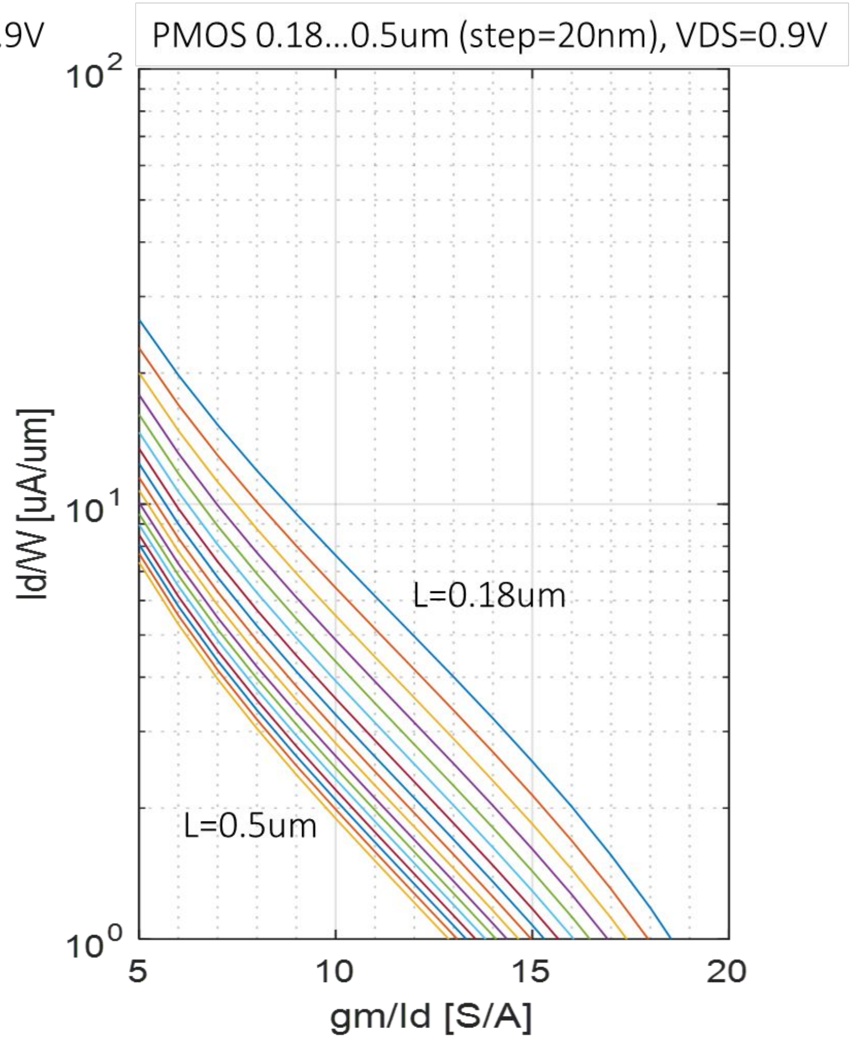


fT = gm/Cgg/2pi → Transit Frequency Plots

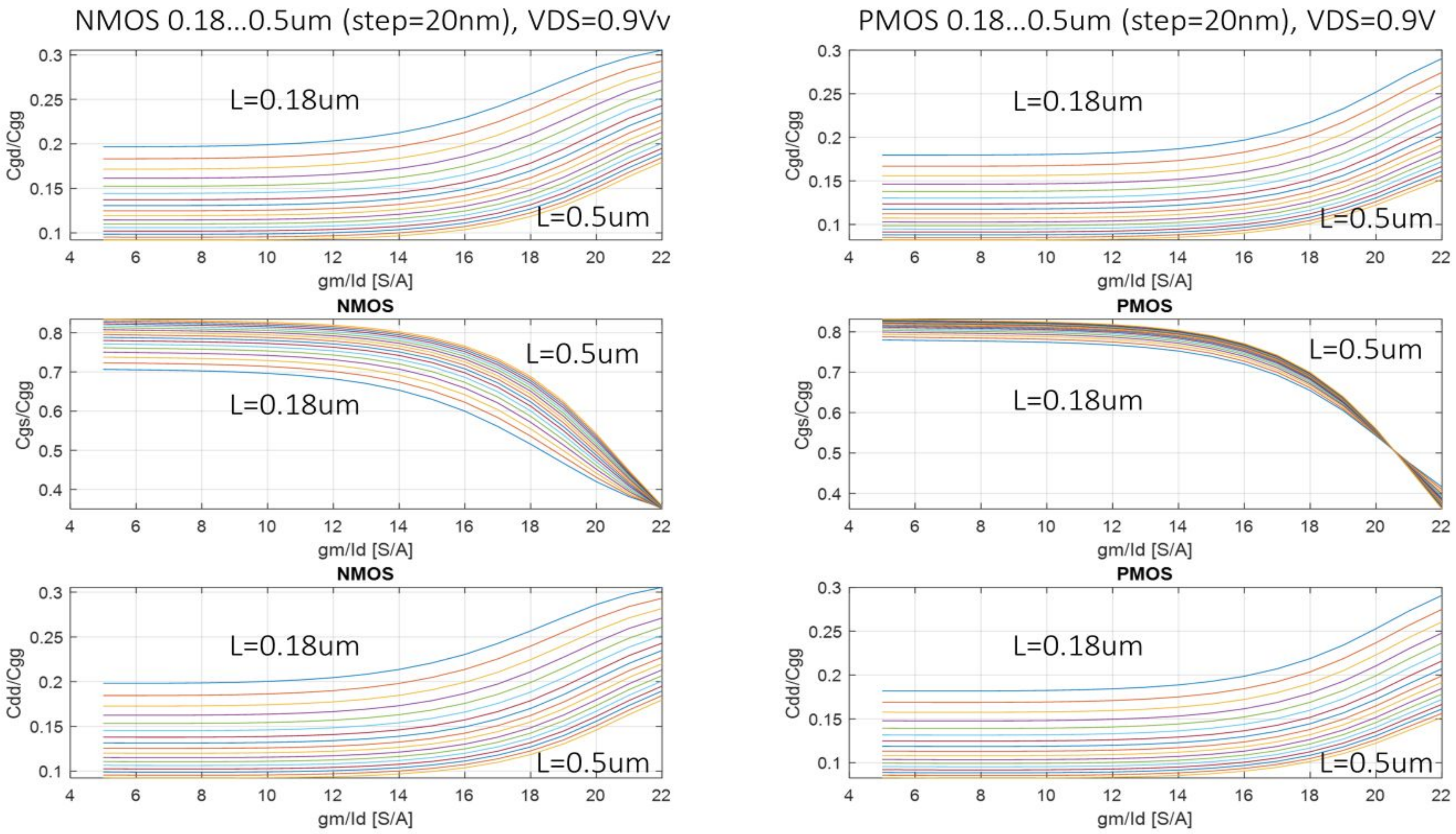


Id/W → Current Density Plots





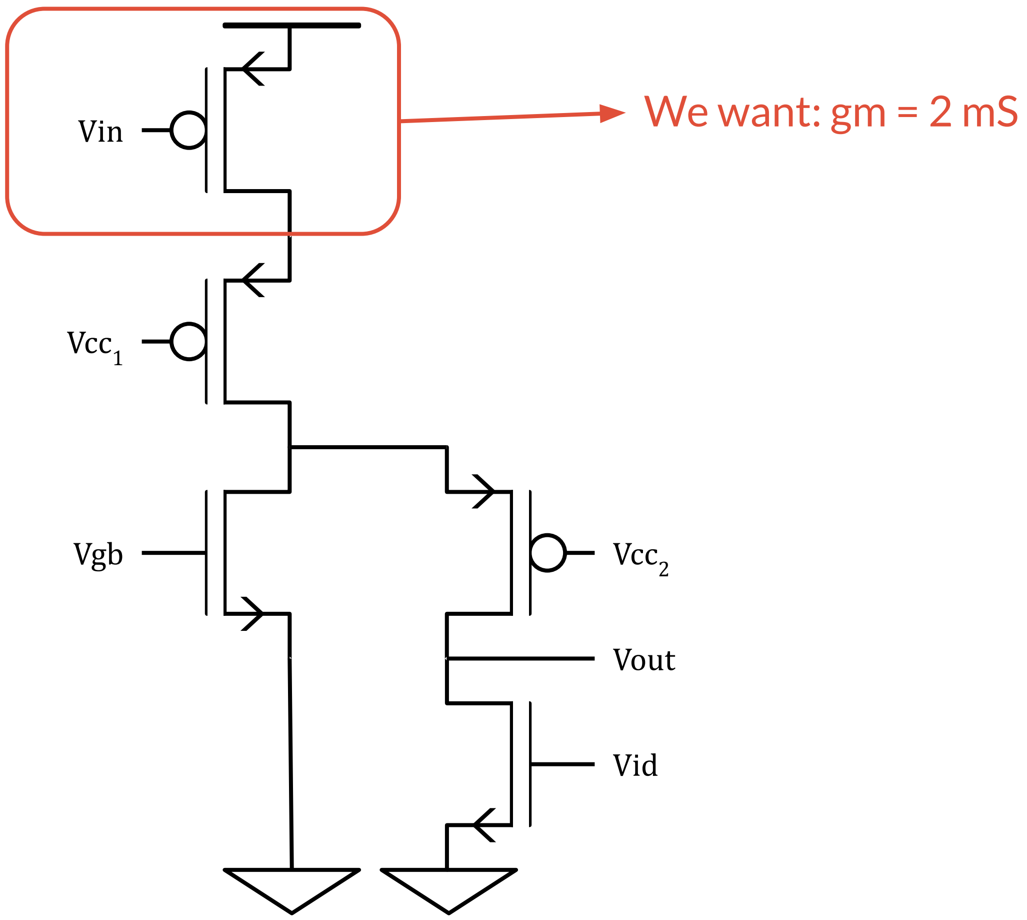
Extrinsic Capacitances ratios



DC Biasing And Sizing Transistors

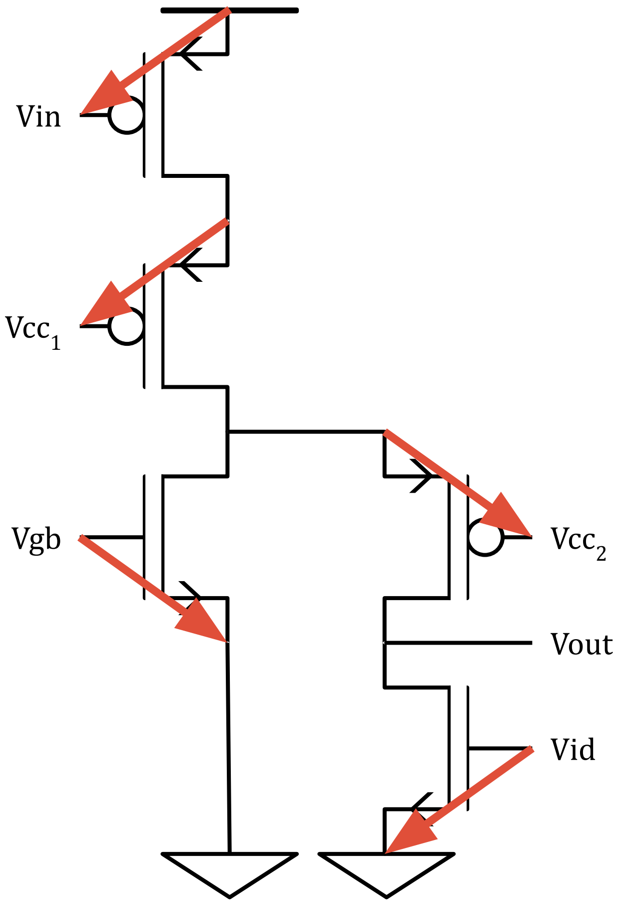
How to size transistors to get a desired gm

Typical situation: We want some gm



Step 1: Obtain gm/Id, L

We will cover later how their optimal values can be found from noise and bandwidth considerations.



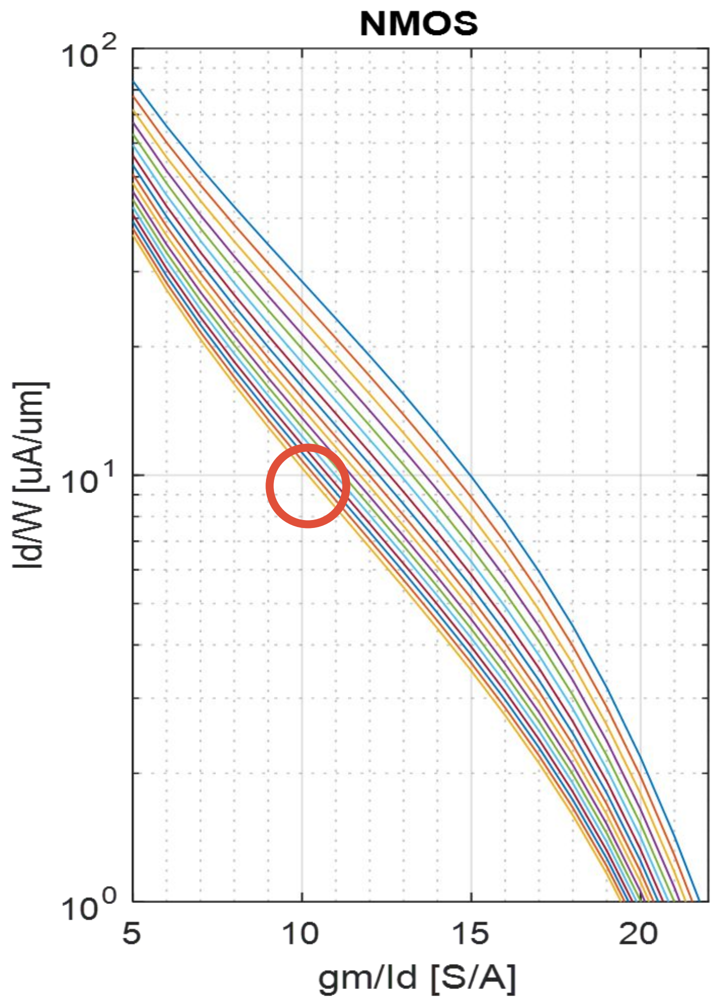
Step 2: Given gm/Id, we can find the current density, etc

$$\frac{g_m}{I_D}$$

$$\frac{I_D}{W} = f_\alpha\left(\frac{g_m}{I_D}, L\right)$$

$$\frac{g_m}{C_{gg}} = \omega_T = f_\beta\left(\frac{g_m}{I_D}, L\right)$$

$$V_{gs} = f_\gamma\left(\frac{g_m}{I_D}, L\right)$$



Step 3: Given the ratios, we can find transistor widths, etc

$$\frac{g_m}{I_D}$$

$$\frac{I_D}{W} = f_\alpha\left(\frac{g_m}{I_D}, L\right)$$

$$\frac{g_m}{C_{gg}} = \omega_T = f_\beta\left(\frac{g_m}{I_D}, L\right)$$

$$V_{gs} = f_\gamma\left(\frac{g_m}{I_D}, L\right)$$

$$I_D = g_m / \frac{g_m}{I_D}$$

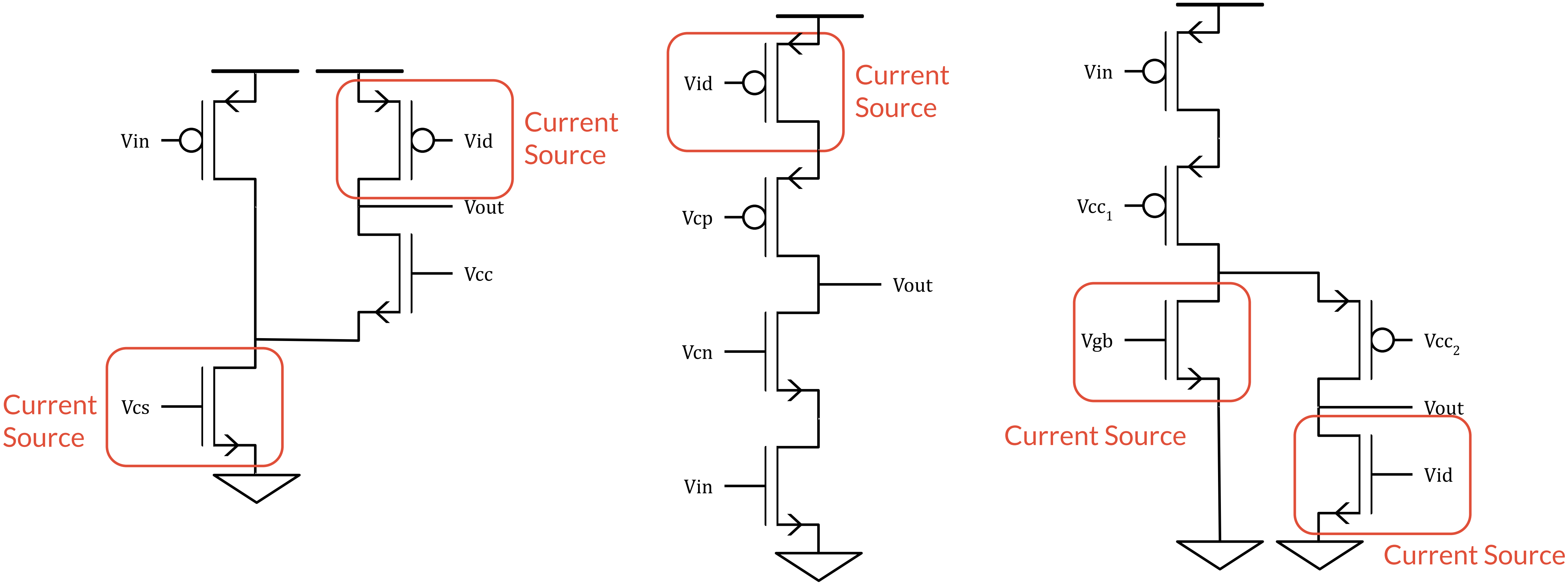
$$W = I_D / \frac{I_D}{W}$$

$$C_{gg} = g_m / \frac{g_m}{C_{gg}}$$

DC Biasing And Sizing Transistors

Current sources

The current sources simply set the desired amount of gm



Intermission

Our first design exercise

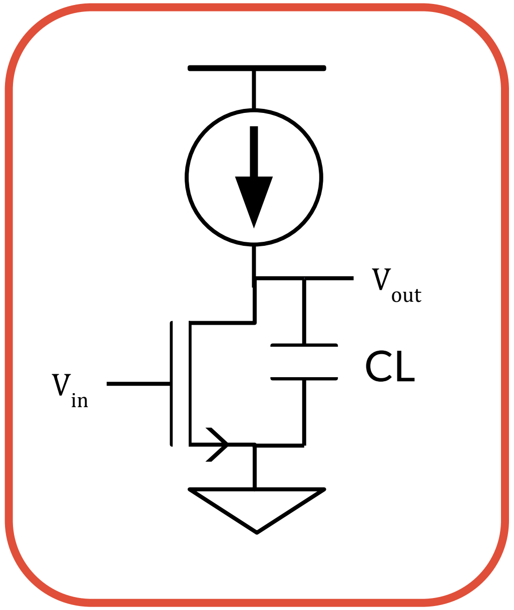
Generic 180nm PDK / 1.8V Supply

No Deep N-Wells: MOSFET body connected to GND/VDD

Task: Designing An Open Loop Intrinsic Amplifier

Part 1: Intrinsic Gain Stage

- Id< 5uA
- CL=250fF
- Vout = 0.9V at DC (see next slide)
- Goals:
  - Gain-Bandwidth Product: >16MHz
  - Maximize Gain

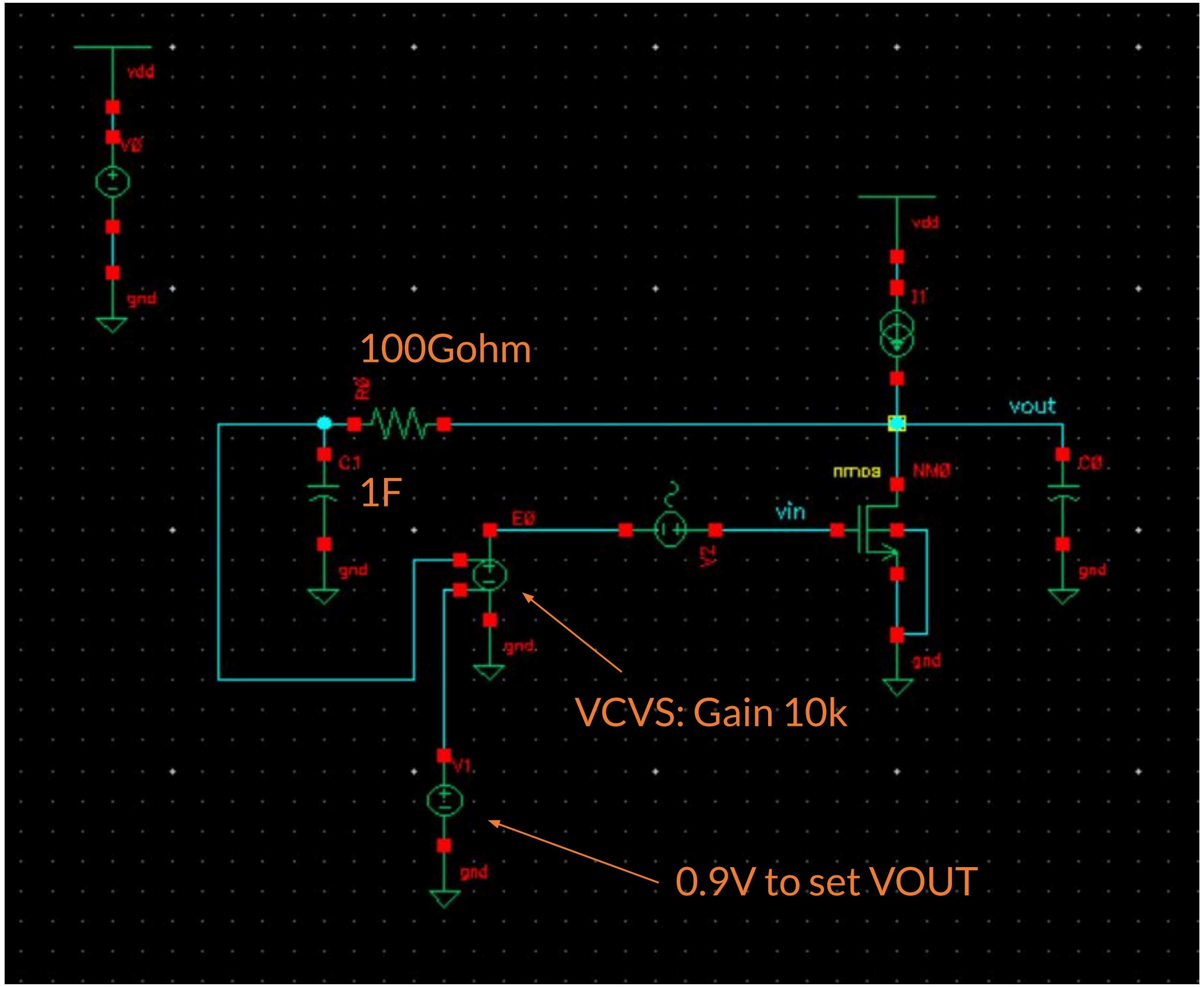


Methodology:

1. By hand: derive gain in terms of gm, gds then derive the expression of the pole and the GBW product
2. Calculate gm to obtain needed GBW
3. Pick an appropriate gm/gds and L to achieve desired gain.
4. Given gm/gds and L, we've fixed gm/Id, fT and Id/W.
5. Using Id/W, find the needed W
6. Run a simulation

Sample Intrinsic Gain Stage Implementation

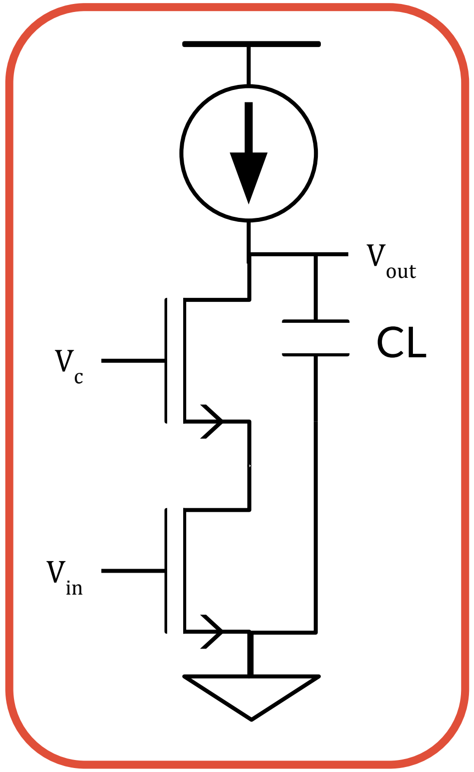
Note: The auxiliary circuit is an ideal op-amp connected to a lowpass filter. The lowpass filter only lets the DC signal through. The op-amp biases the nMOS such that VOUT = 0.9V in DC



Task: Designing An Open Loop Amplifier

Part 2: Cascoded Stage

- Id< 5uA
- CL=250fF
- Vout = 0.9V at DC (see previous slide)
- Goals:
  - Gain-Bandwidth Product: >16MHz
  - Maximize Gain



Methodology:

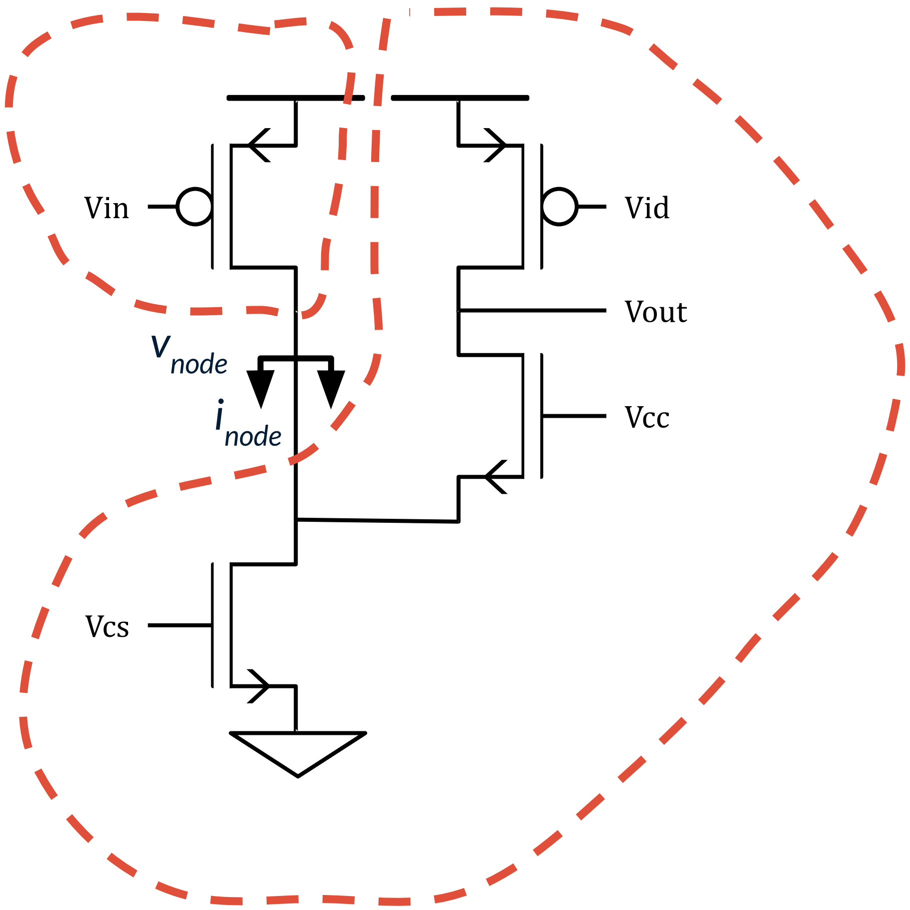
1. Simply add a cascode with the same dimensions of the input transistor
2. Derive the equations
3. See what maximum gain can be achieved
4. Run a simulation. You may need to try different voltages for V_c

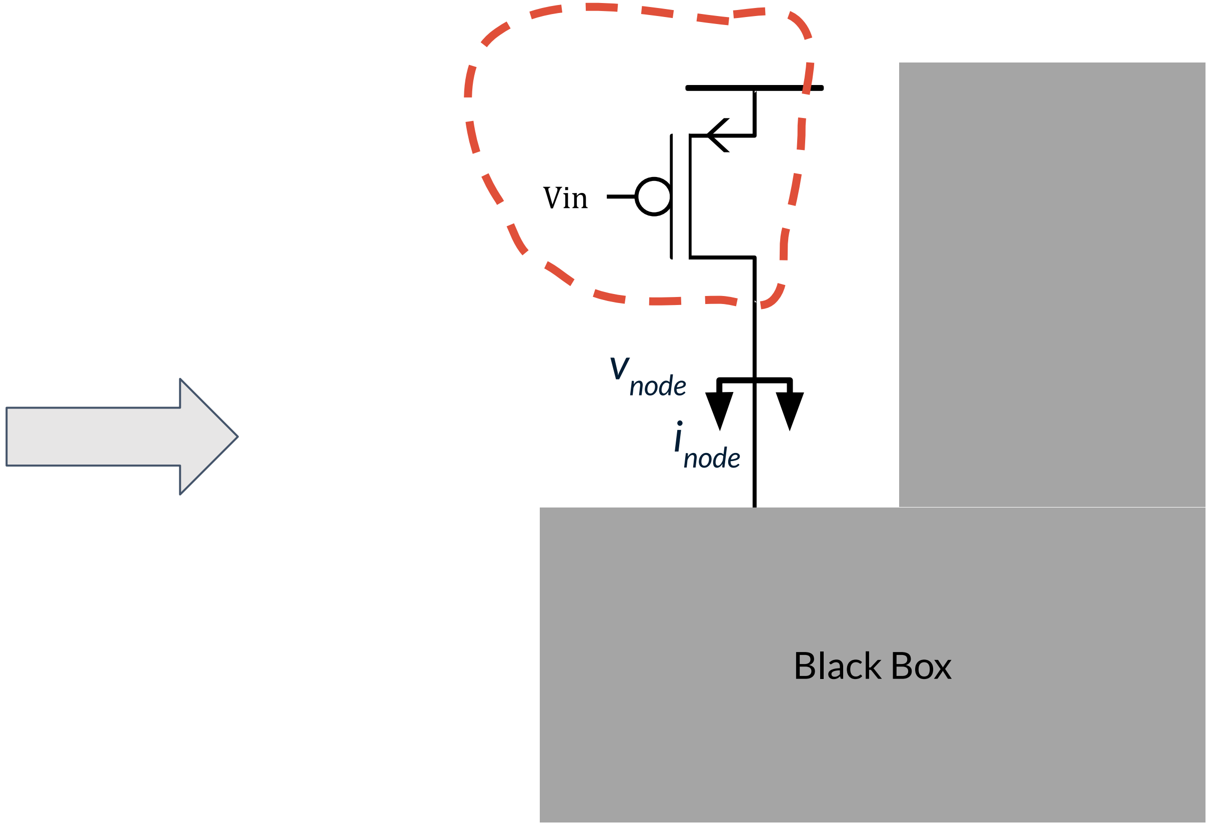
AC Analysis And Feedback

How To Solve Problems With Feedback Loops

Yesterday's Lecture

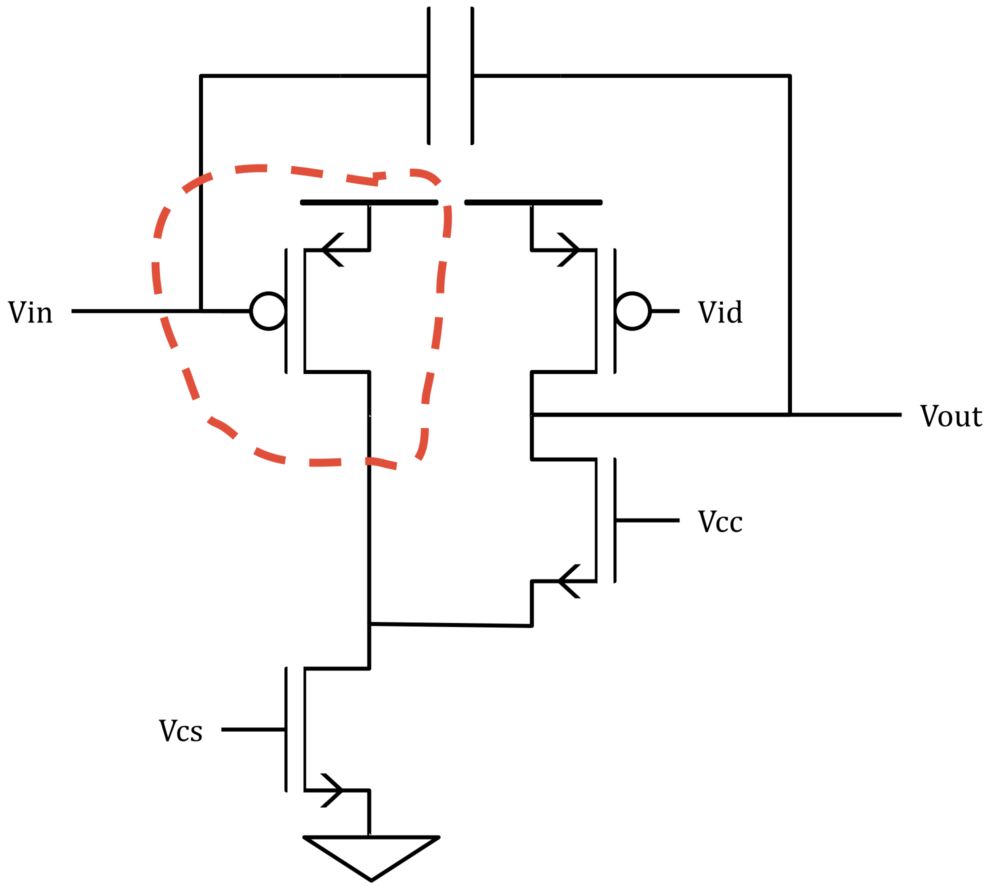
So far, we've looked at circuits without feedback





Problem: What If We Have Loops?

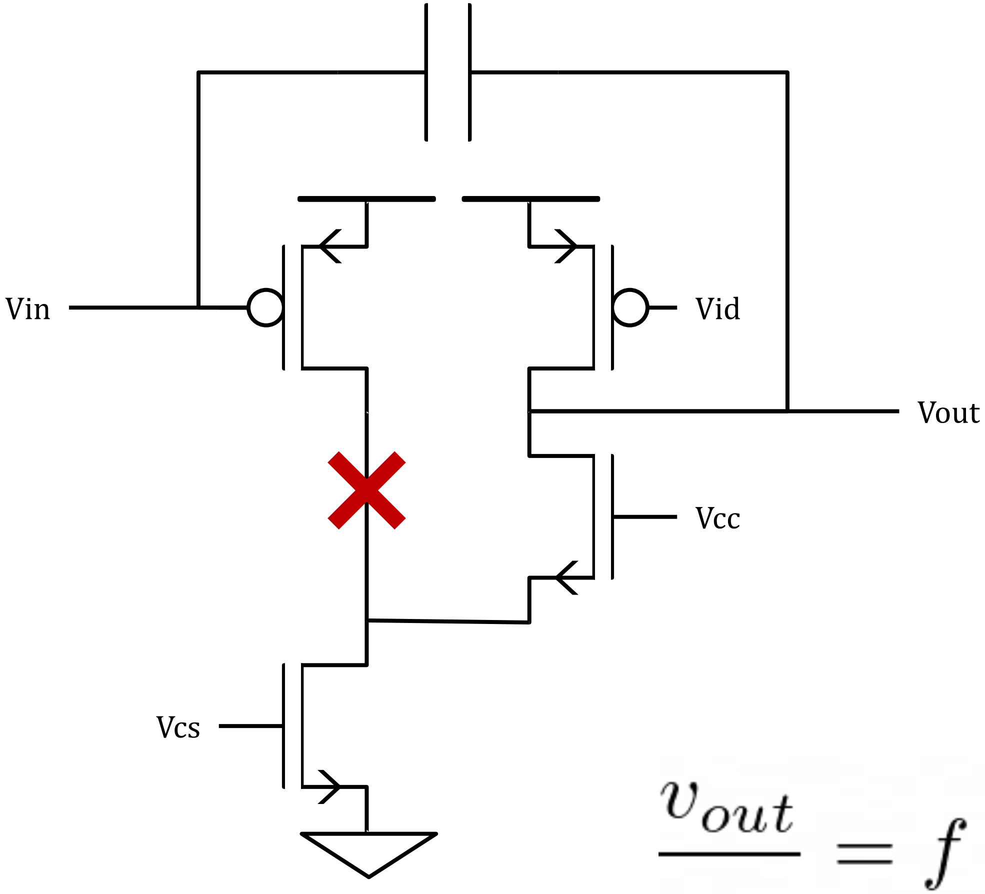
There are two points of contact between the transistor and the output

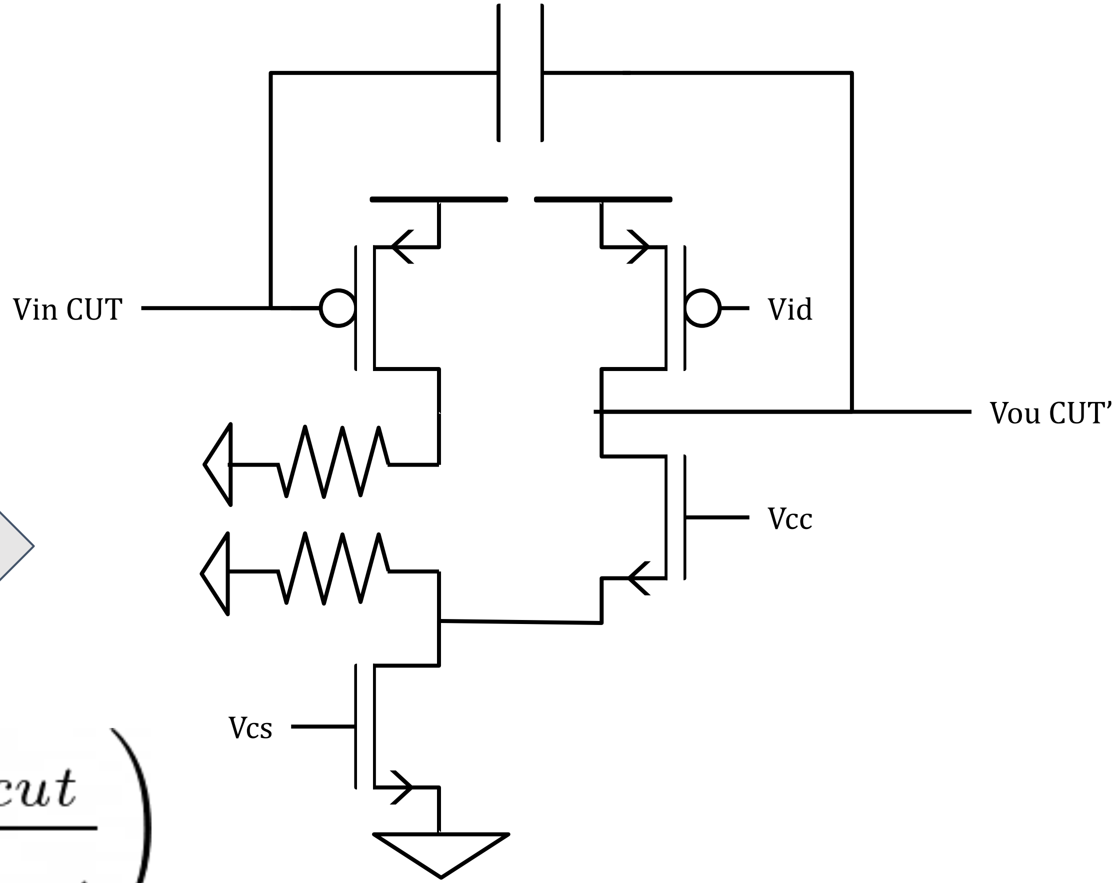


Method: We Cut The Feedback Loop

When the loop is cut, we get a circuit without feedback which we can solve.

We then relate the gain of this “cut” circuit to the gain of the uncut circuit





$$\frac{v_{out}}{v_{in}} = f\left(\frac{v_{in,cut}}{v_{out,cut}}\right)$$

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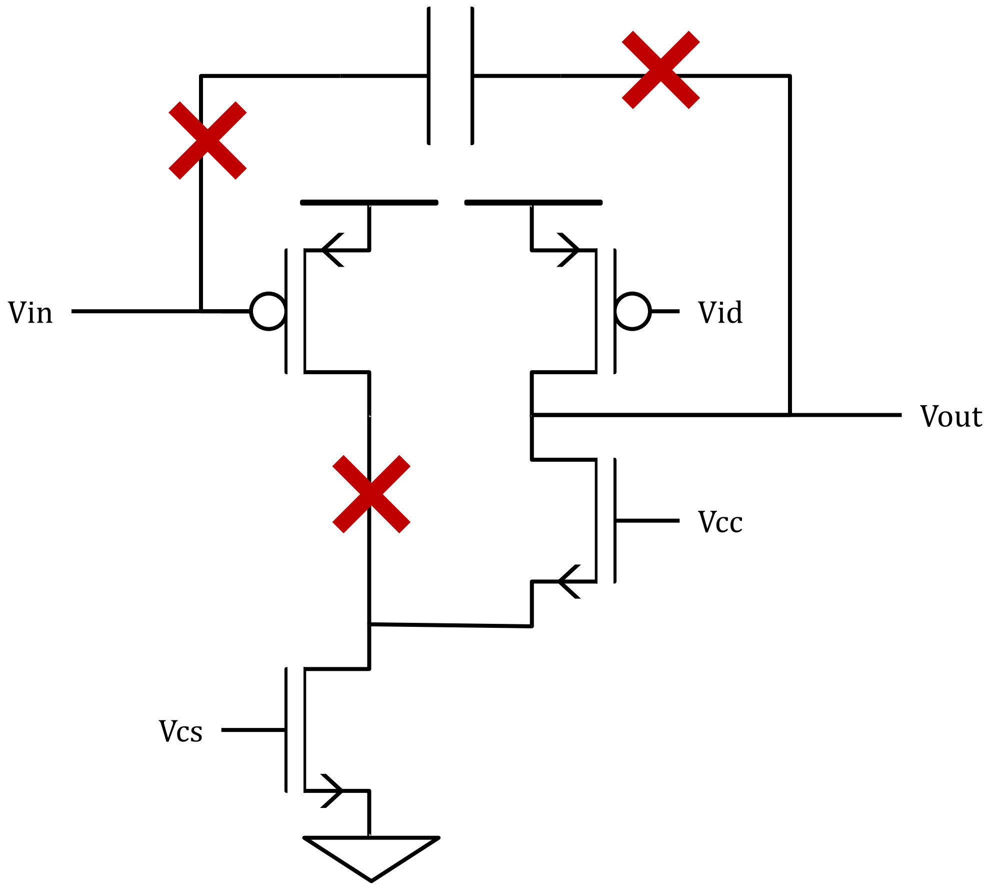
Question: Where To Cut?

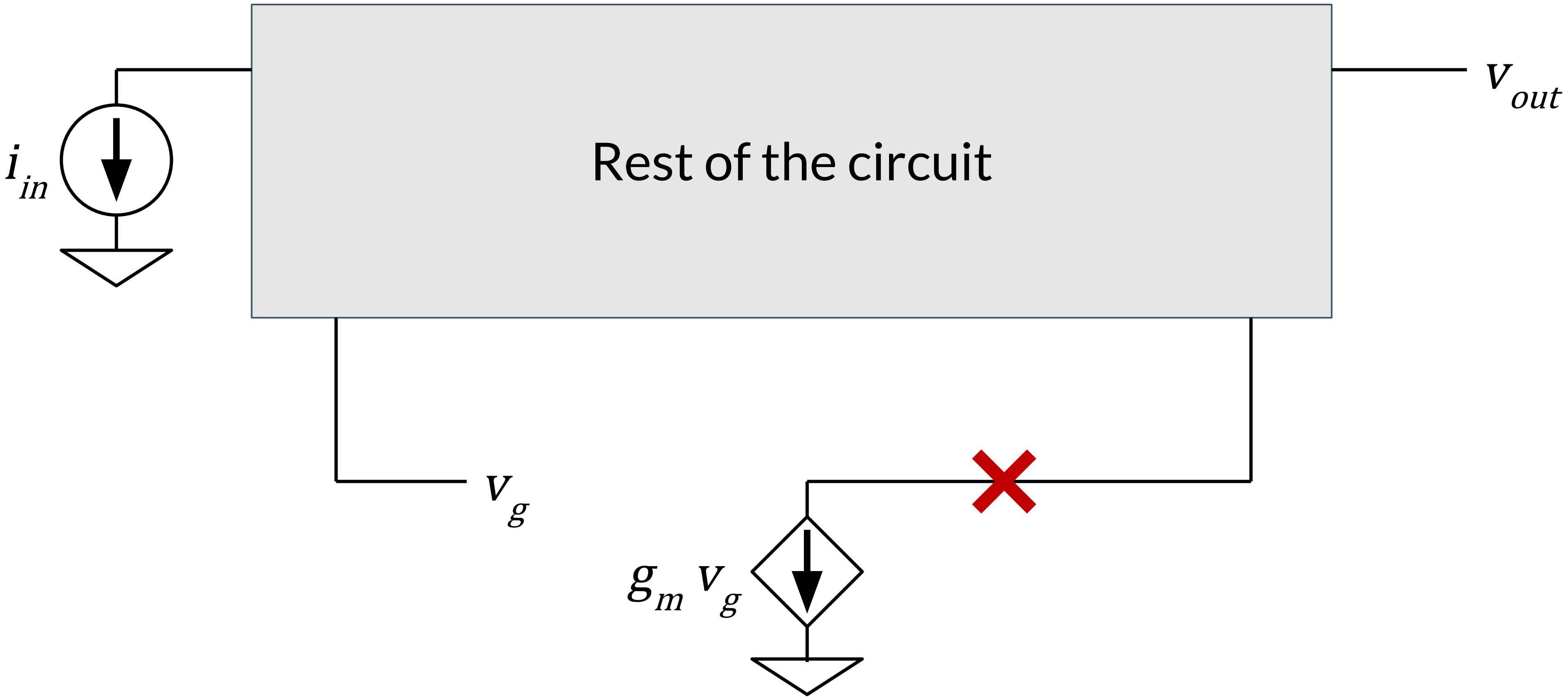
The Extra Element Theorem, found by Robert Middlebrook, let's us cut the circuit *anywhere.*

However, this theorem is complicated and requires multiple computations.



Insight: Cut After A Controlled Current Source

If we make the cut after a VCVS, the math becomes a lot easier.

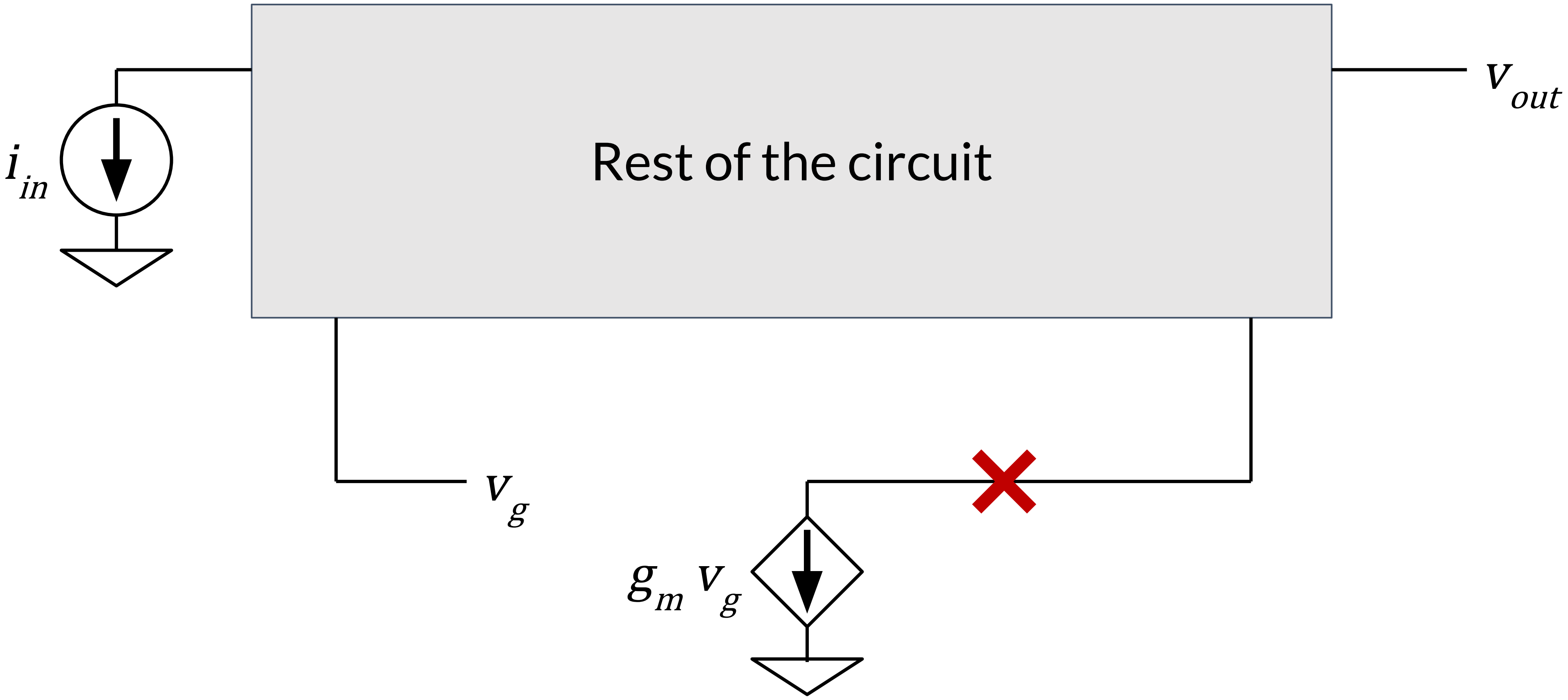


AC Analysis And Feedback

The Rosenstark Feedback Formula

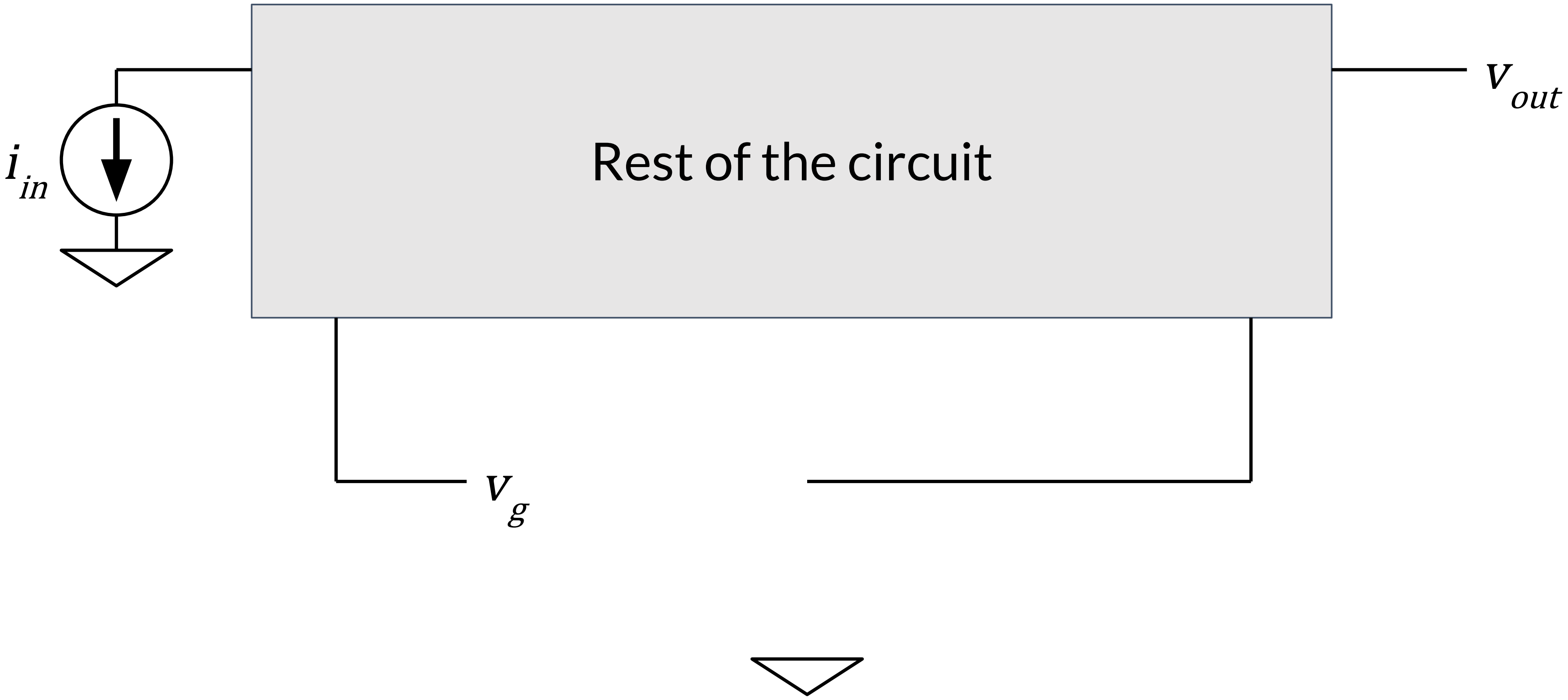
We Need To Define Three Terms

G_0 G_∞ L



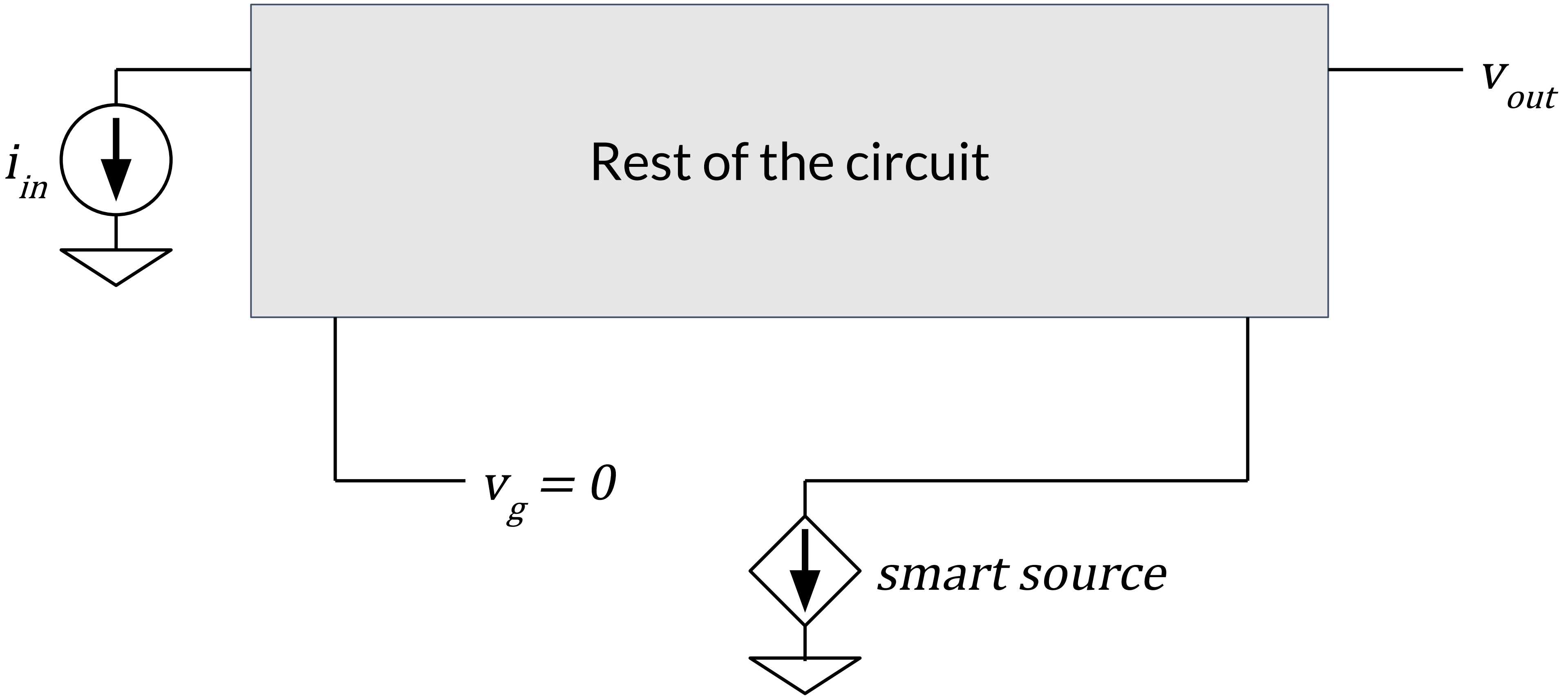
The Gain With No Transconductor G_0

$$G_0 = \frac{v_{out}}{i_{in}}$$



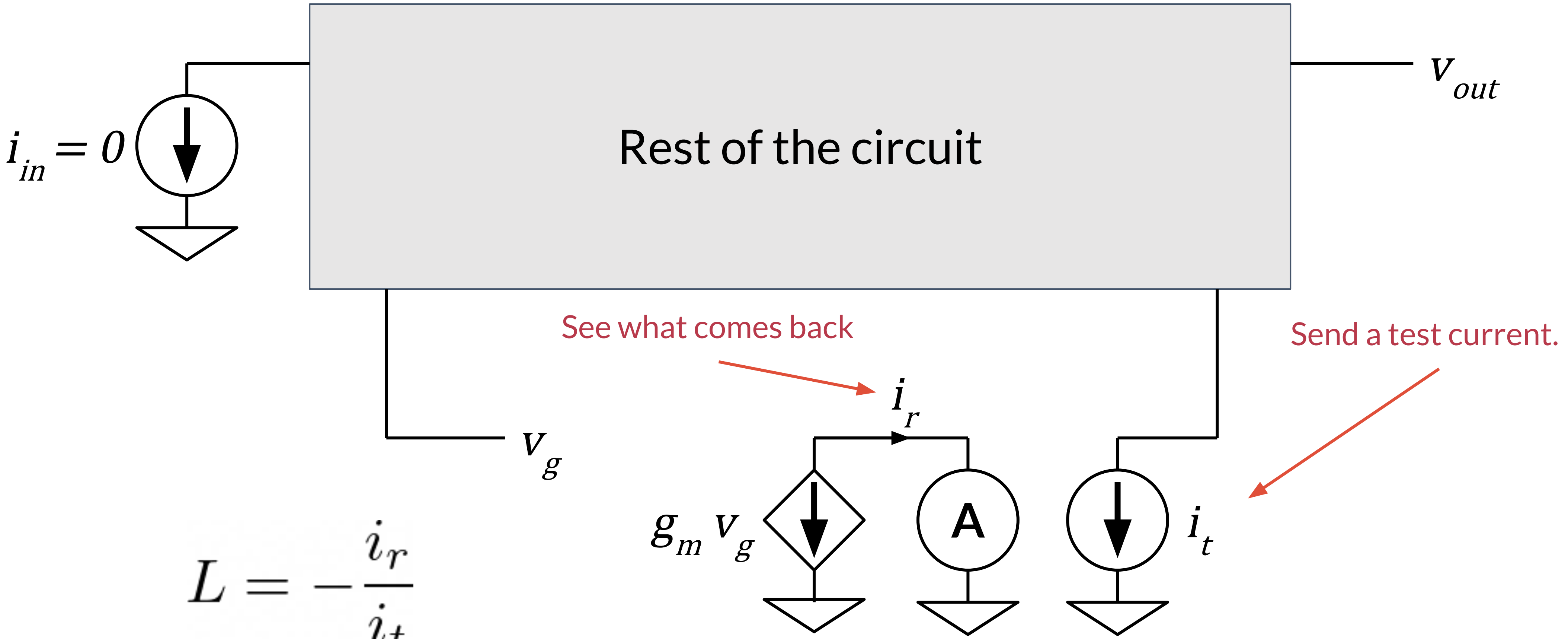
The Ideal Gain G_∞

$$G_\infty = \frac{v_{out}}{i_{in}}$$



The Loop Gain *L*

This is where we cut the feedback loop. Set the input to zero, send a test current, see what comes back.

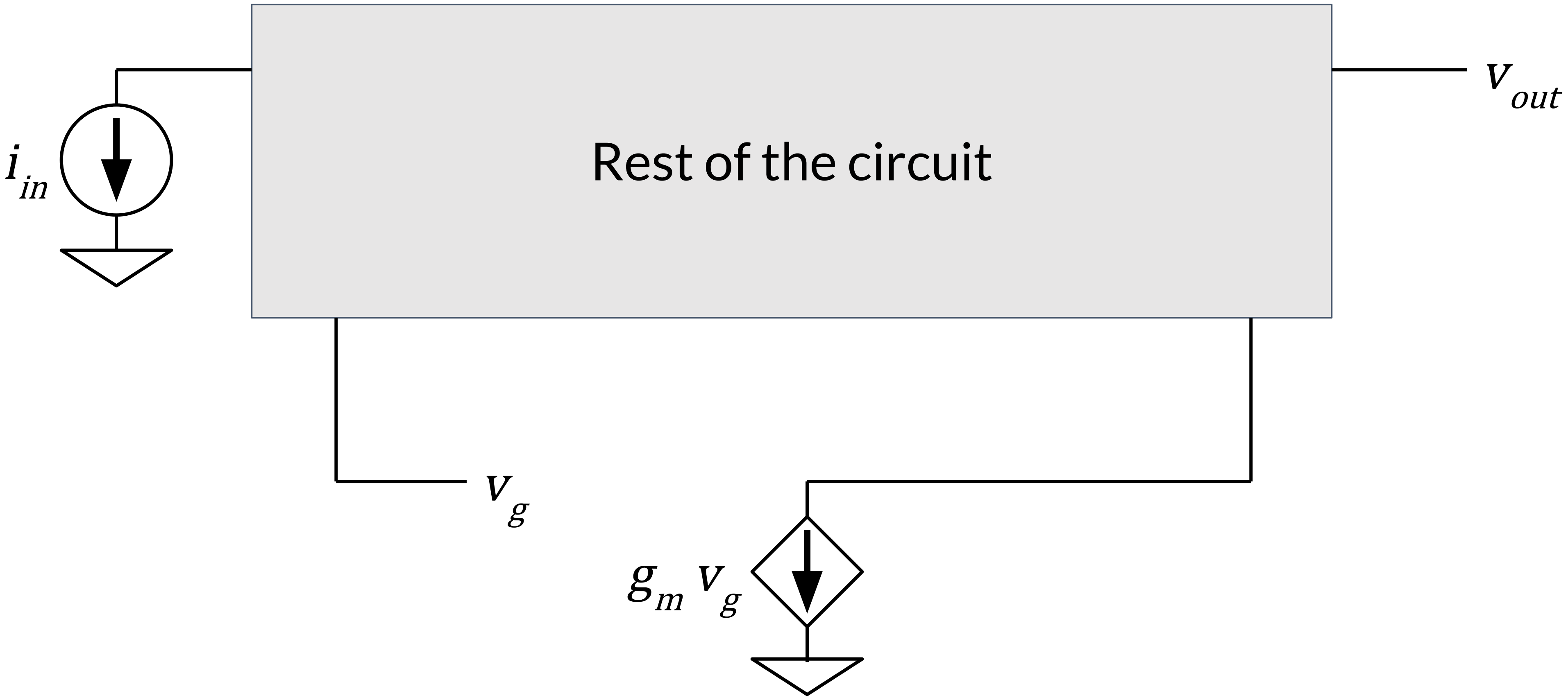


$$L = -\frac{i_r}{i_t}$$

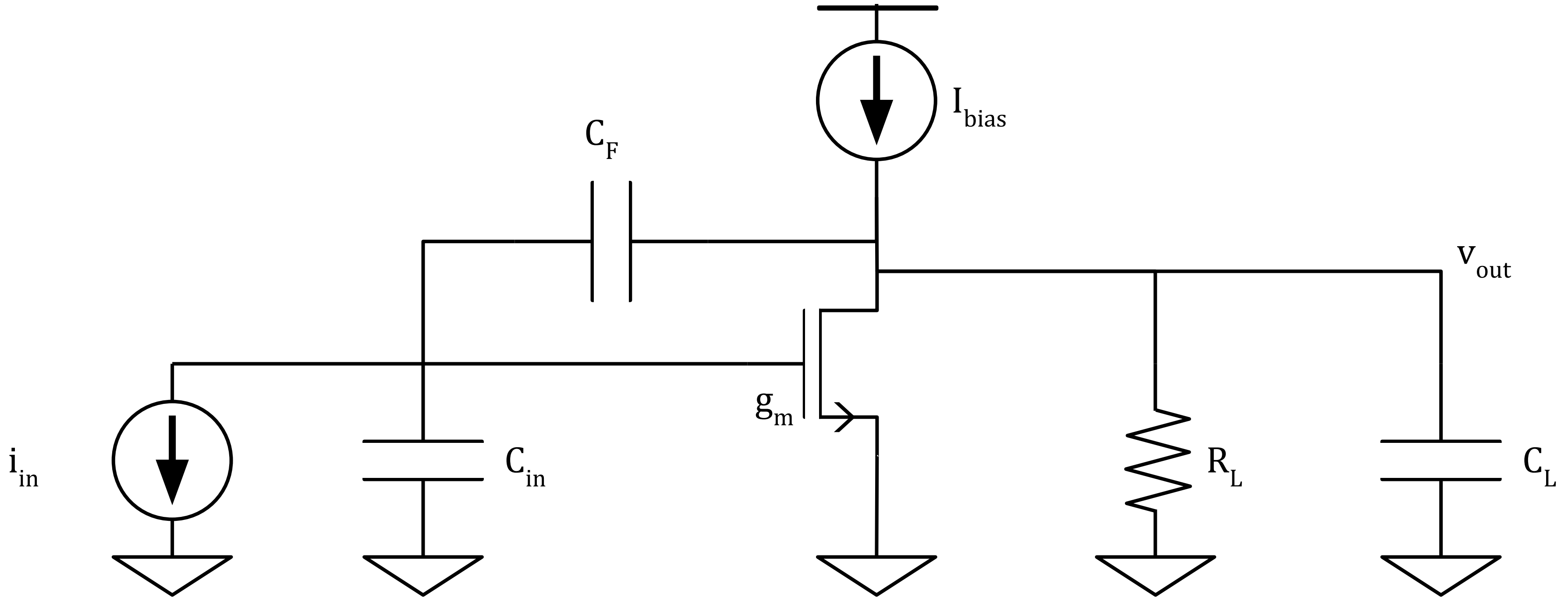
The Rosenstark Formula

$$\frac{v_{out}}{i_{in}} = G_\infty \frac{L}{1+L} + G_0 \frac{1}{1+L}$$

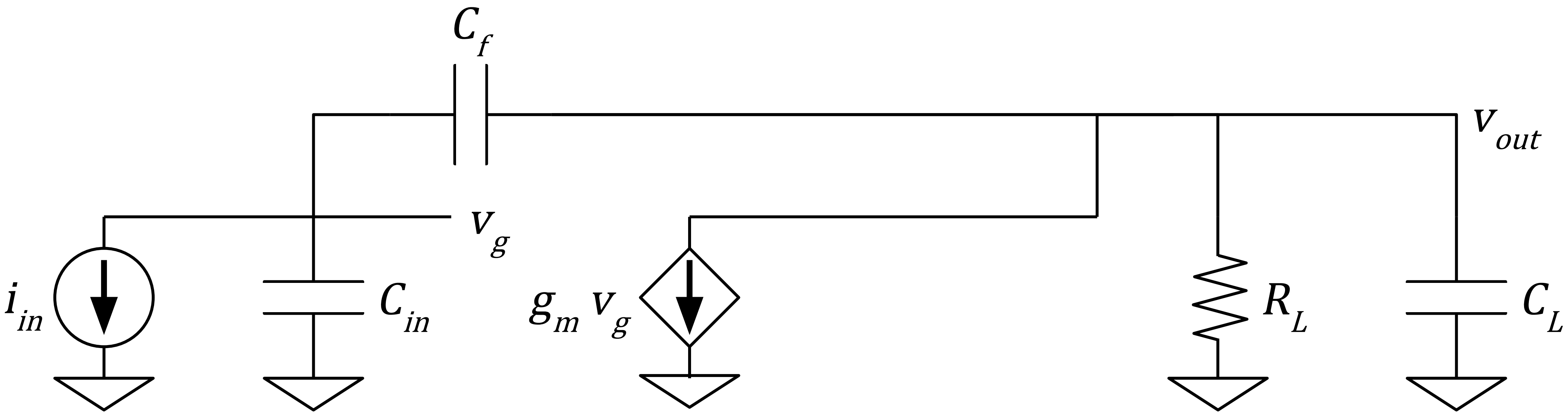
These three quantities give us the gain of the circuit



Example Walkthrough: The Single-stage CSA

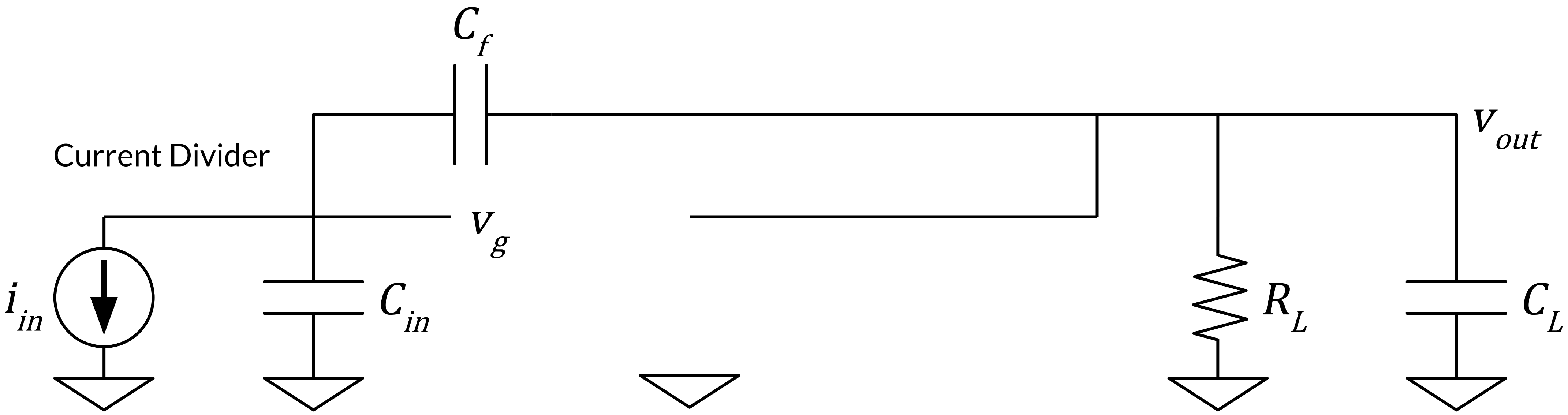


The Single-stage CSA: Small Signal Circuit

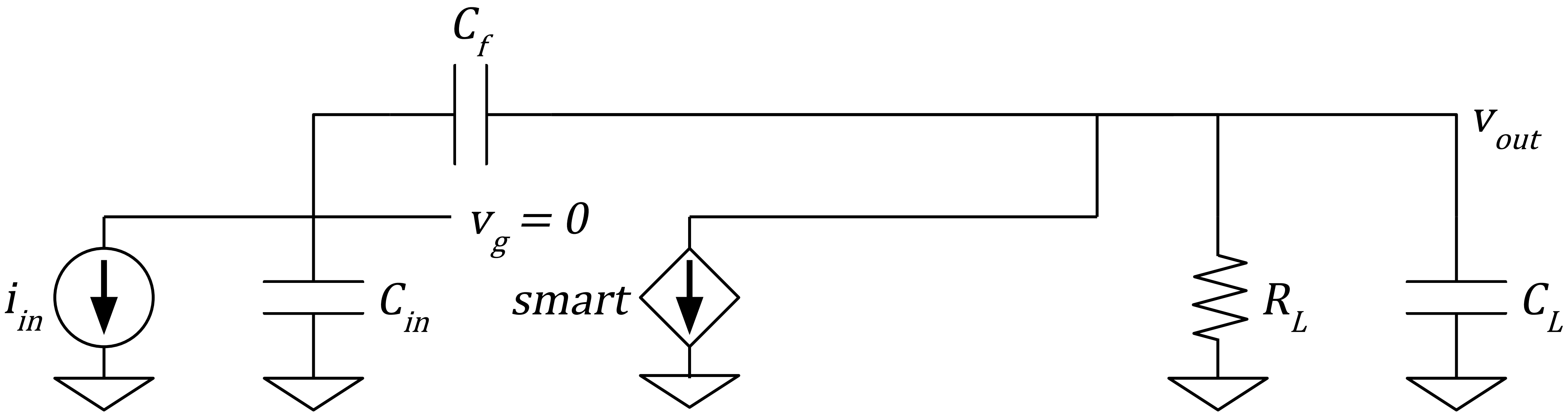


The Single-stage CSA: G_0

$$G_0 = \frac{v_{out}}{i_{in}} = \frac{R_L}{(1 + sR_LC_L)(1 + \frac{C_{in}}{C_f}) + sC_{in}R_L}$$



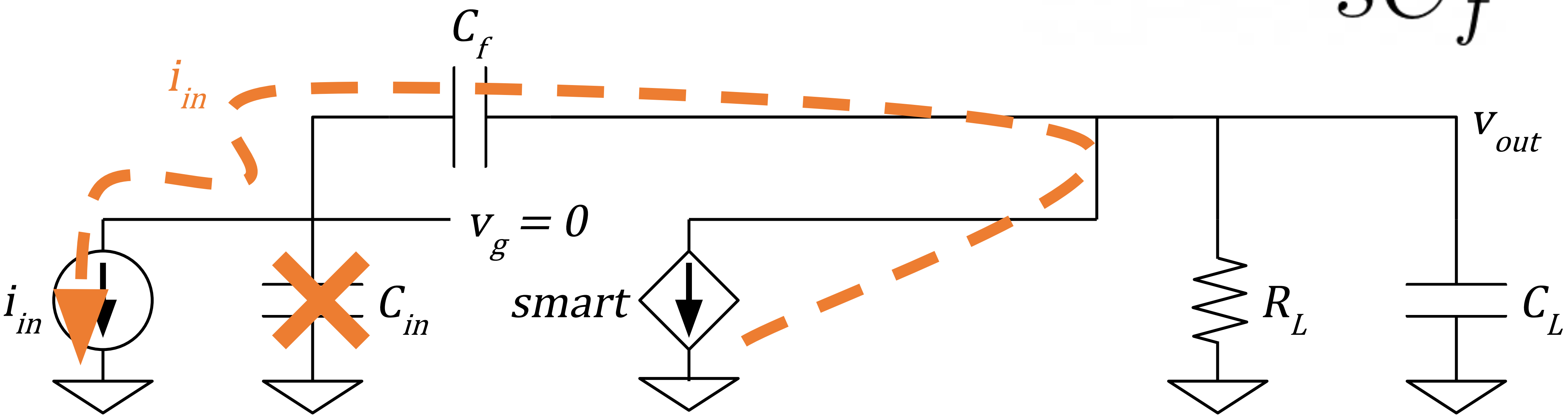
The Single-stage CSA: G_∞



The Single-stage CSA: G_∞

$$v_{out} = \frac{i_{in}}{sC_F}$$

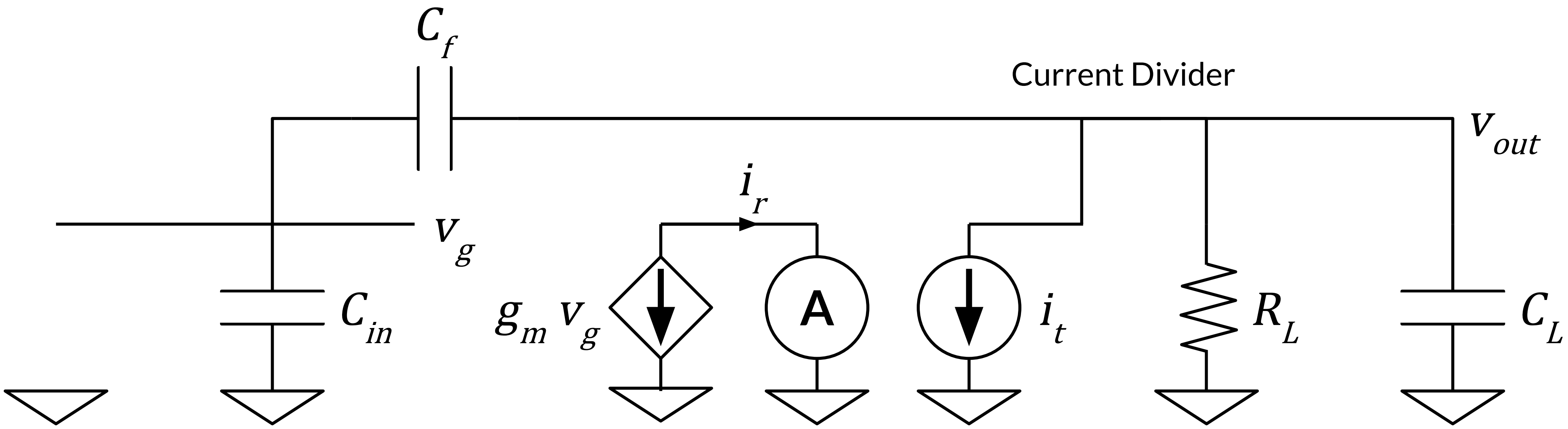
$$G_\infty = \frac{1}{sC_f}$$



The Single-stage CSA: L

$$L(s) = \frac{R_L}{1 + sR_L C_{Ltot}} \frac{C_F}{C_{in} + C_F} g_m$$

$$C_{Ltot} = C_L + \frac{C_F C_{in}}{C_F + C_{in}}$$



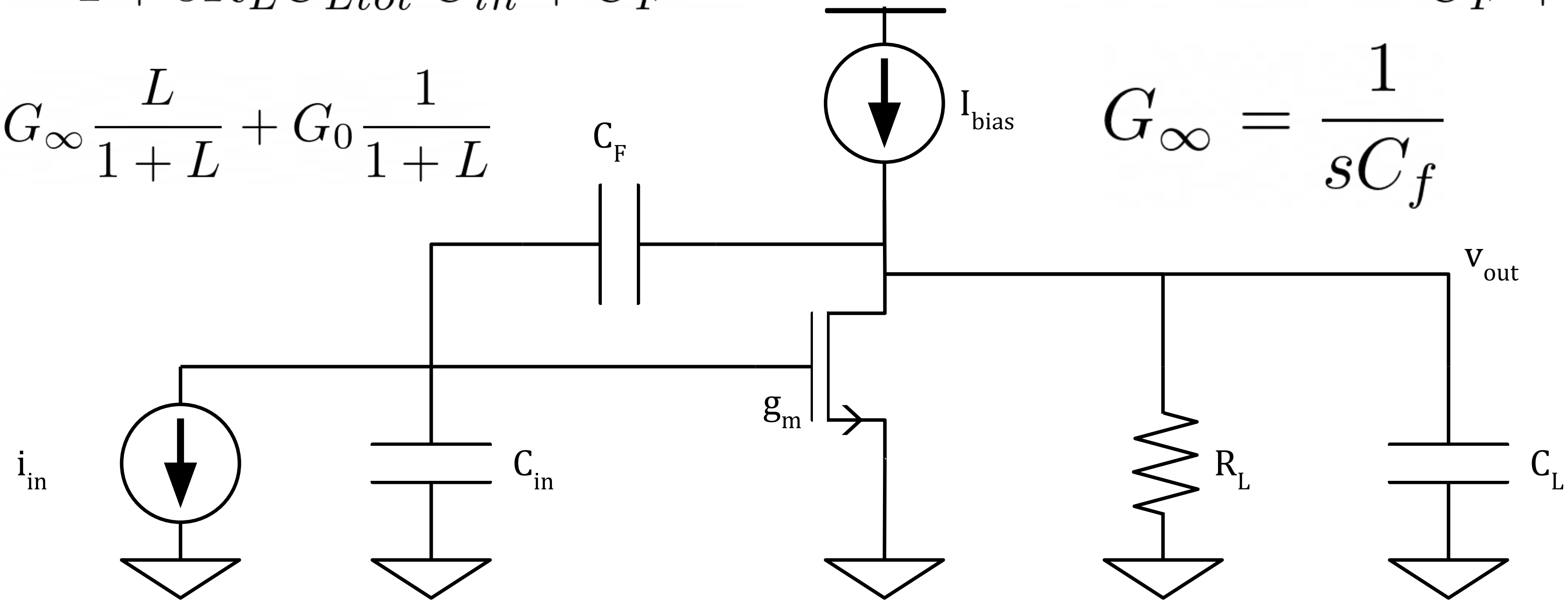
The Single-stage CSA: The Result

$$L(s) = \frac{R_L}{1 + sR_L C_{Ltot}} \frac{C_F}{C_{in} + C_F} g_m$$

$$C_{Ltot} = C_L + \frac{C_F C_{in}}{C_F + C_{in}}$$

$$\frac{v_{out}}{i_{in}} = G_\infty \frac{L}{1+L} + G_0 \frac{1}{1+L}$$

$$G_\infty = \frac{1}{sC_f}$$



$$G_0 = \frac{v_{out}}{i_{in}} = \frac{R_L}{(1 + sR_L C_L)(1 + \frac{C_{in}}{C_f}) + sC_{in} R_L}$$

SLAC

AC Analysis And Feedback

Intuition With The Rosenstark Formula

The Full Rosenstark Formula

$$\frac{v_{out}}{i_{in}} = G_\infty \frac{L}{1+L} + G_0 \frac{1}{1+L}$$

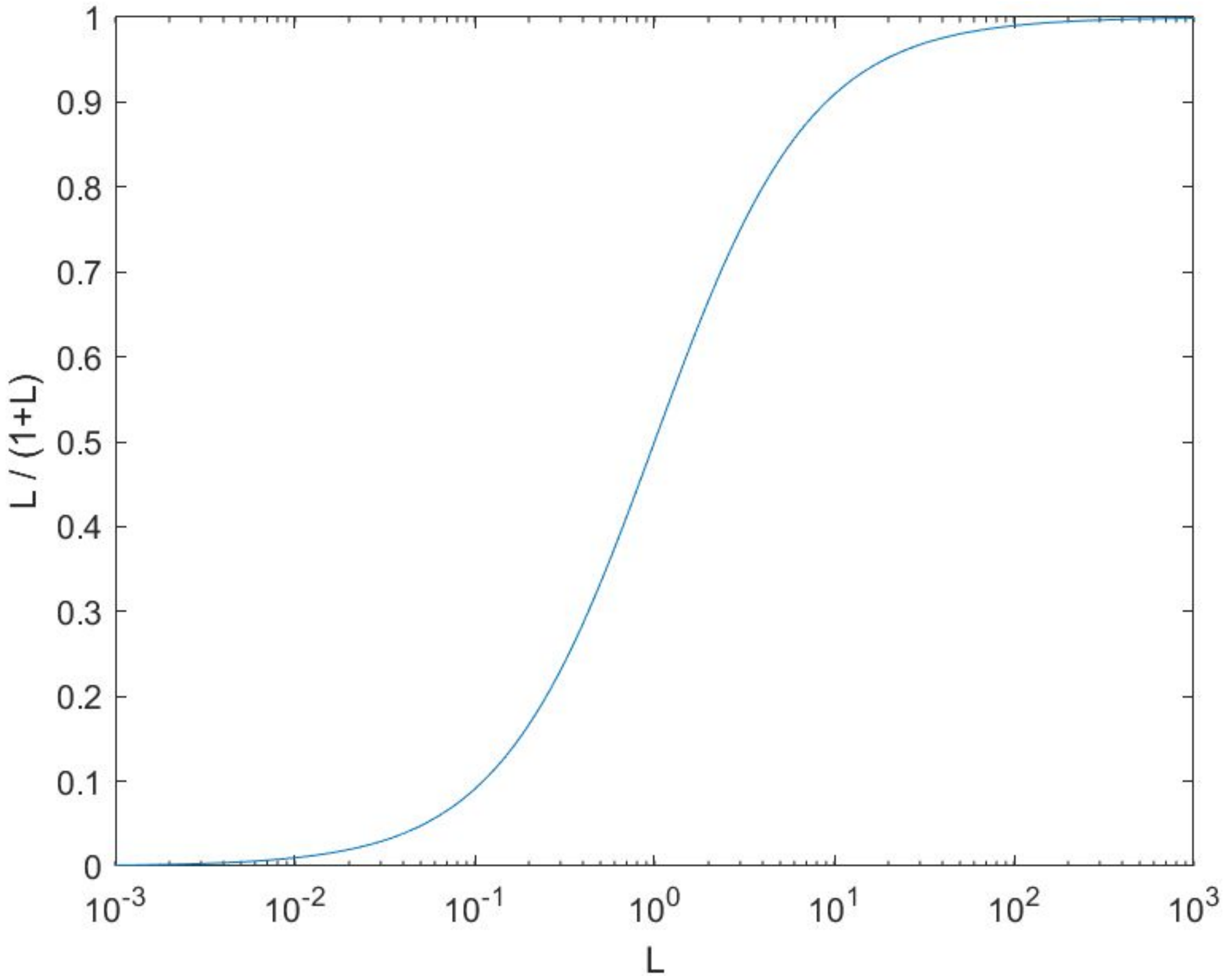
Typically, G_0 / (1+L) is very small

$$\frac{v_{out}}{i_{in}} = G_\infty \frac{L}{1+L} + G_0 \frac{1}{1+L}$$

$$\frac{v_{out}}{i_{in}} \approx G_\infty \frac{L}{1+L}$$

Let's Plot L/(1+L)

We notice that L/(1+L) = 1 for L > 1



Interpretation

$$\frac{v_{out}}{i_{in}} \approx G_{\infty} \frac{L}{1+L}$$

implies

$$\frac{v_{out}}{i_{in}} \approx G_{\infty}$$

as long as

$$L \gg 1$$

Result

The gain is set by:

$$\frac{v_{out}}{i_{in}} \approx G_{\infty}$$

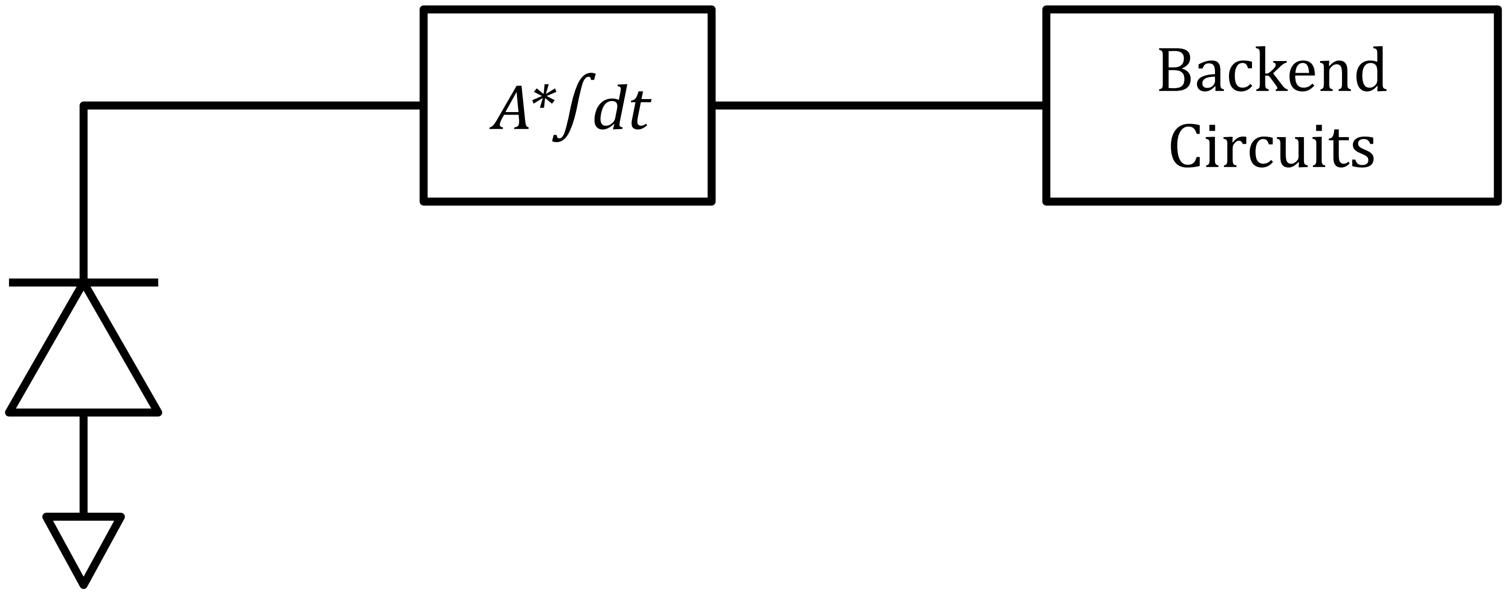
The bandwidth is set by:

$$\left| L\left(j\omega_{3dB}\right)\right| = 1$$

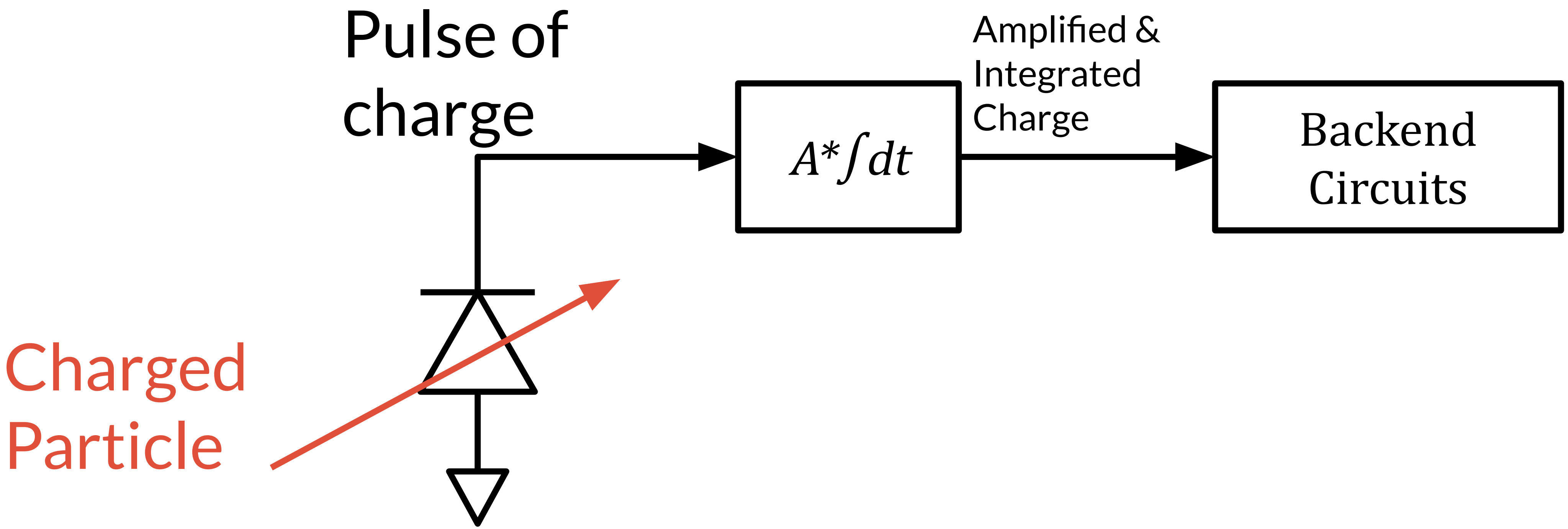
AC Analysis And Feedback

Charge-sensitive amplifiers and diode readouts

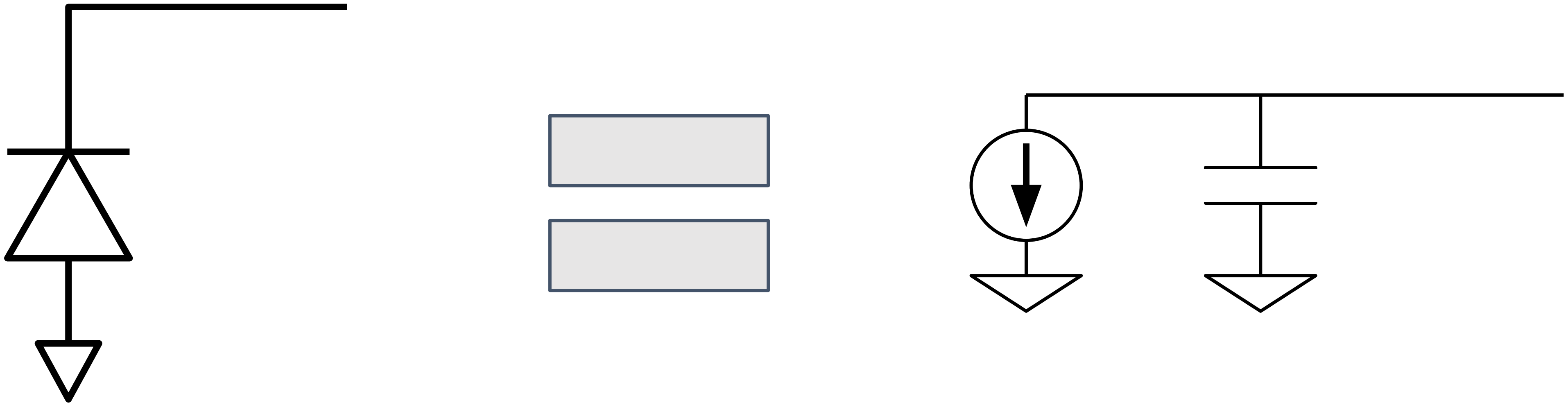
What have we been working towards?



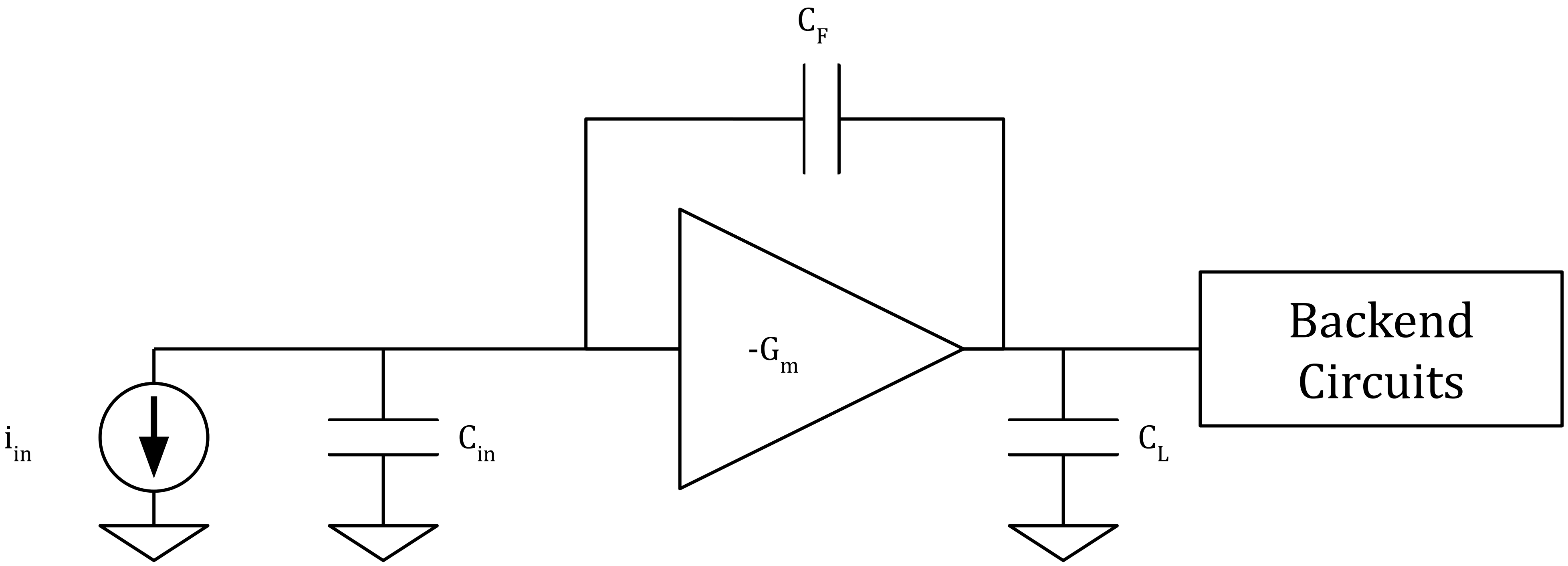
What have we been working towards?



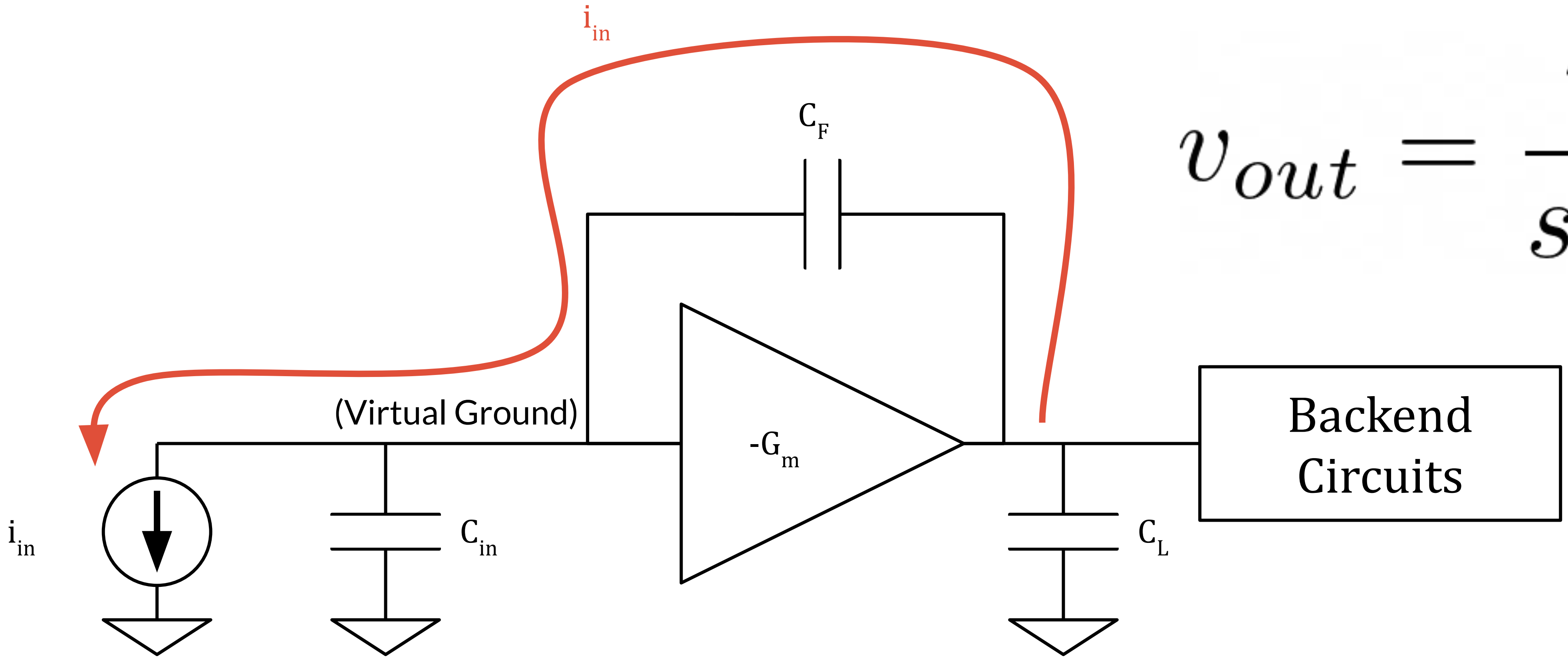
How does a particle sensor look like?



The full Charge-Sensitive Amplifier (CSA) system

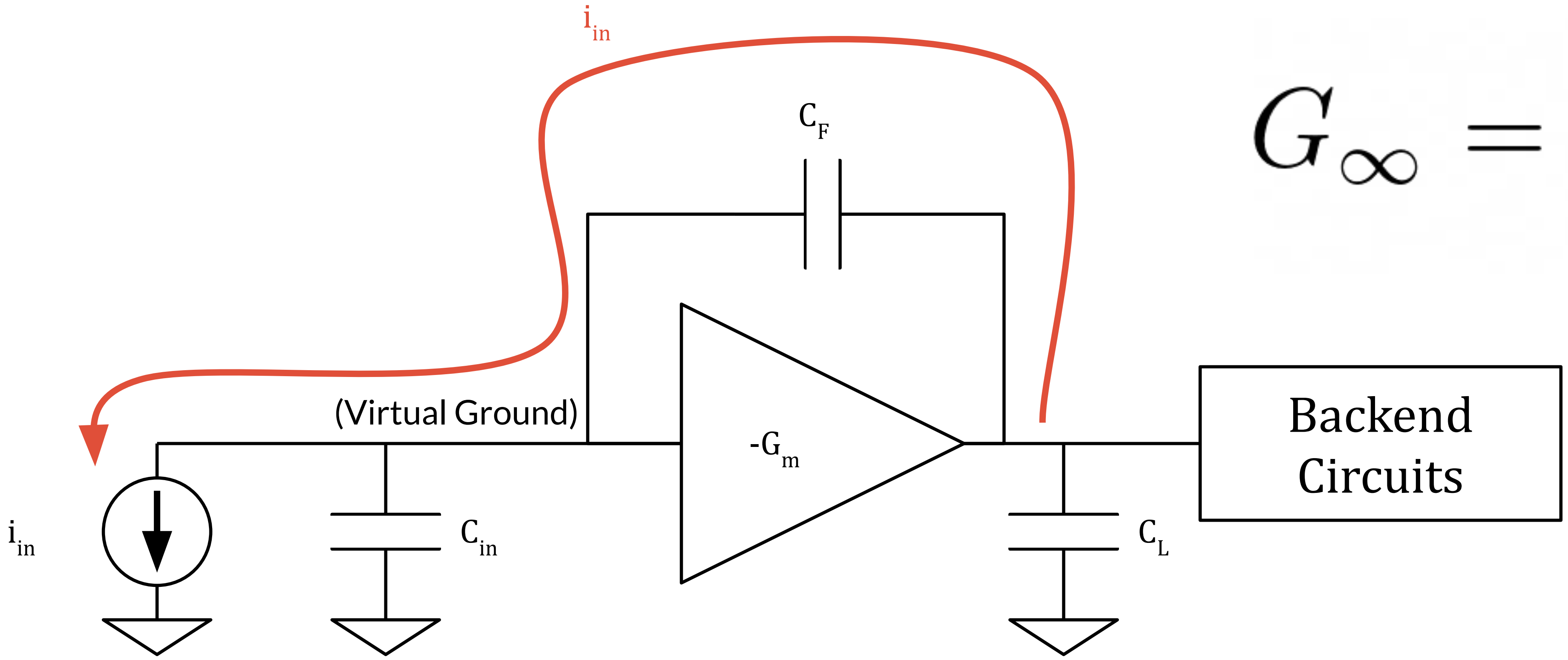


Ideal CSA with G_∞



$$v_{out} = \frac{i_{in}}{sC_F}$$

Ideal CSA with G_∞



$$G_\infty = \frac{1}{sC_f}$$

We are ready to give the full CSA specs

- Diode **Input Capacitance: 100fF**
- Max processing time 7us → **Settling time at ε_d=0.01% <100ns** → Bandwidth > 15MHz
- Max signal 25fC, Max output swing of 1V → **Gain 40mV/fC**
- **Static Error: ε_S < 0.1%**
- **Input-Referred Noise: <150e-**
- Use minimum current consumption (max 12uA)

Dynamic Error: At what fraction of the final output do we consider the input fully settled?

$$\epsilon_s = \frac{L(0)}{1 + L(0)}$$

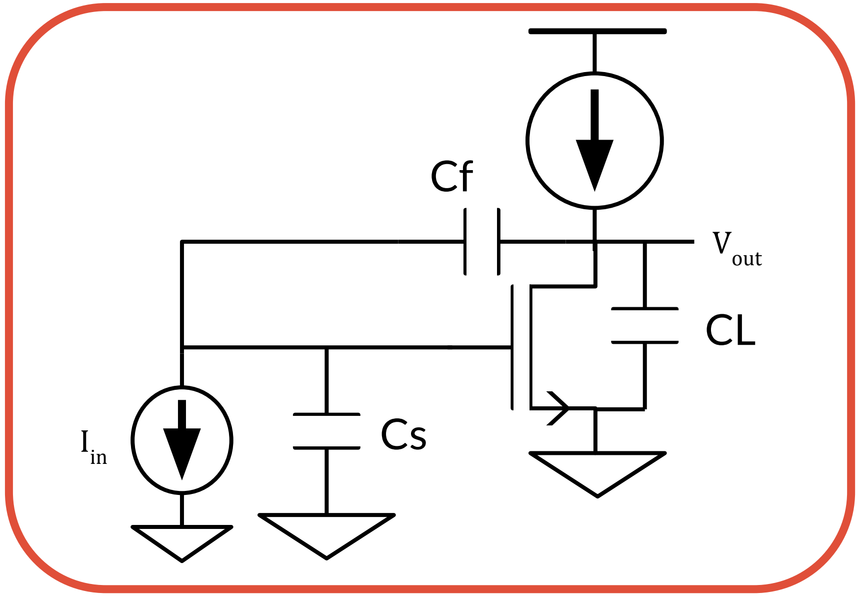
$$f_{3dB} = \frac{1}{2\pi\tau} = \frac{\ln(1/\epsilon_d)}{2\pi t_S}$$

Static Error: How far does the closed-loop gain deviate from just an ideal C_F at DC?

Task: Designing intrinsic CSA Amplifier

Part 3: Intrinsic Gain Stage with feedback

- Id< 12uA
- Cs=100fF
- CL=250fF
- Max signal 25fC / Max signal output swing 1V
  - Cf = 25fC/1V
- Size Cgs=0.1(Cf+Cs)
- Goals:
  - Gain-Bandwidth Product: >16MHz
  - Maximize Gain
  - Determine what is the minimum static error you can reach



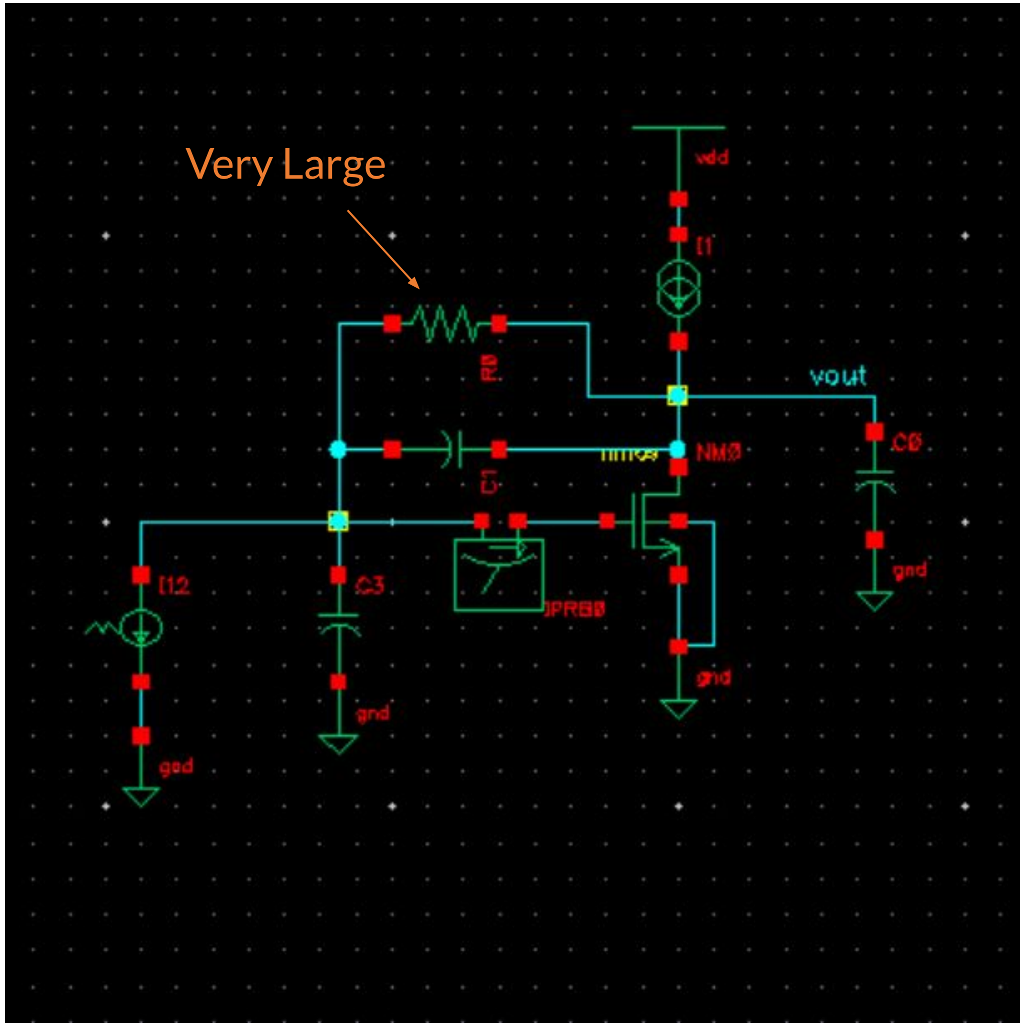
Methodology:

1. By hand: derive Loop gain in terms of gm, gds then derive the expression of the pole and the GBW product
2. Calculate the minimum gm then pick a value of gm/Id compatible with power constraints.
3. Pick an appropriate L to achieve maximum gain.
4. Given gm/Id and L, we've fixed, fT and Id/W.
5. Using Id/W, find the needed W.
6. Run a simulation (check stability)

$$\epsilon_s = \frac{L(0)}{1 + L(0)}$$

Sample Implementation

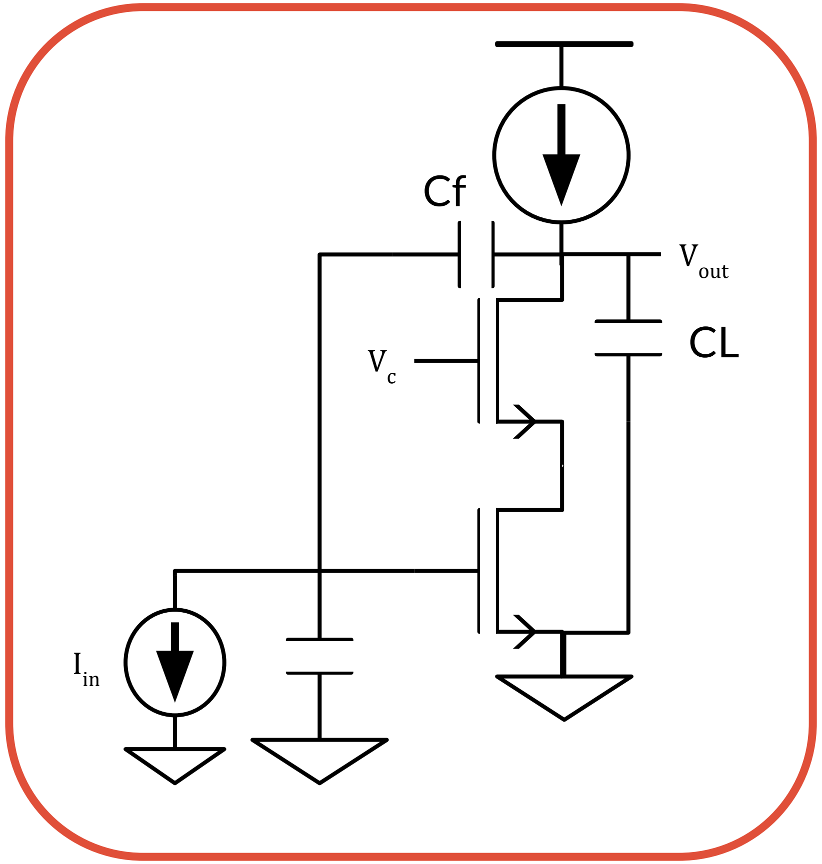
Feedback resistor used to set DC bias only



Task: Designing a CSA Amplifier (ideal load)

Part 4: Cascoded Stage

- Id< 12uA
- Cs=100fF
- CL=250fF
- Max signal 25fC / Max signal output swing 1V
  - Cf = 25fC/1V
- Size Cgs=0.1(Cf+Cs)
- Goals:
  - Gain-Bandwidth Product: >16MHz
  - Determine what is the minimum static error you can reach



Methodology:

- Simply add a cascode with the same dimensions of the input transistor
- Derive the equations
- Run a simulation (check stability)

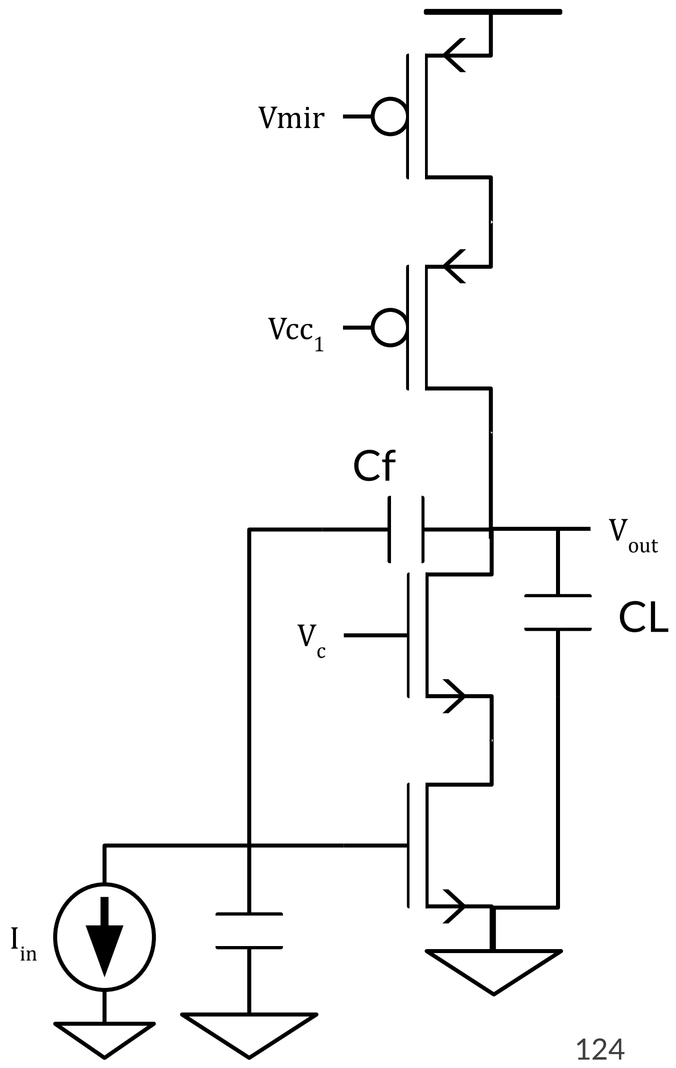
Task: Designing a CSA Amplifier (active load)

Part 5: Cascoded Stage

- Id< 12uA
- Cs=100fF
- CL=250fF
- Max signal 25fC / Max signal output swing 1V
    - Cf = 25fC/1V
- Size Cgs=0.1(Cf+Cs)
- Goals:
    - Gain-Bandwidth Product: >16MHz
    - Verify that the Static error below is below 0.1%

Methodology:

- Simply add two cascode pmos (for simplicity use the same sizes of the nmos branch and mirror the current in them.
- Derive the equation for the closed loop gain
- Run a simulation (check stability)



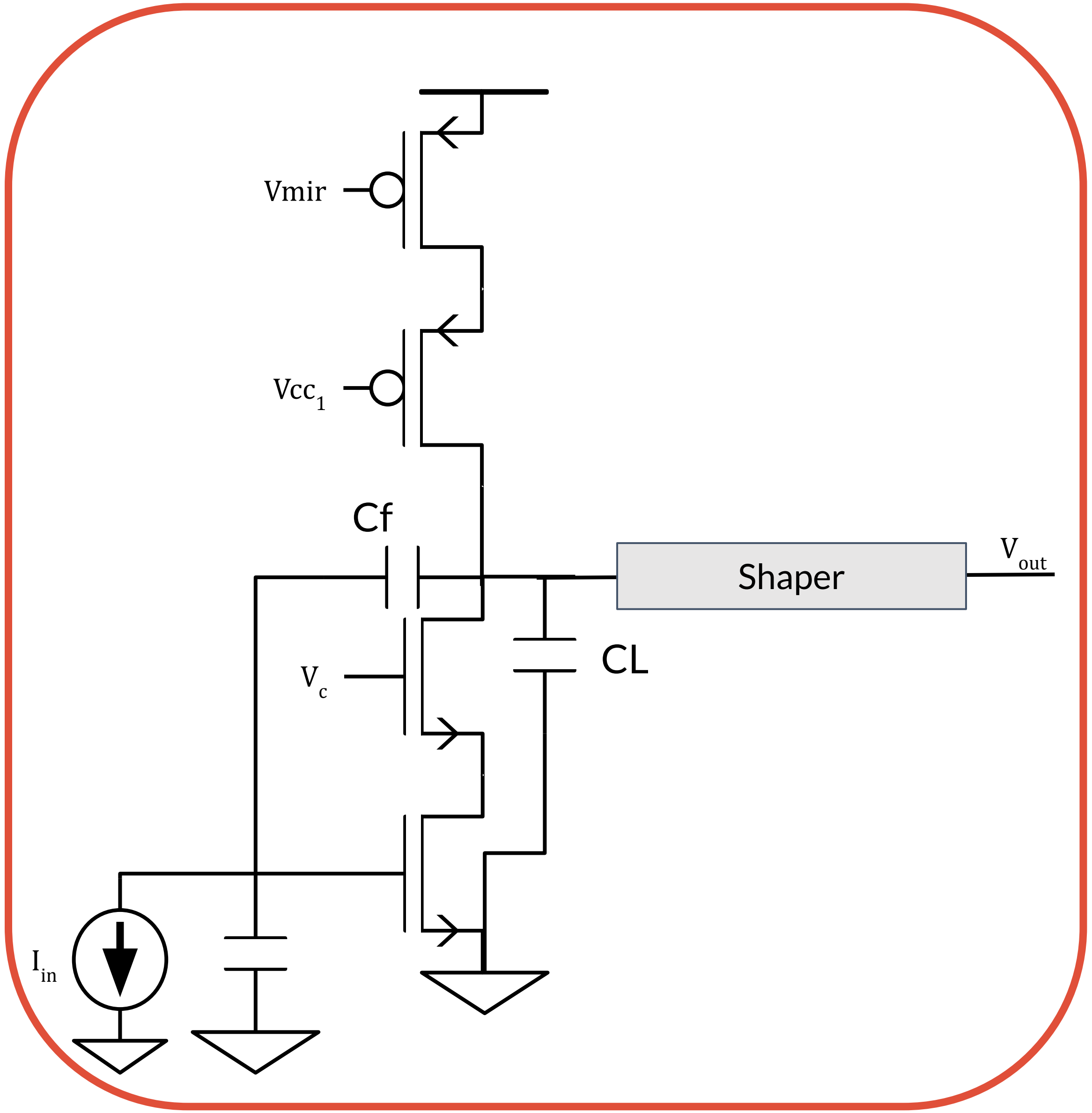
Task: Designing a CSA + Shaper

Part 6: CSA+Shaper

1. What Shaper time constant do we need to reach an ENC < 150e-?
2. Does the waveform return to 0 within 7us?

Methodology:

3. Use the ideal shaper.
4. Plot the total output noise r.m.s.
5. Calculate the ENC
6. Vary the shaper time constant until ENC <150e-



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