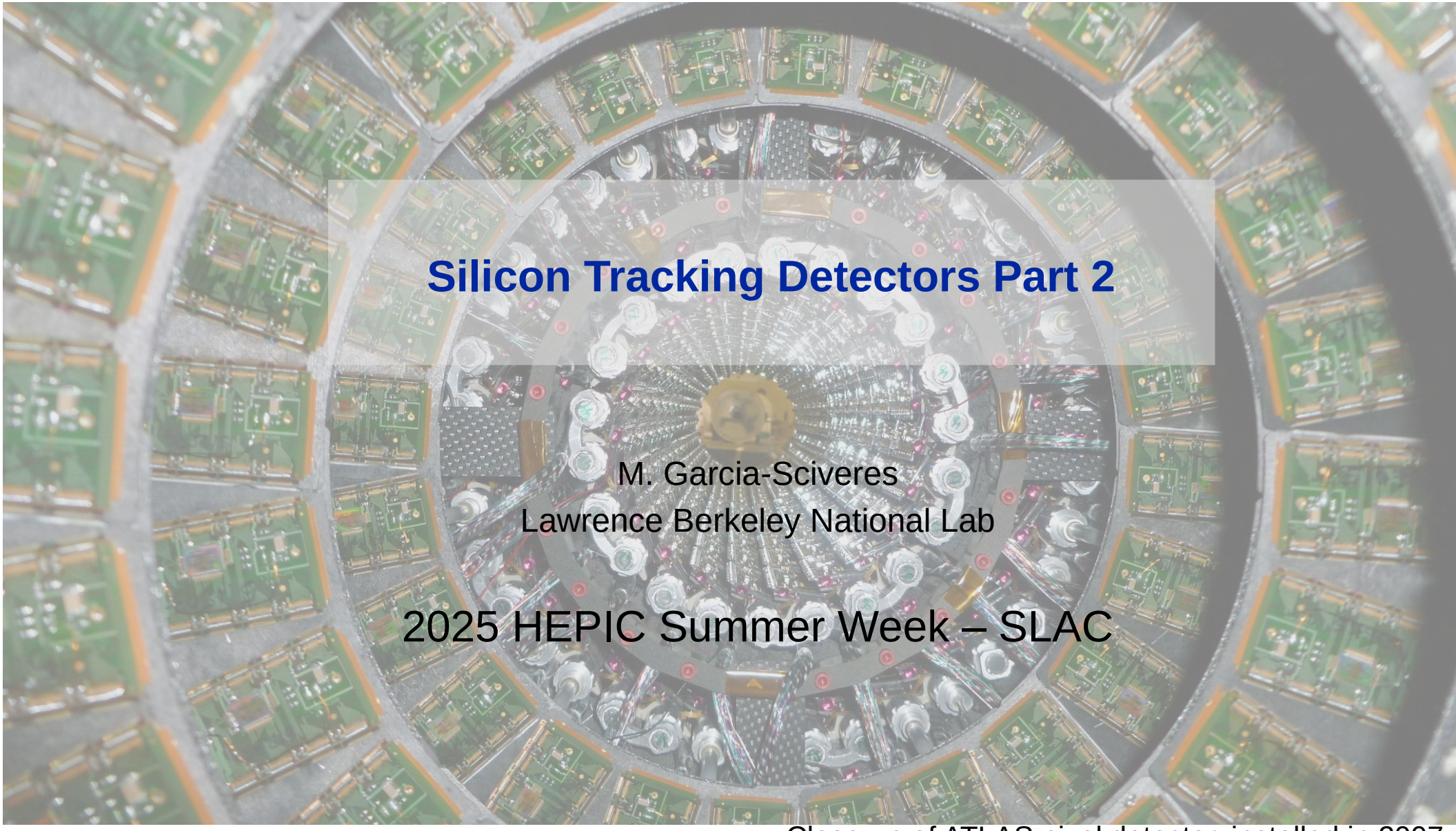
Silicon Tracking Detectors Part 2

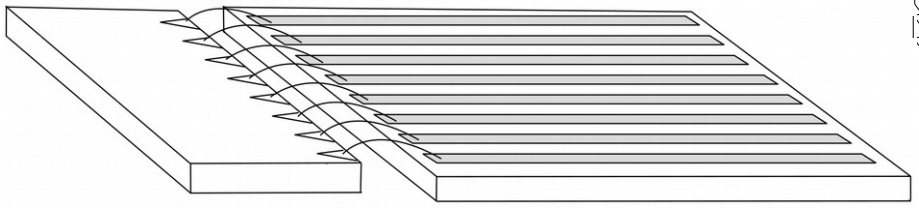
M. Garcia-Sciveres
Lawrence Berkeley National Lab

2025 HEPIC Summer Week – SLAC

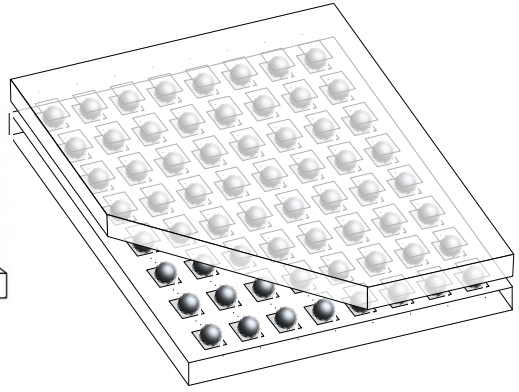


Close-up of ATLAS pixel detector, installed in 2007

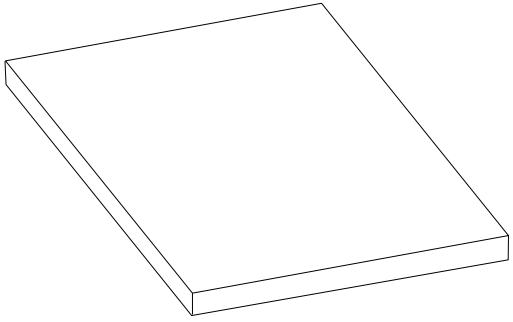
Silicon Tracker Types



Hybrid Strips

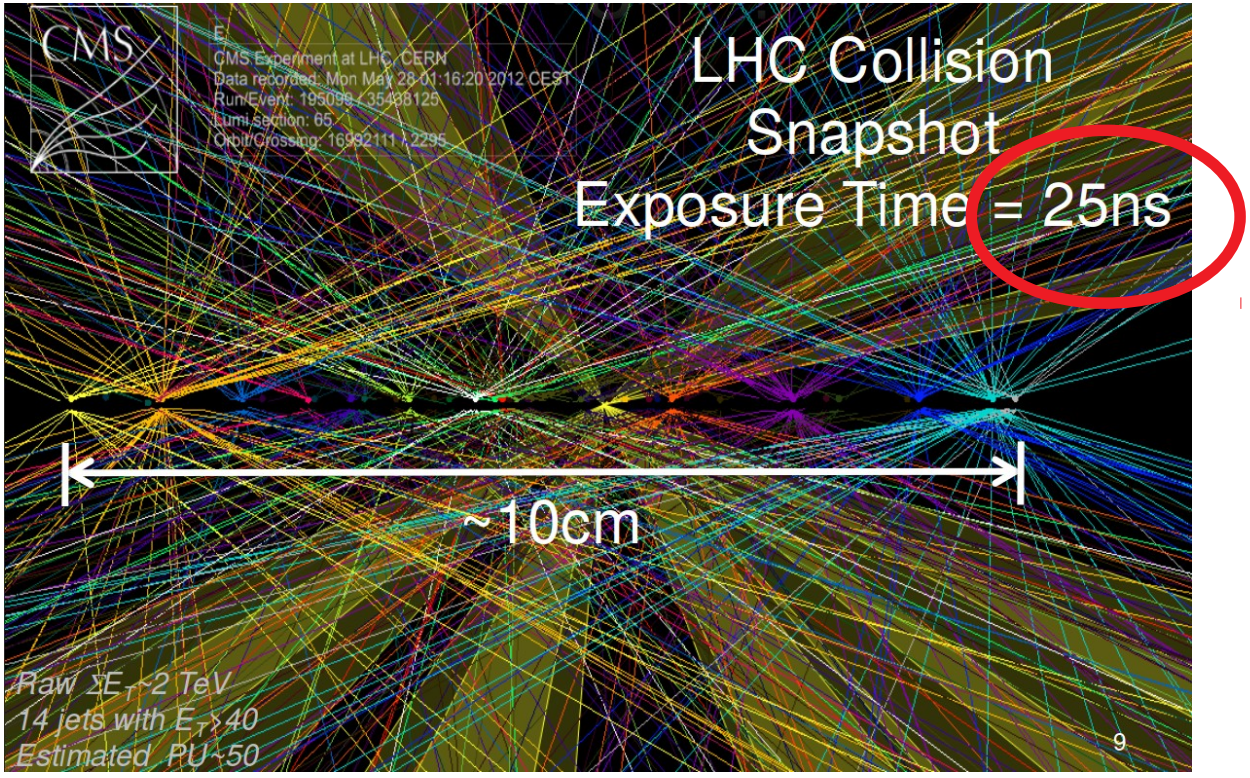


Hybrid Pixels



Monolithic

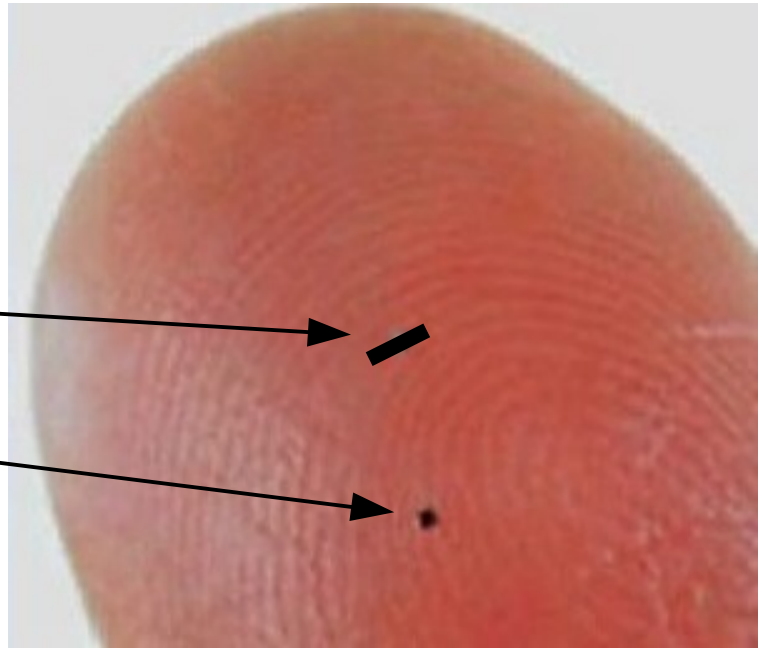
how do we handle the rate?



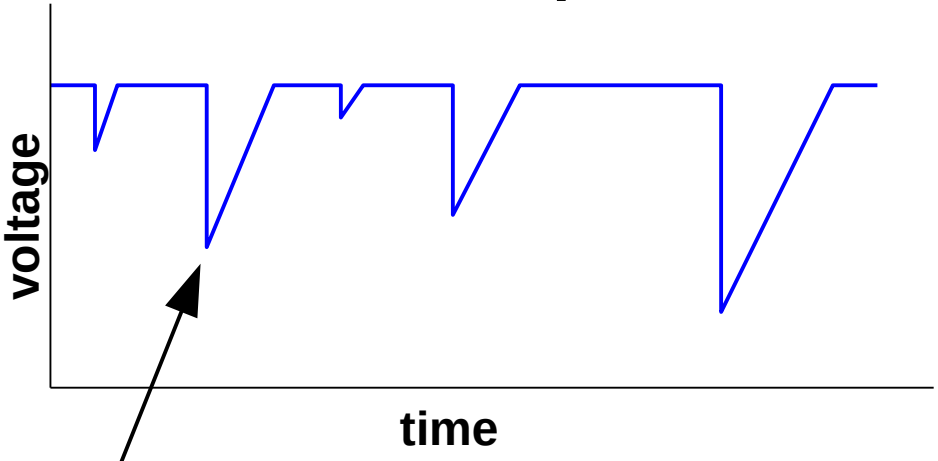
- Capturing 40M 5Gpixel images per second is not feasible.
- Triggering only saves a factor of 40 in readout
  - 1M 5Gpixel images per second is still far from feasible
- A: We do NOT do conventional image capture.
- We treat every pixel as an independent, free-running detector and store it's output (heavily redacted)

Single Pixel Perspective

Pixel size



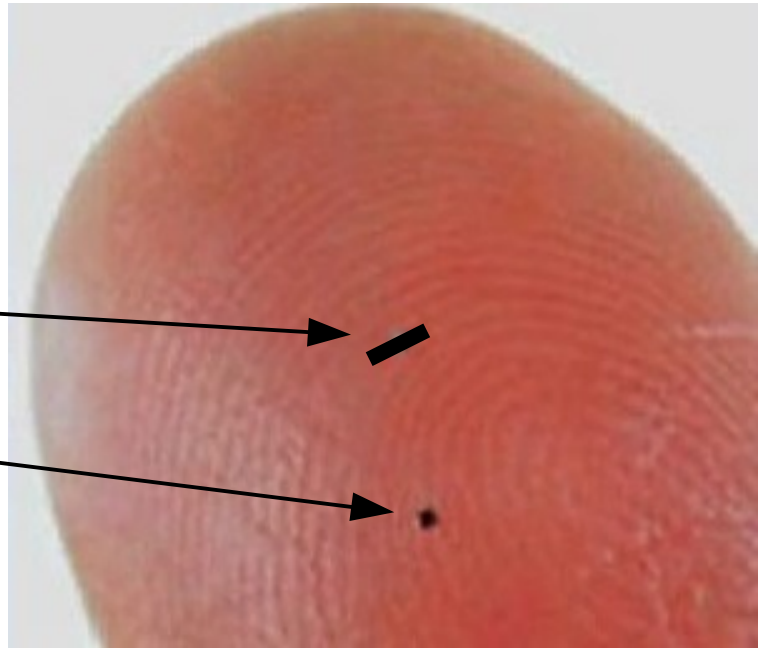
Pixel output



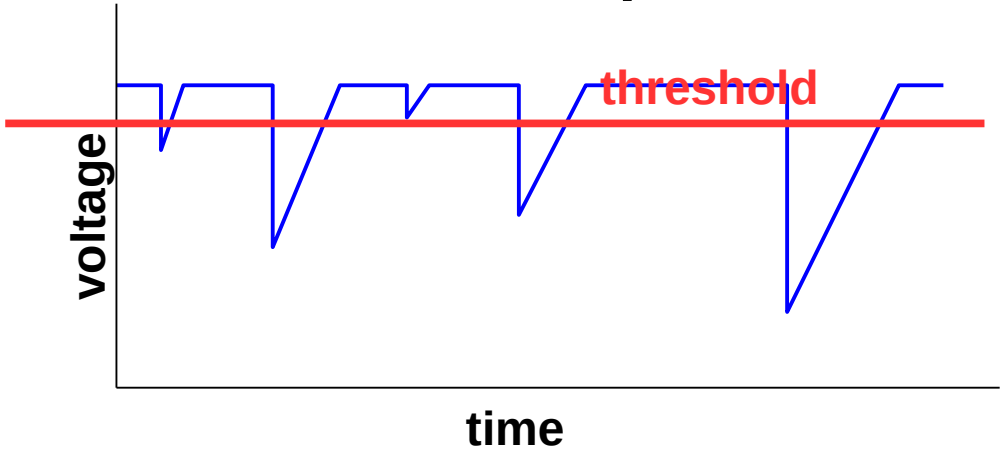
Hits
~50 kHz
(not too bad compared to 40 MHz)

Single Pixel Perspective

Pixel size

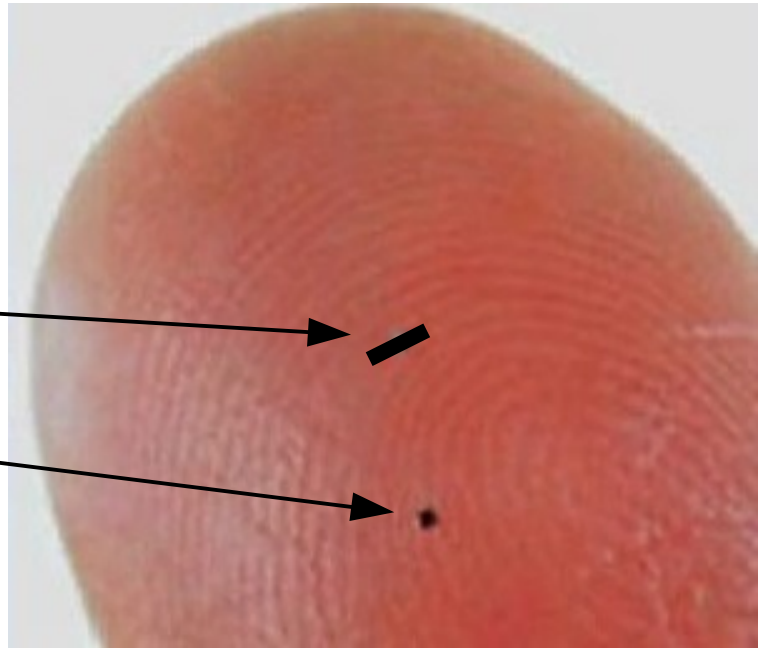


Pixel output

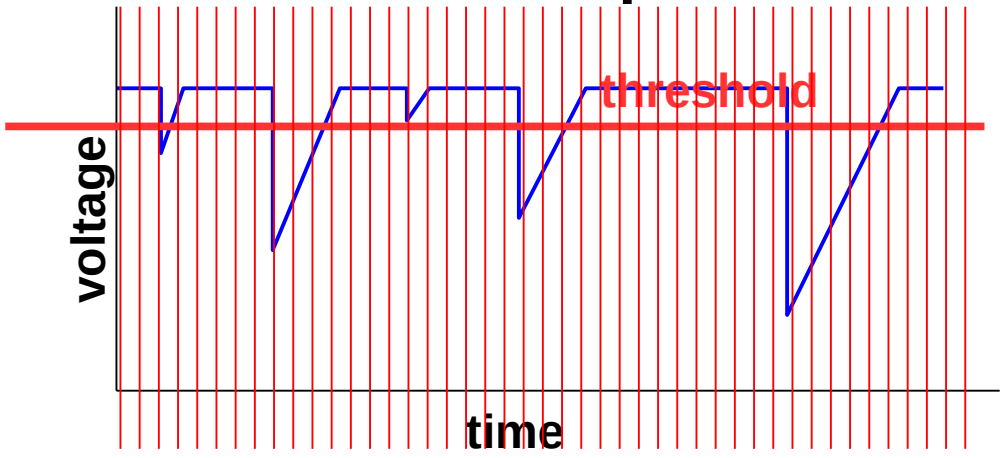


Single Pixel Perspective

Pixel size



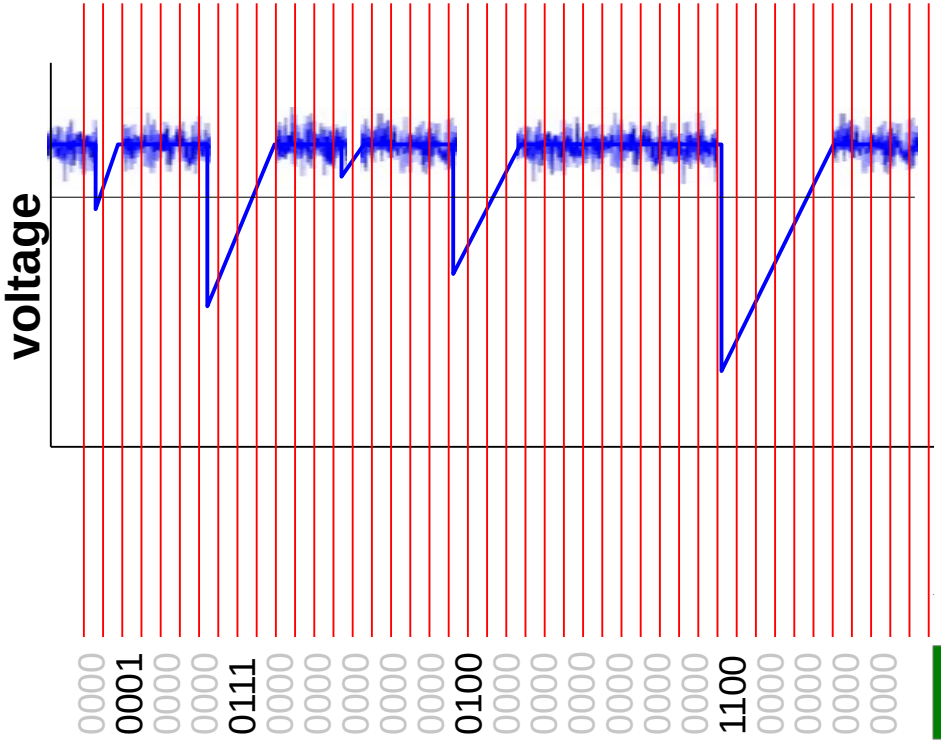
Pixel output



Bunch crossings

Digitize amplitude above threshold in each Bunch Crossing

On-Chip Storage and Trigger



On-chip memory ("FIFO")

Readout ~Gbps

Storage of all individual hits W/ ADC value (~40 Gbps for a 100Kpx chip)

Triggers (select 1/40 time slices)

A chip is storing 40Gbps?

High rate pixel readout chips are memories (in addition to being pixel readout chips)

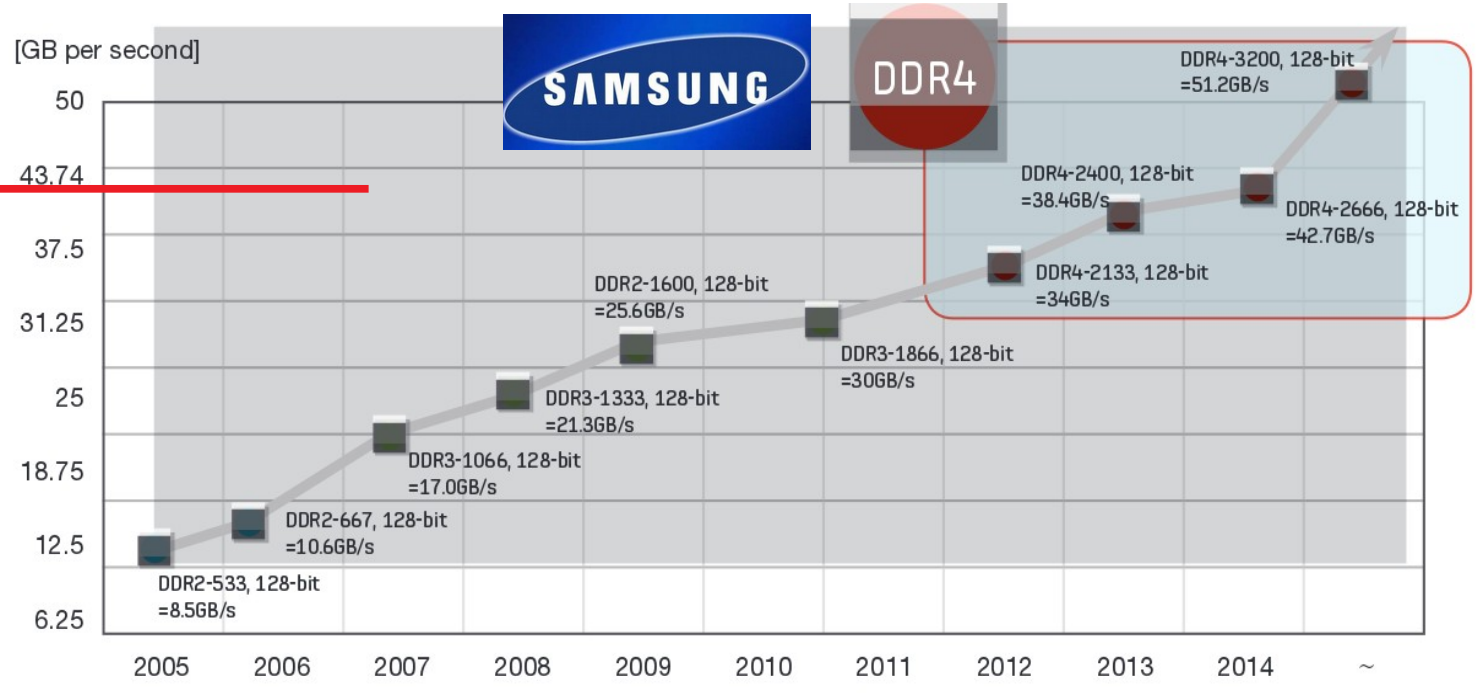


Figure 2. DDR4 higher performance compared with DDR3L and DDR2

Plot is for a memory module containing 8 silicon chips so B = b

(and this is not rad hard)

Silicon Detectors at Colliders

(and in orbit)

Fermi LAT

Strip Detectors

1980	NA1
1981	NA11
1982	NA14
1990	MarkII
1990	DELPHI
1991	ALEPH
1991	OPAL
1992	CDF SVX
1993	L3
1996	CDF SVX'
1998	CLEO III
1999	BaBar
2001	CDF SVXII+ISL
2009	ATLAS SCT
2009	CMS tracker
2025	ATLAS ITK
2025	CMS upgrade

Hybrid Pixels

1999	Delphi
2009	ATLAS
2009	CMS
2015	ATLAS IBL
2017	CMS
2019	velopix
2025	ATLAS
2025	CMS

CMOS Pixels

2014	STAR
2019	ALICE

CCDs

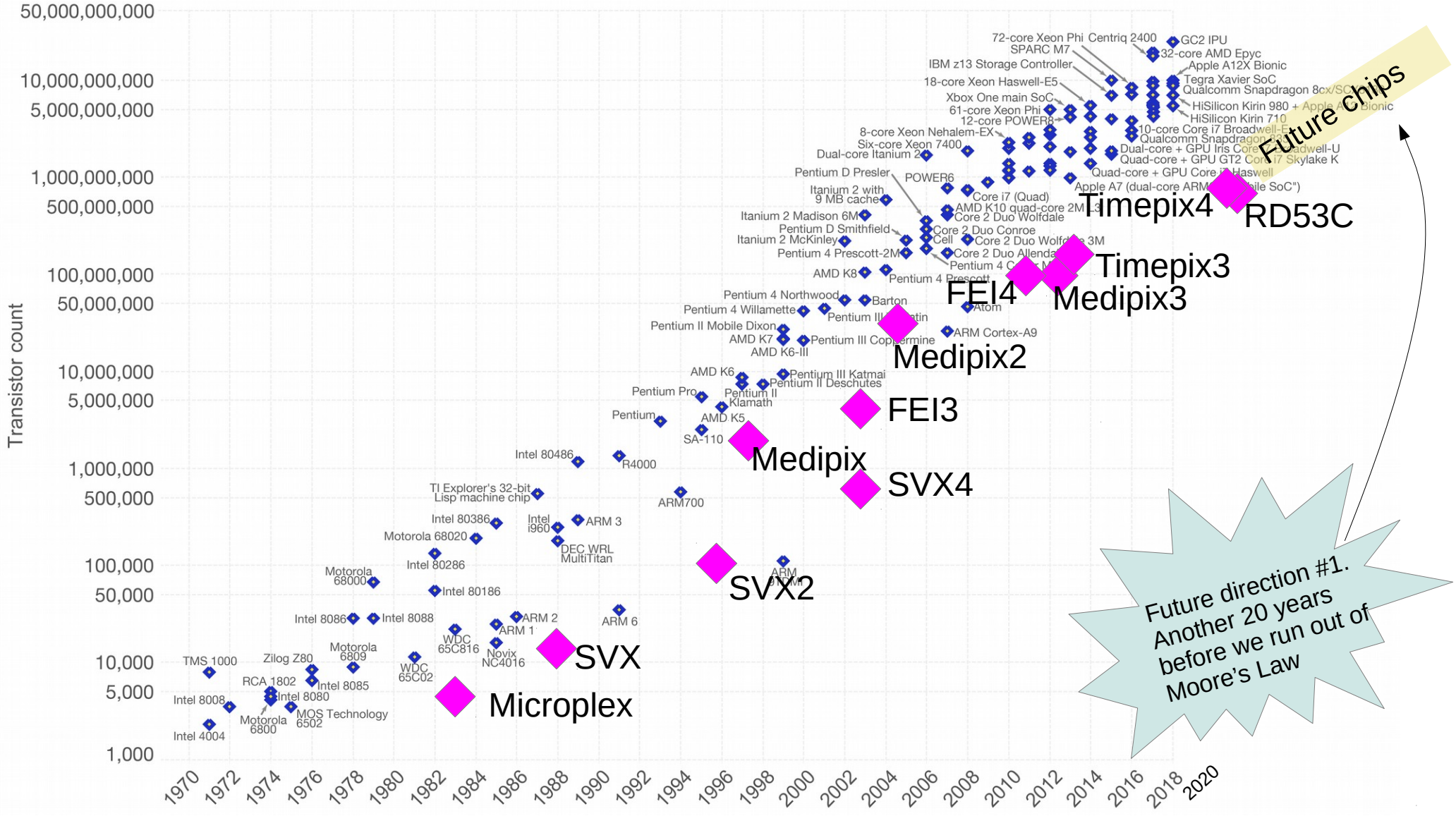
1993	VXD

pixel

IBL

ITk

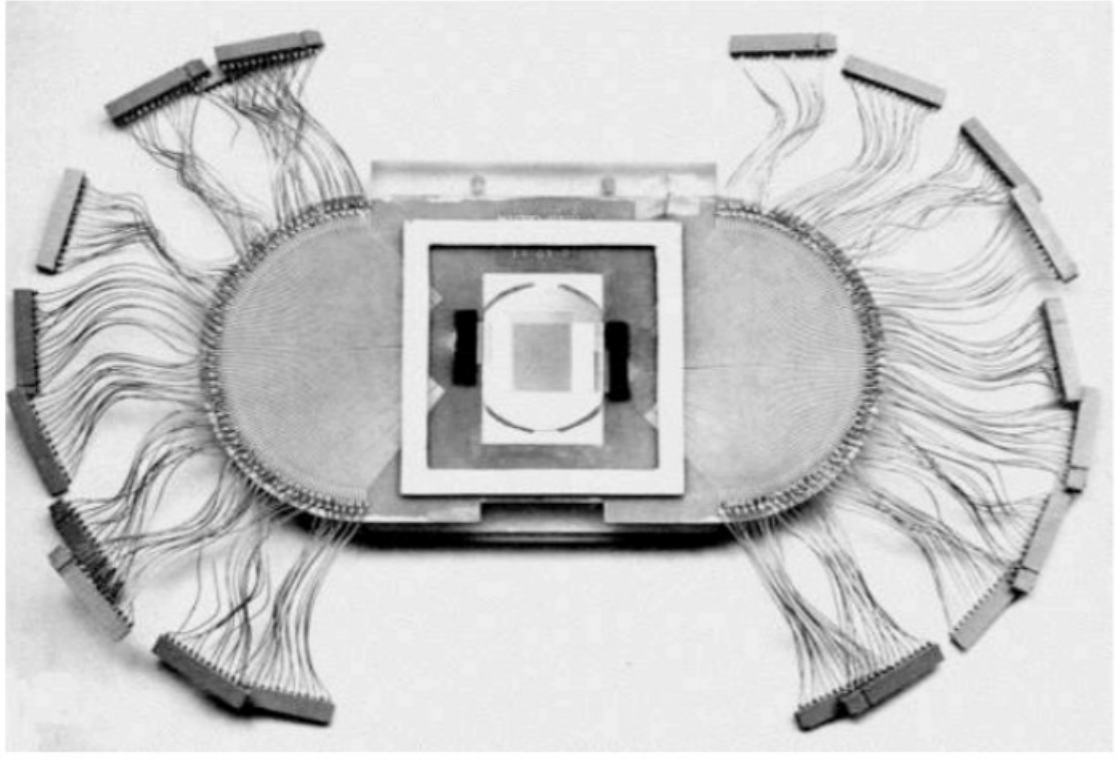
HEP Tracker Integrated Circuits



Why Microplex?

Because this was a silicon strip module before:

NA11, CERN 1981

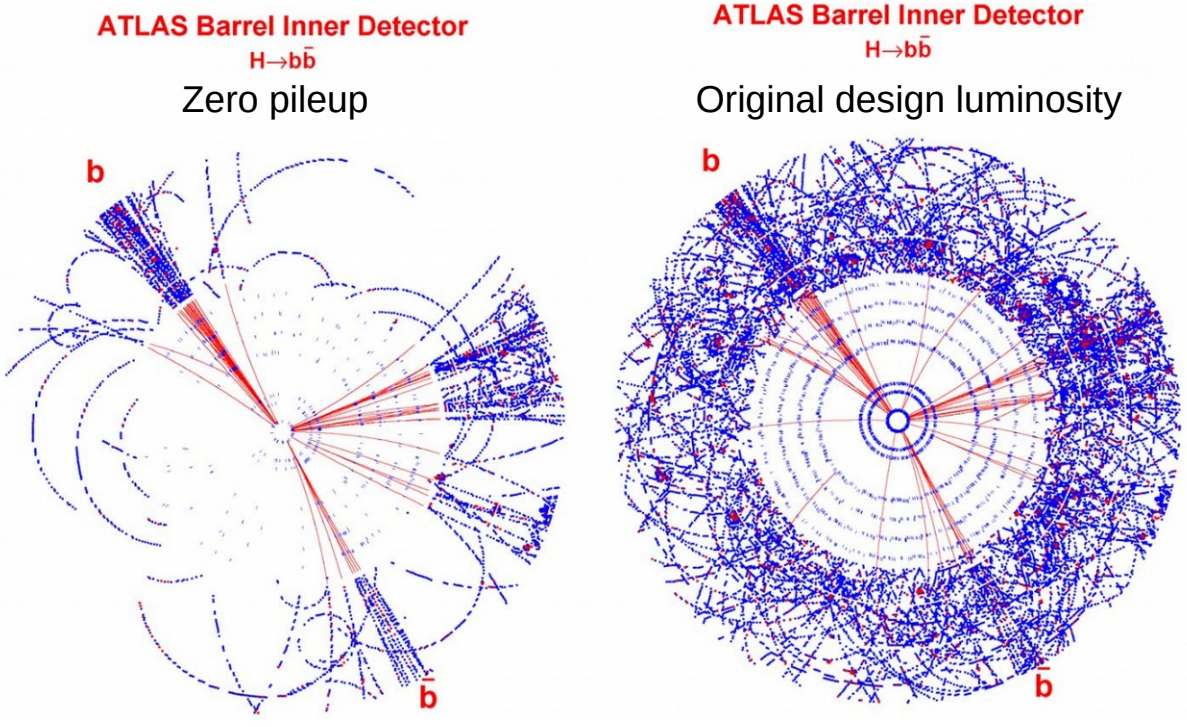


NIM205 (1983) 99

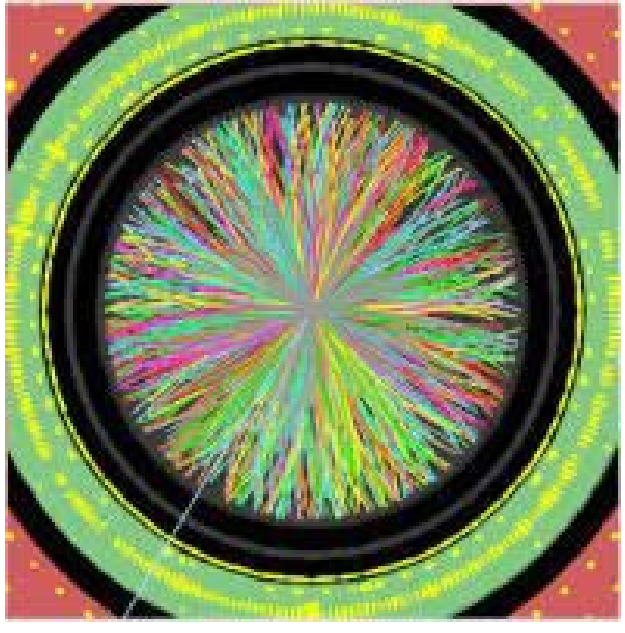
It did not scale

Why Microplex?

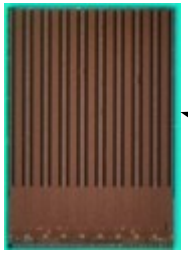
Original ATLAS motivation for pixels circa 1995



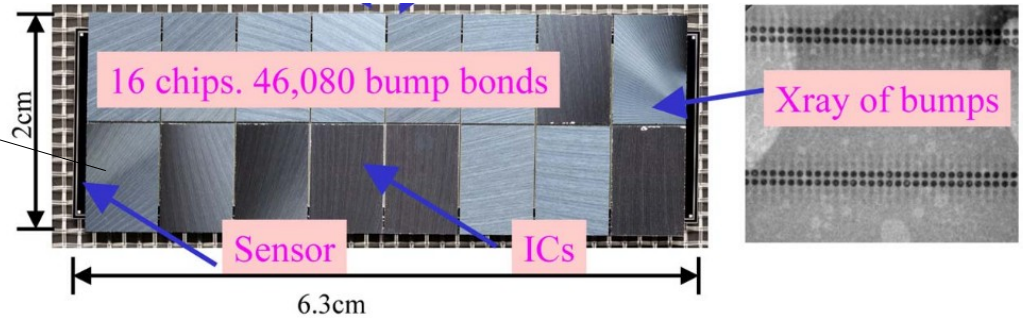
HL-LHC is far beyond



FE-I3 readout chip



Solution:



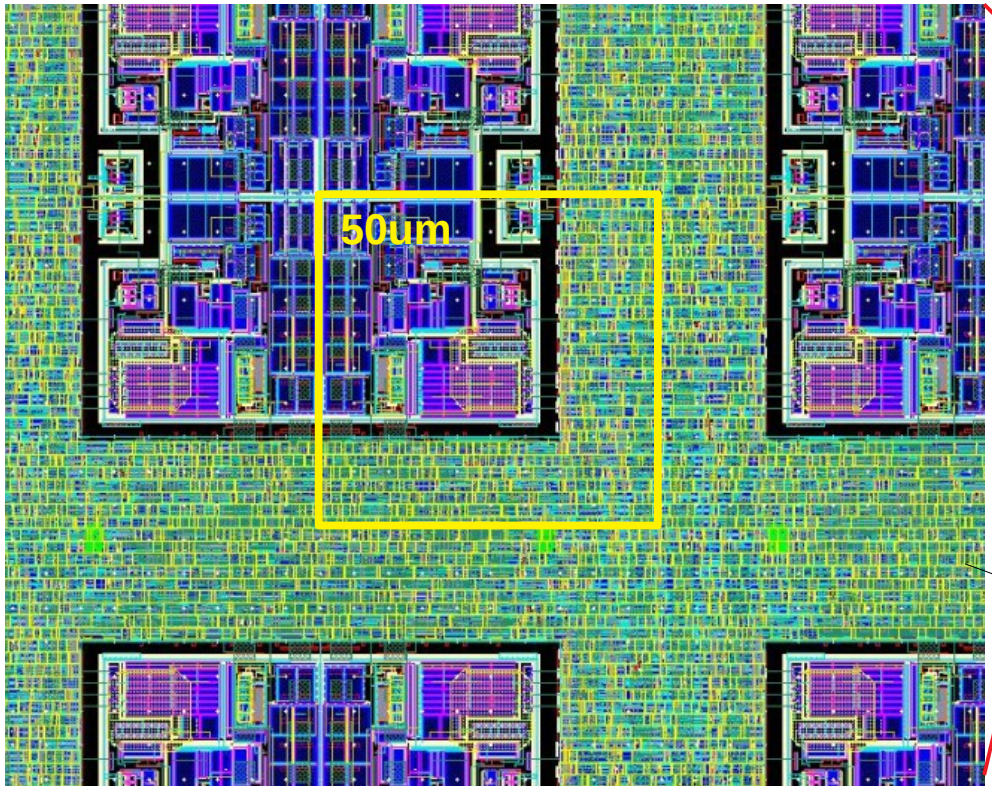
It did not scale.
A new readout chip solution had to be developed

RD53 Hybrid Pixel Readout
100x higher rate and radiation

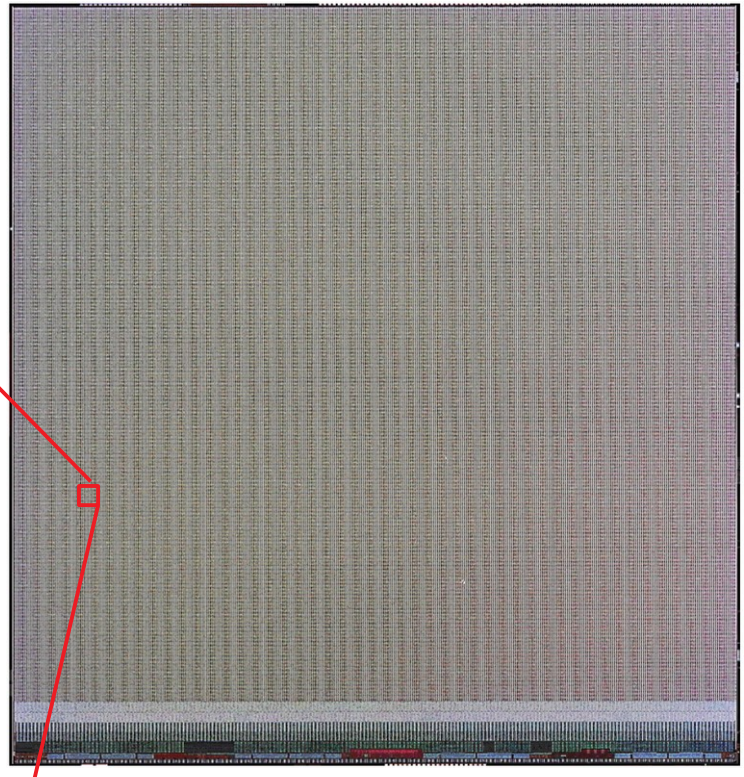
Cern.ch/rd53

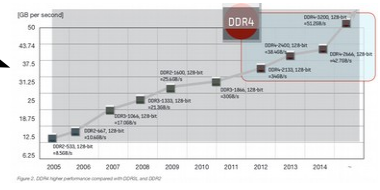
RD-53 Collaboration Home

RD-53 will design and produce the next generation of readout chips for the ATLAS and CMS pixel detector upgrades at the HL-LHC. More details can be found in the 2018 extension proposal and the original collaboration proposal.

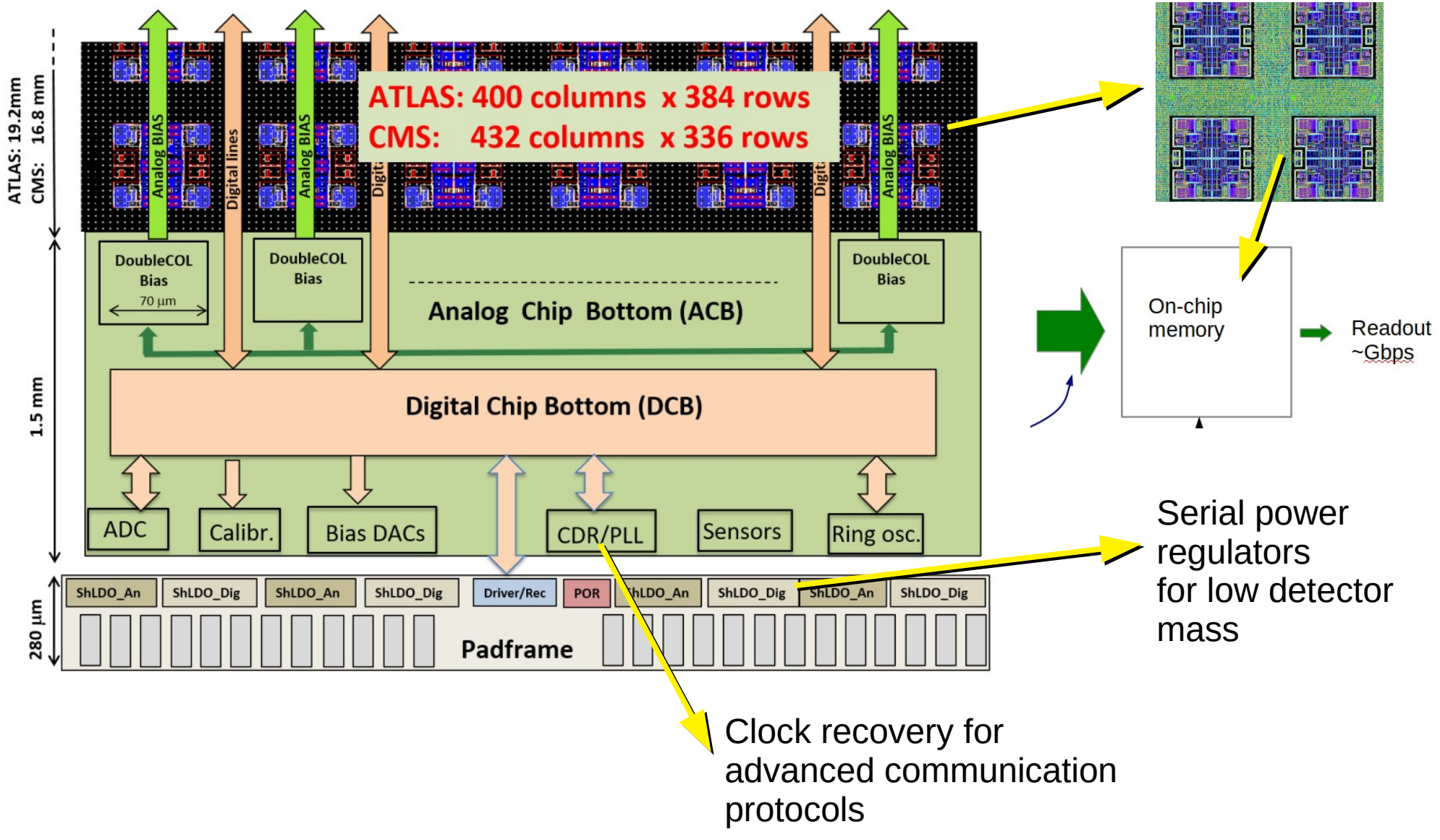


~1000 transistors

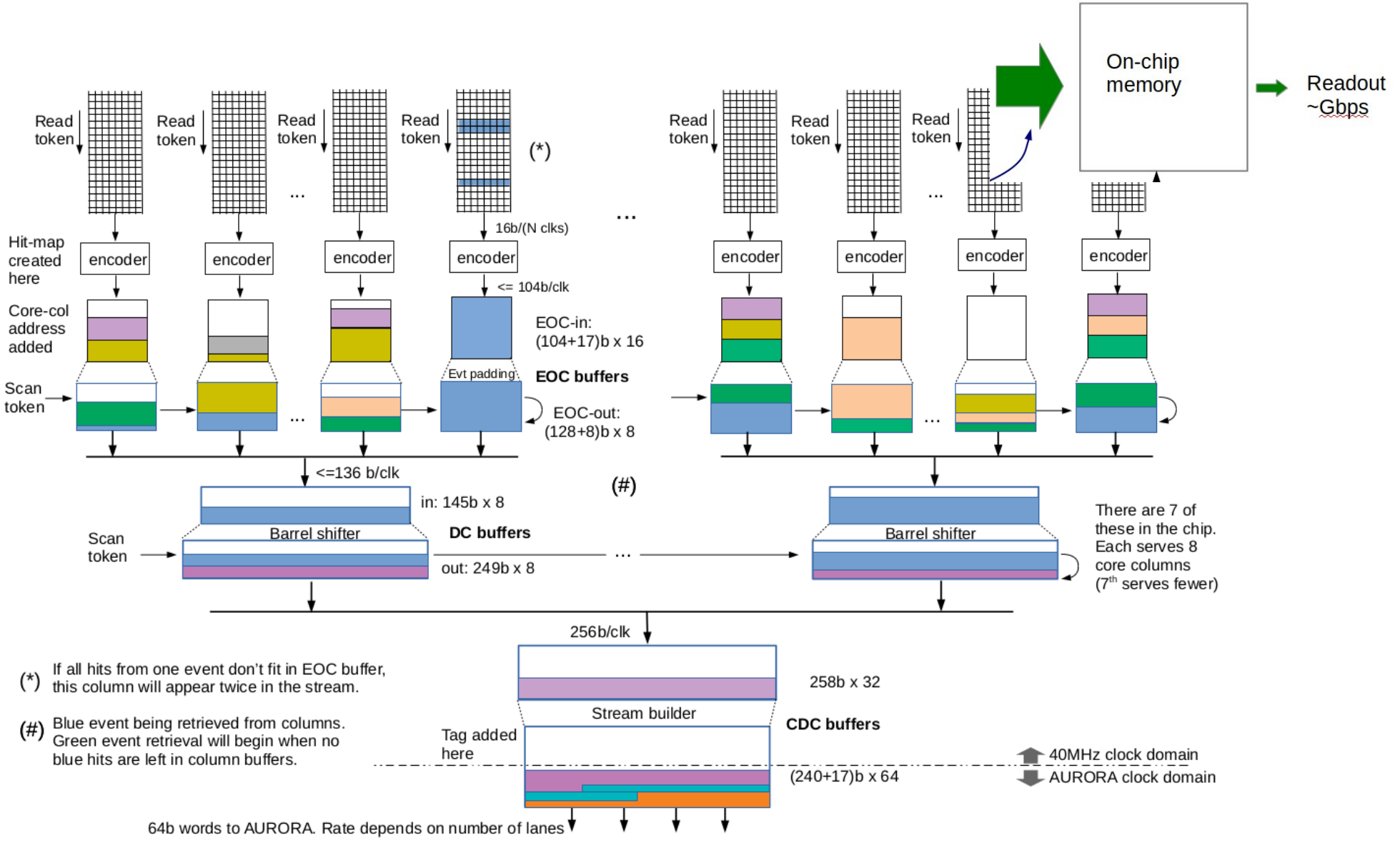




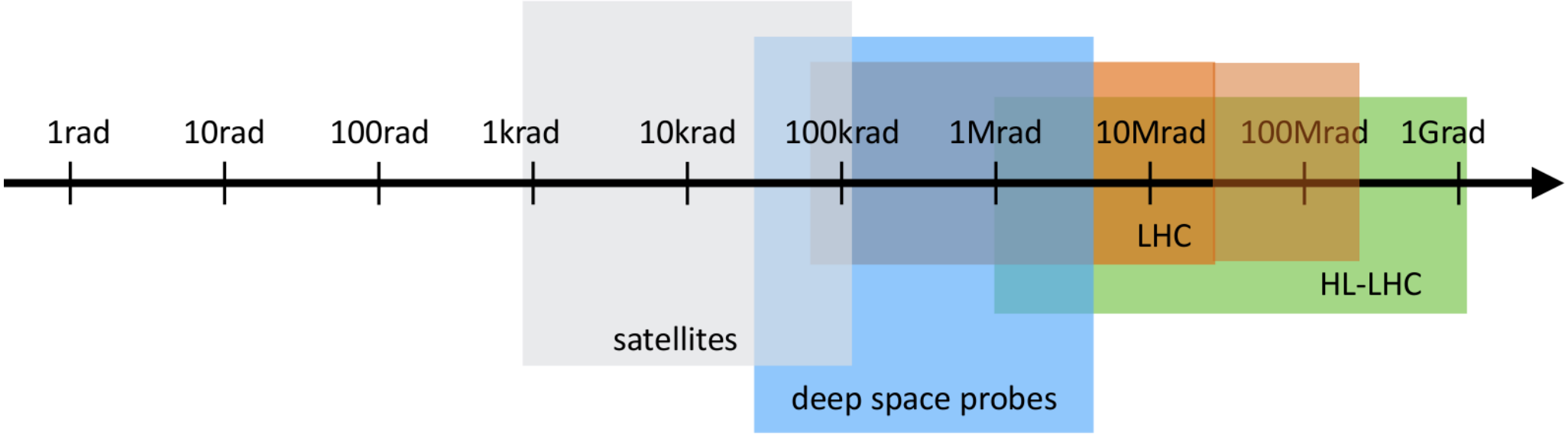
Complex system on chip



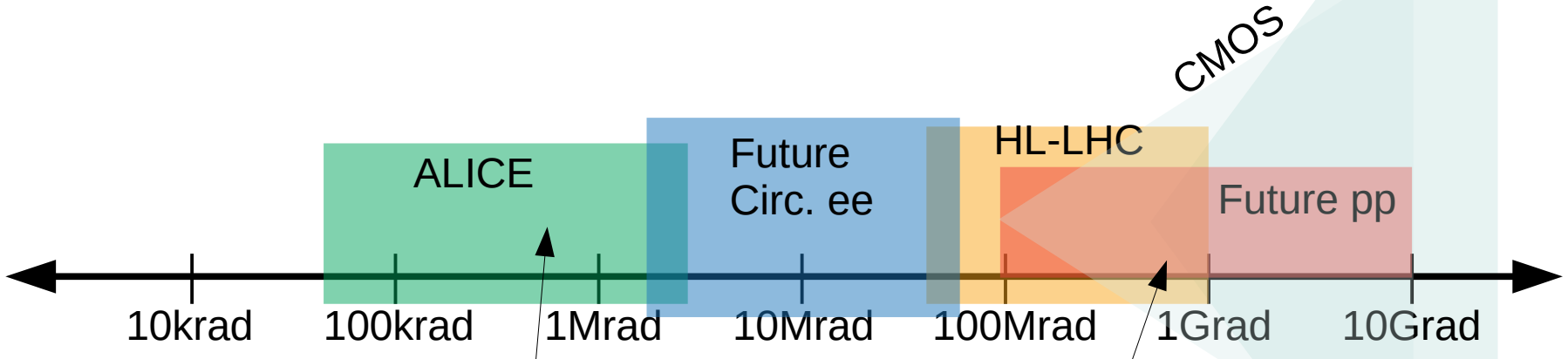
Example of non-trivial processing



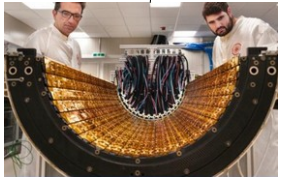
Radiation Environments

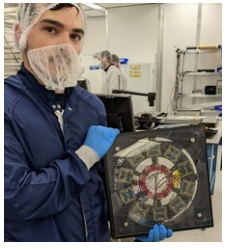


HEP IC Radiation Outlook



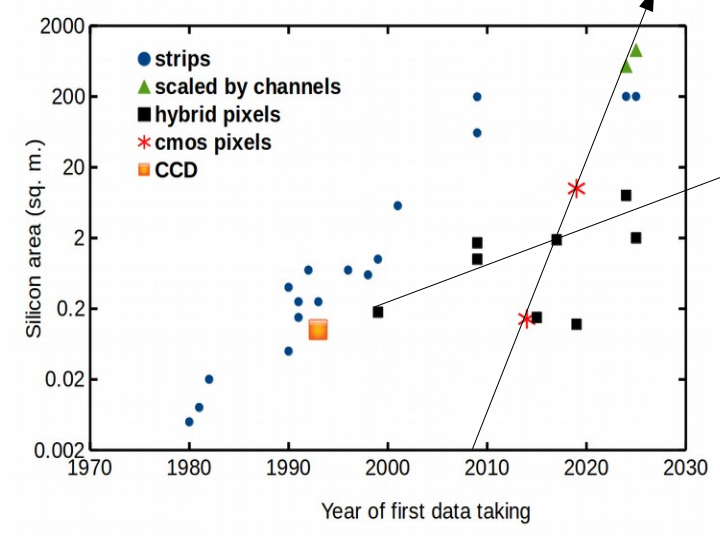
Inner Layer Dose

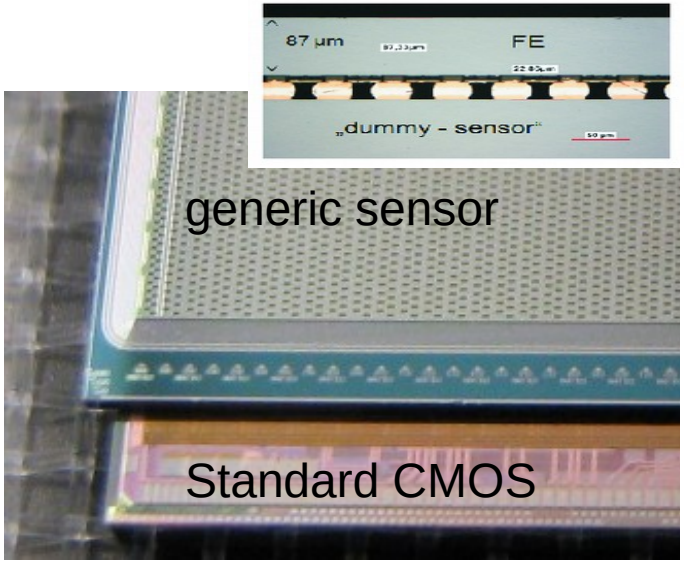


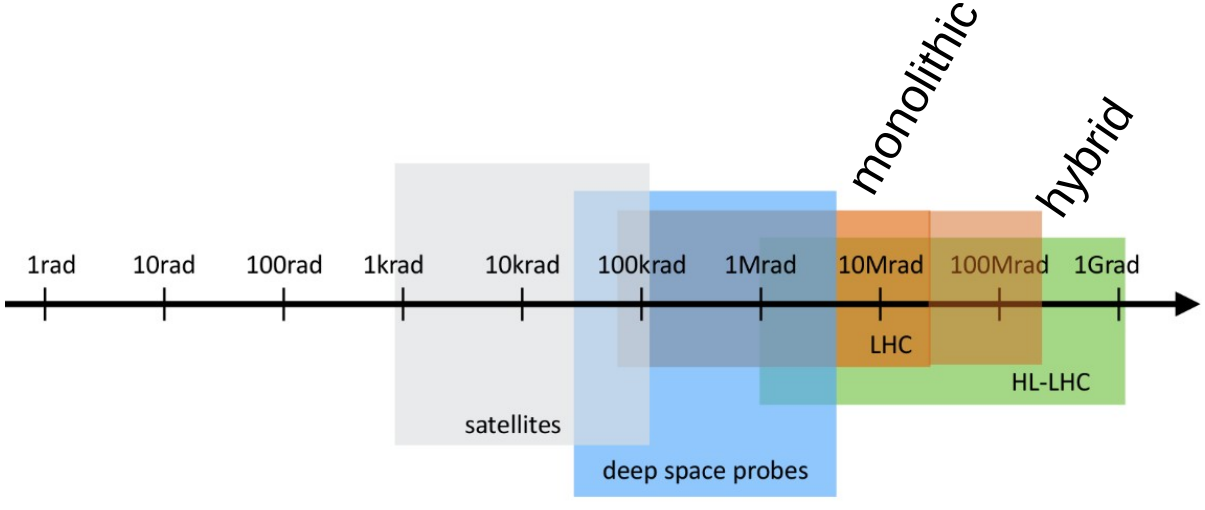


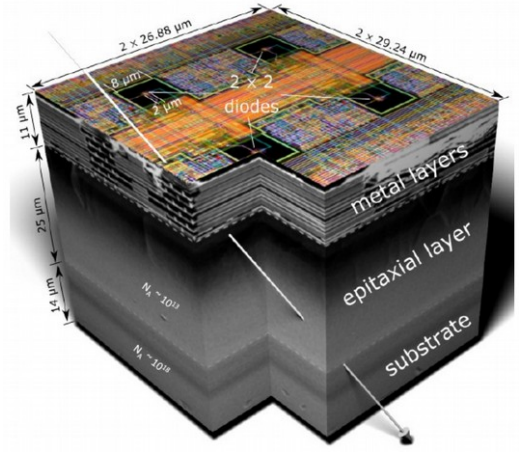
Temperature history
Process details
Dose rate
Dose history
Annealing
…

Trade-offs



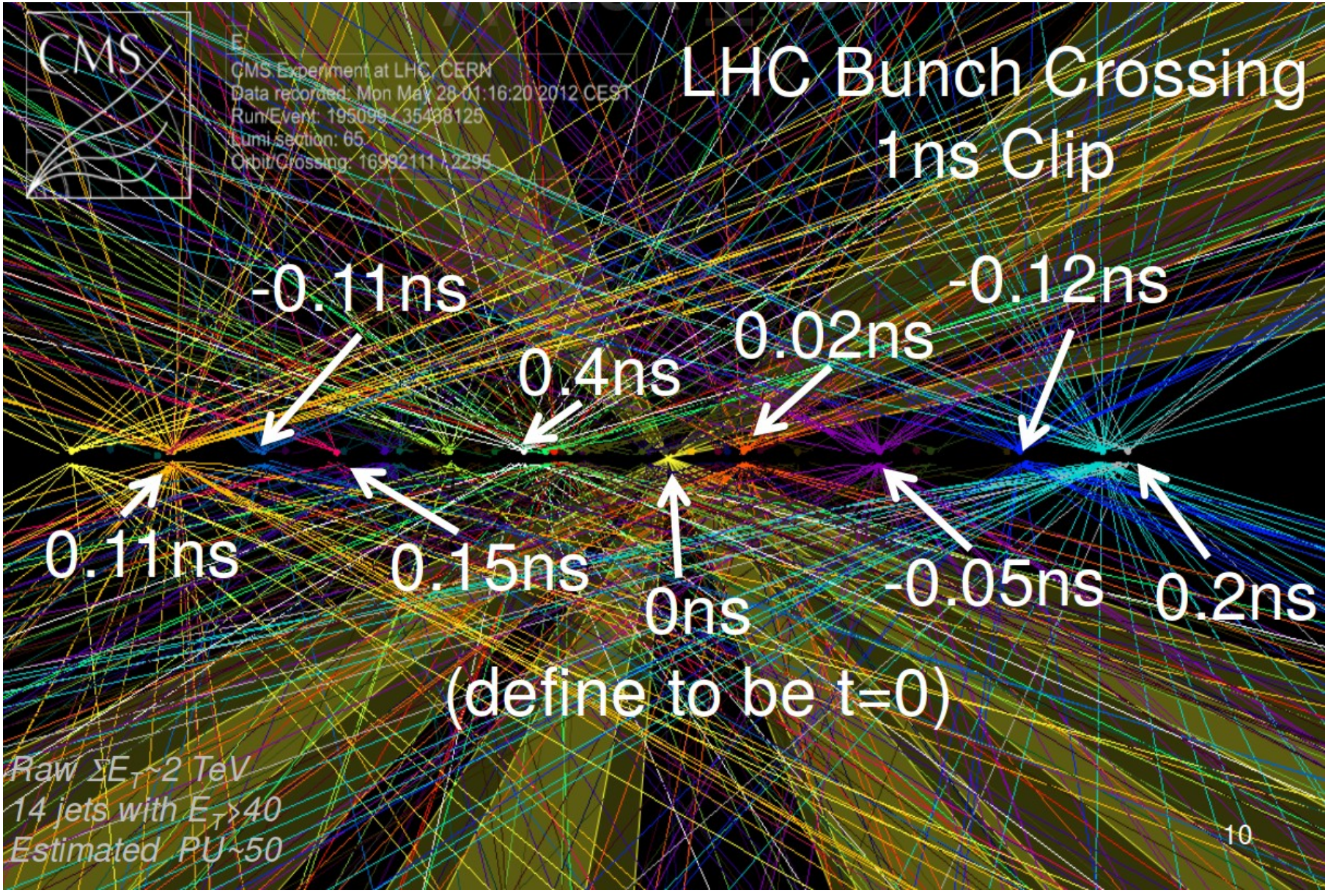




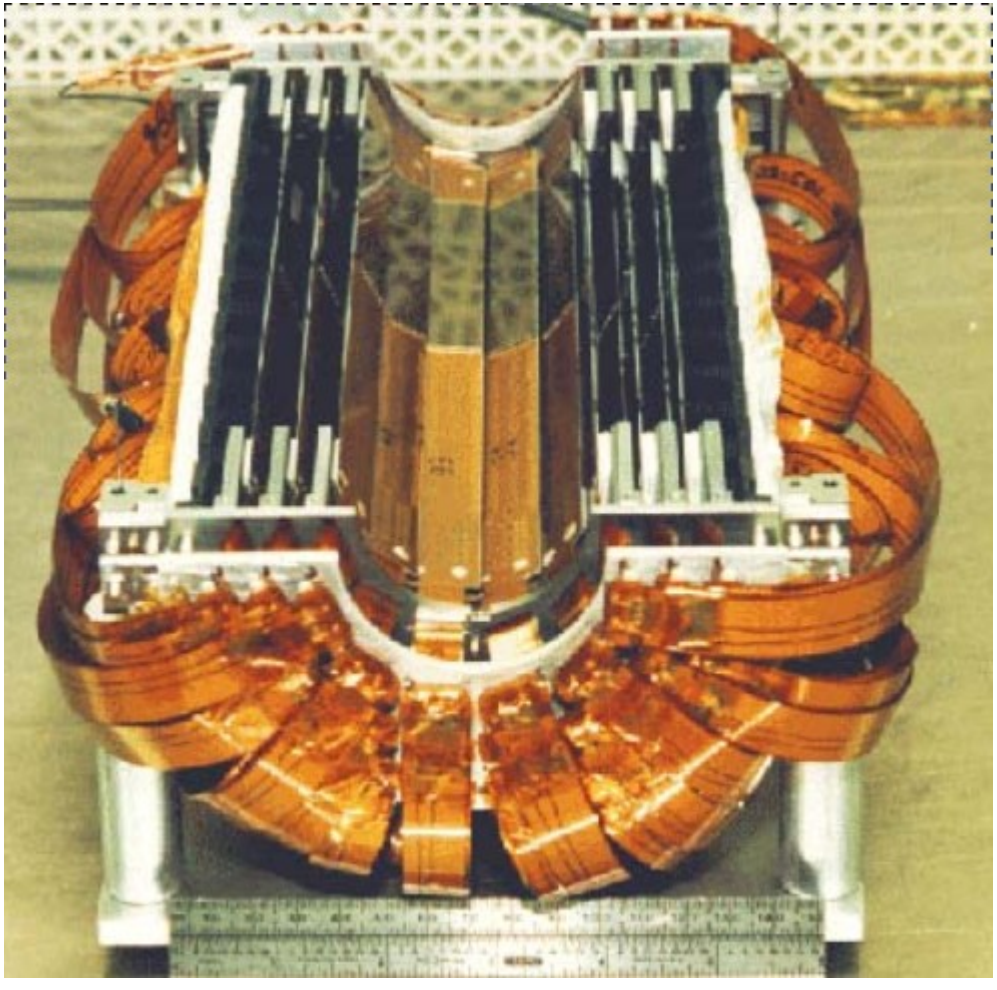


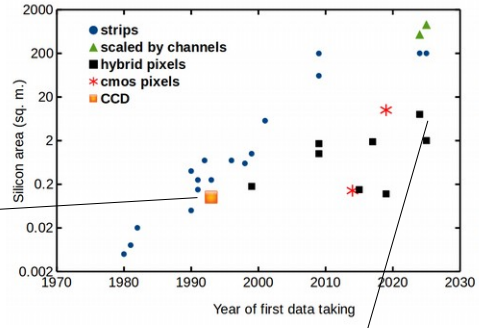
Highly customized non-portable process

A future direction



The Rate Extremes



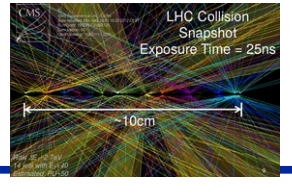


SLD VXD

- Silicon area: 0.12 m²
- 300M pixels (20μm x 20μm)
- But only 350,000 Z decays recorded
- => most pixels were never hit by real collision particle!

HL-LHC

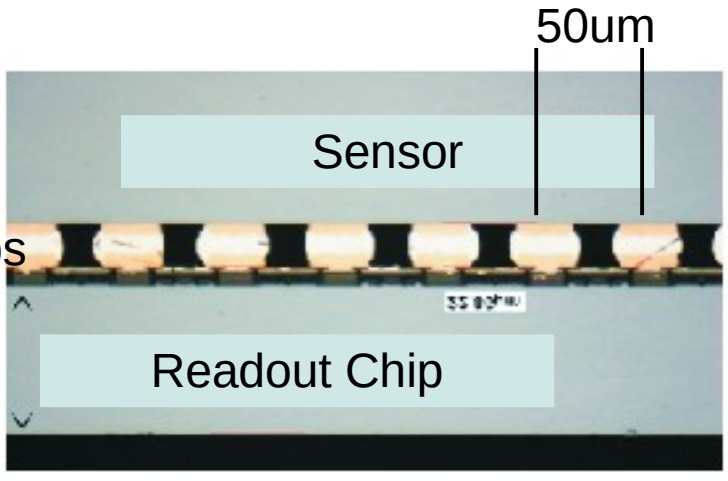
- Inner layers of ATLAS and CMS high luminosity upgrades will see 10 collision particles in every Si atom!

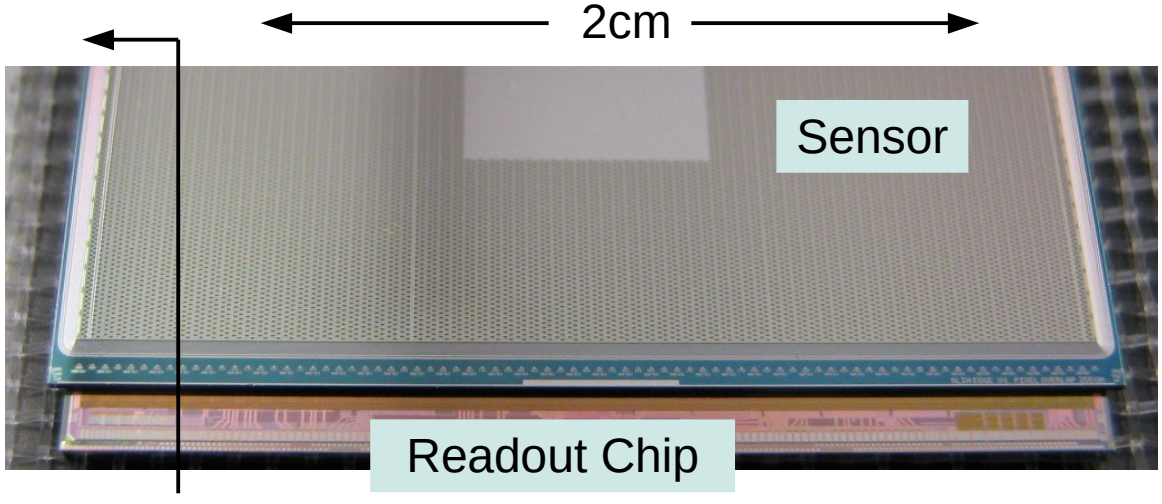


X 10^{16}

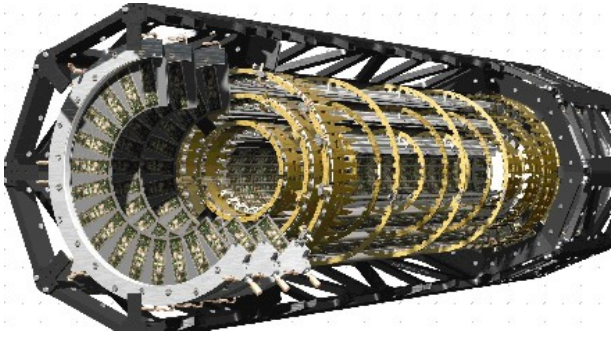
B A C K U P

Hybrid Pixel Detector Technology

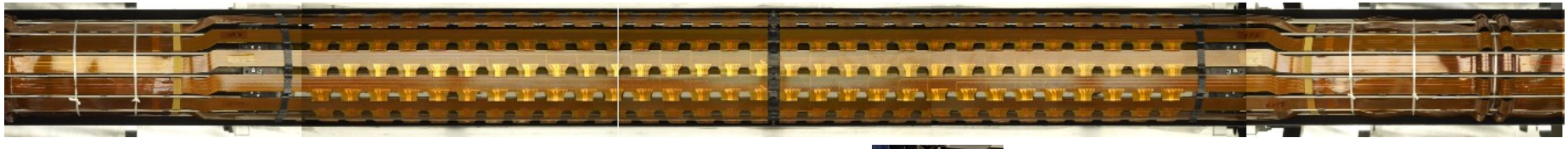




ATLAS PIXEL 2007 80M pixels

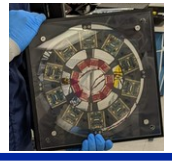


ATLAS IBL 2014 12M pixels

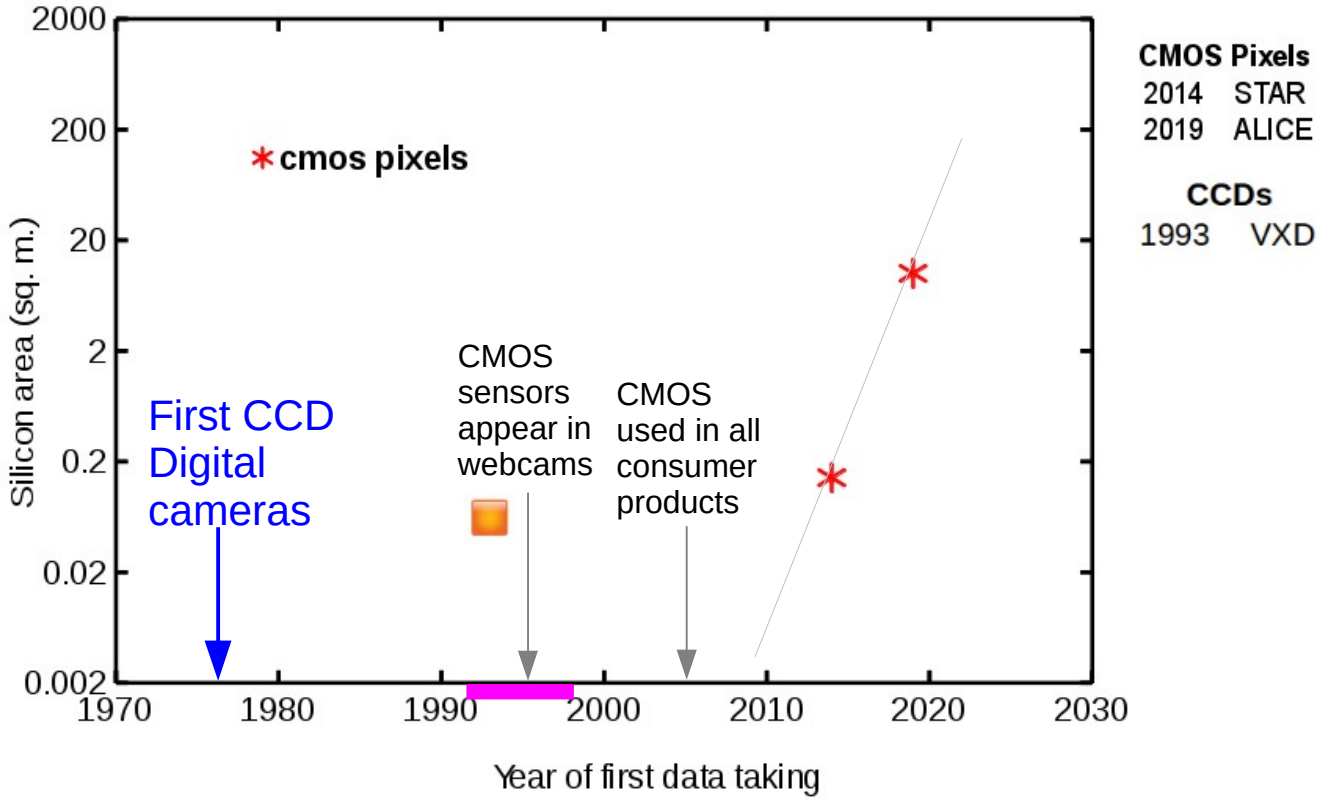


ATLAS ITK 2026, 5G pixels

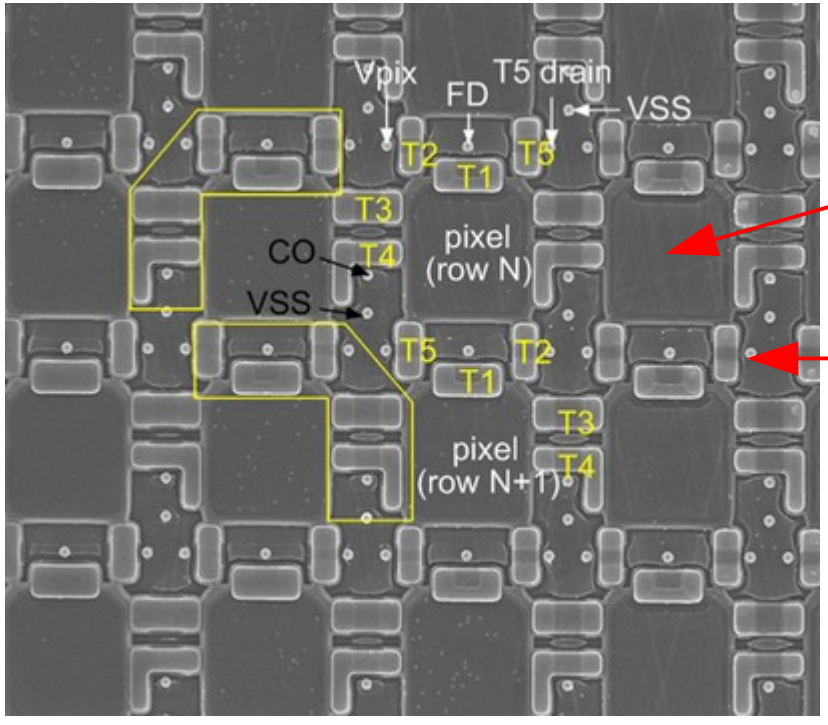
Remember the tour...



Connection to Consumer Electronics



Close-up of CMOS camera sensor



Photodiode covers about half the pixel area in this example

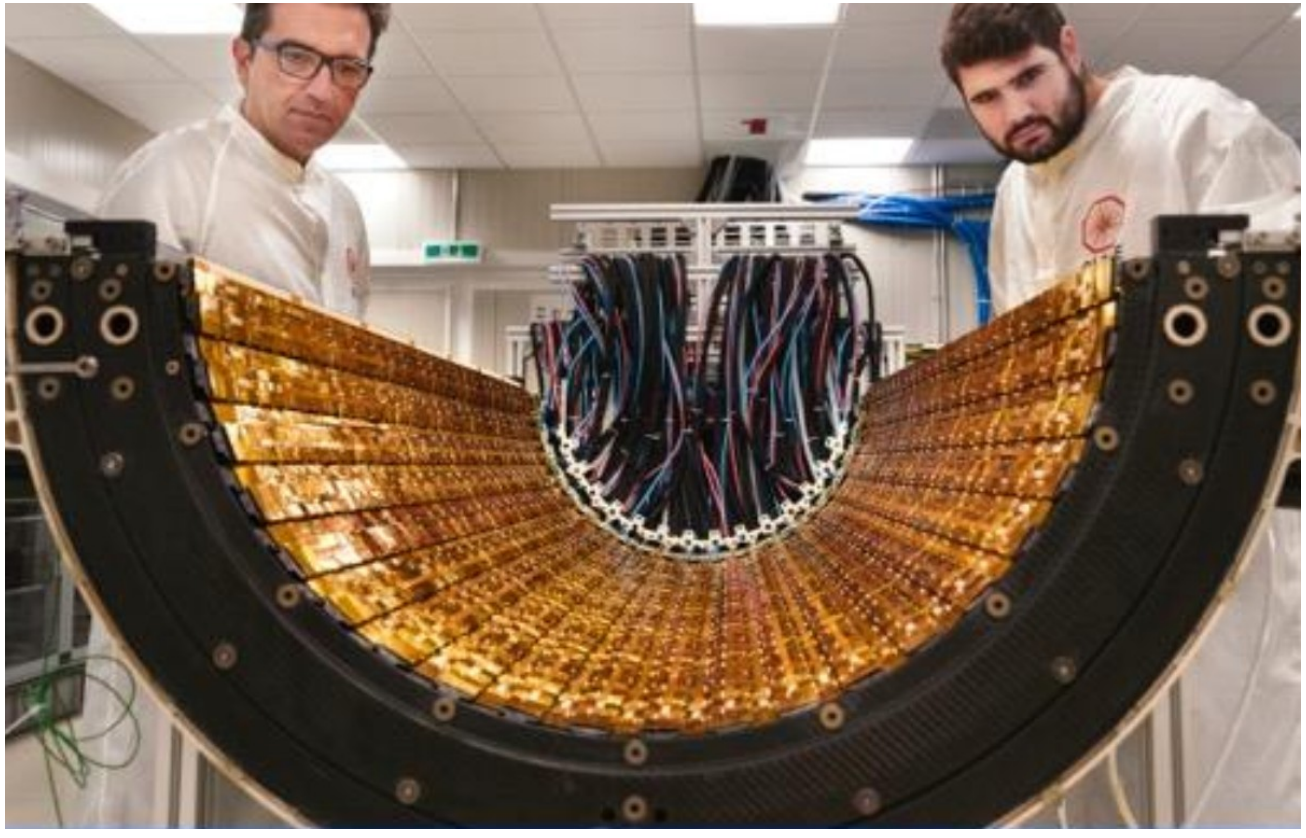
Metal traces have been removed. They run over the transistors leaving photodiode exposed

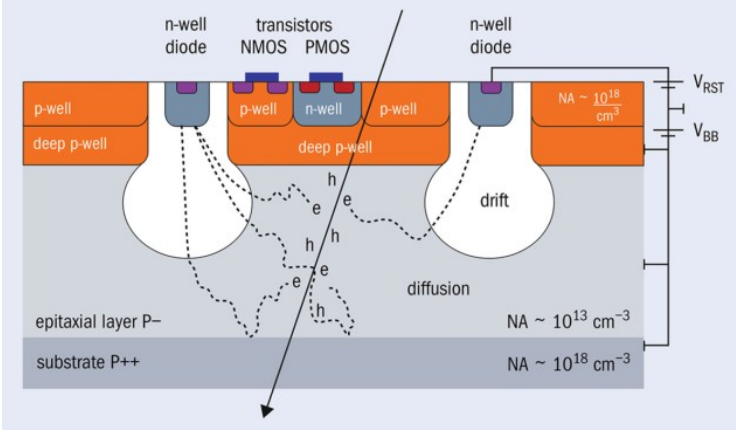
For particle tracking need 100% fill factor

Need low enough noise that can detect a single particle

Need radiation hardness

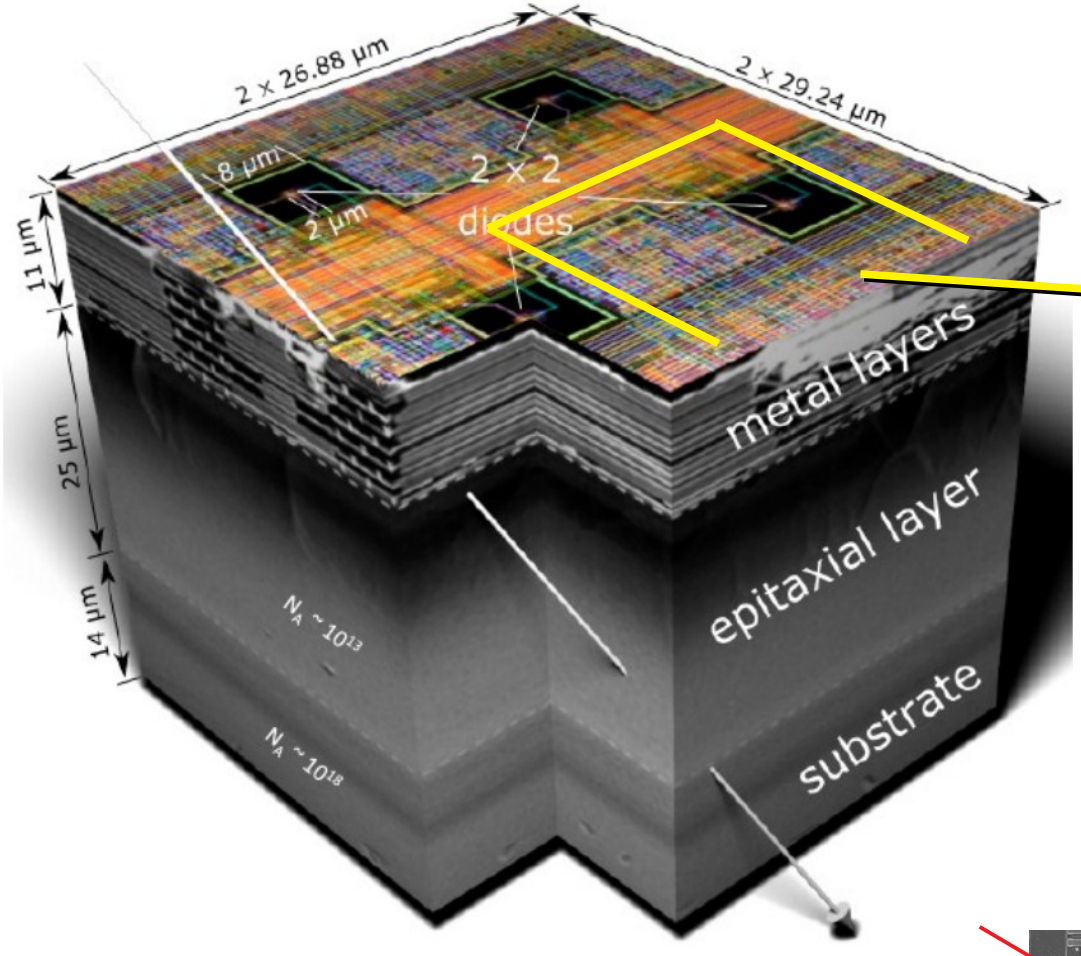
ALICE just installed a 10m² tracker made of CMOS sensors

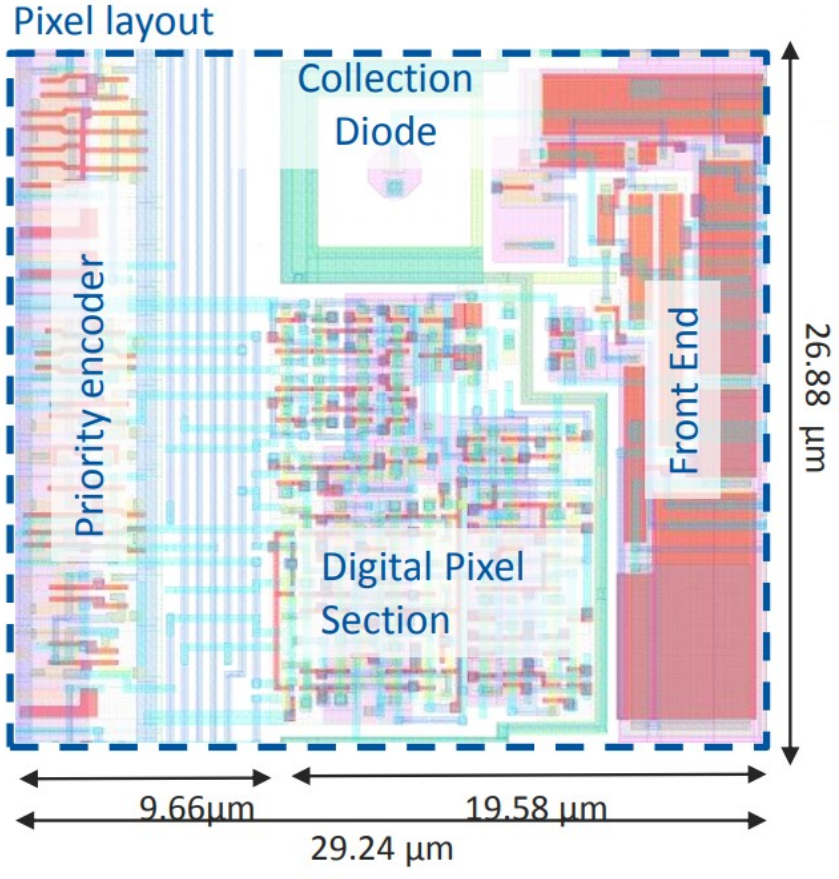


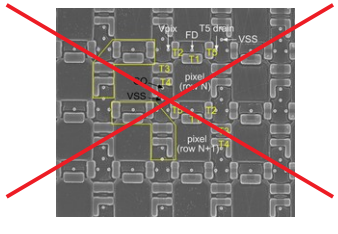


Highly customized CMOS process. Proprietary. Not portable

ALPIDE sensor chip- not a simple 3T pixel

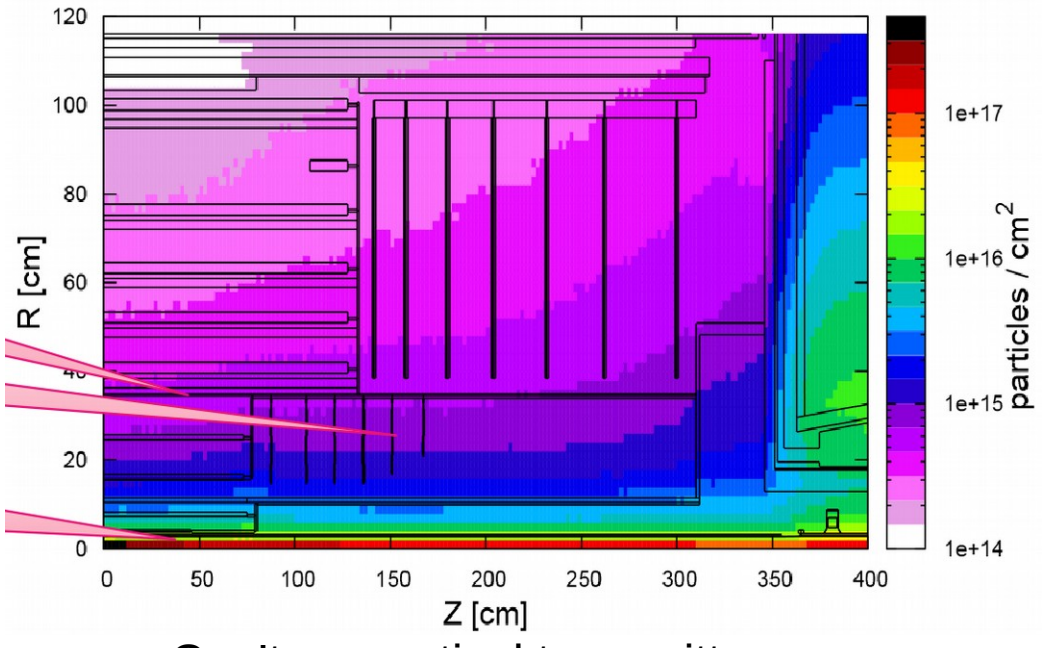


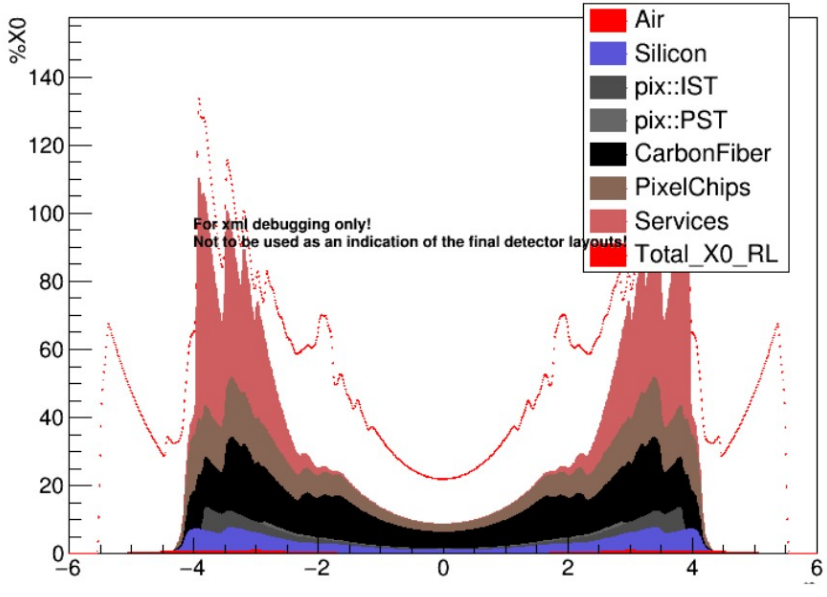




~100 transistors

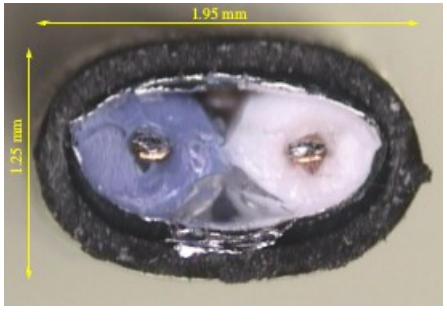
Limited Readout Bandwidth

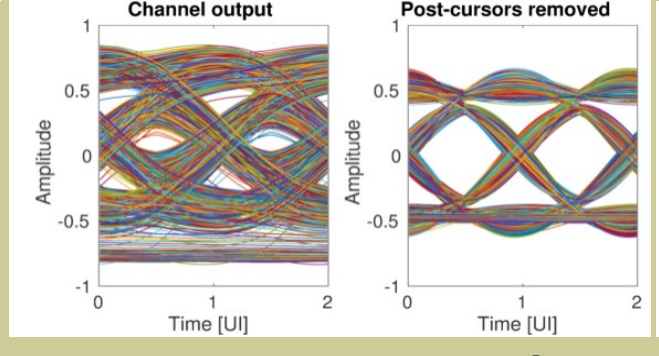


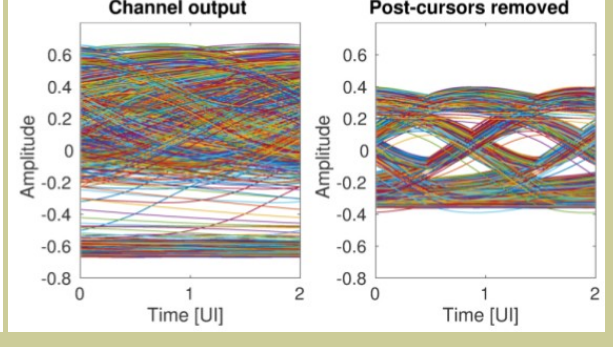


Can’t use optical transmitters

Can’t use heavy shielded cables

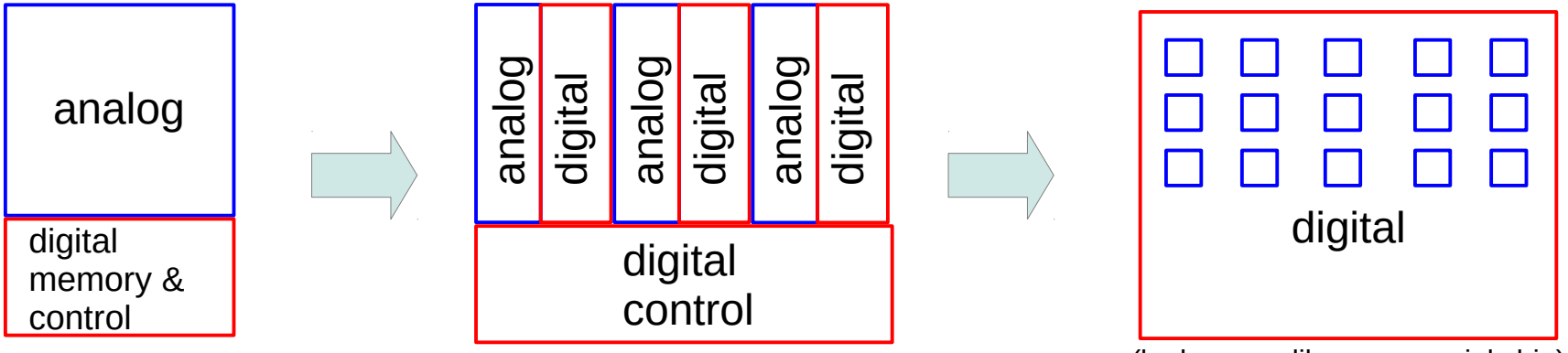






3m **5Gbps Simulation** **5m**

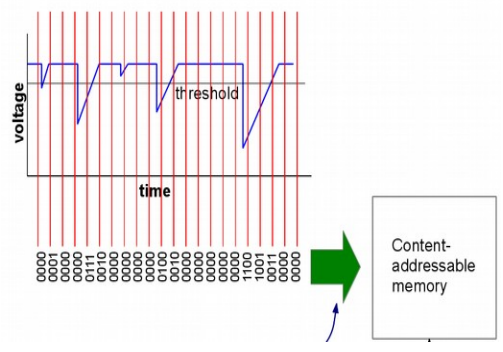
Readout Chip Evolution

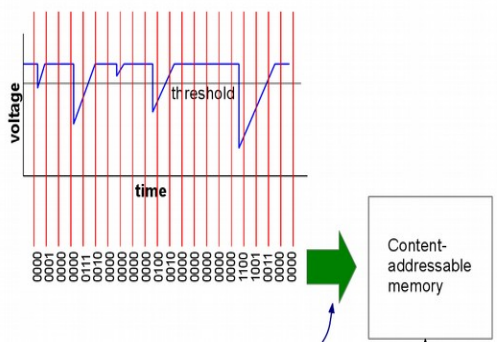


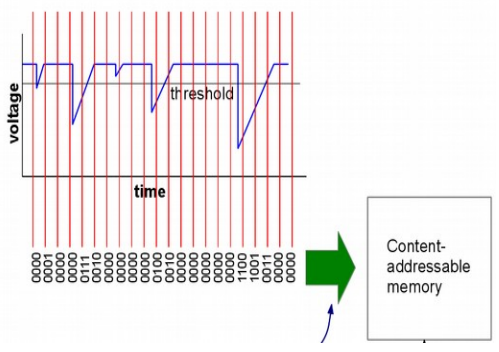
10 yrs ago

today

Future





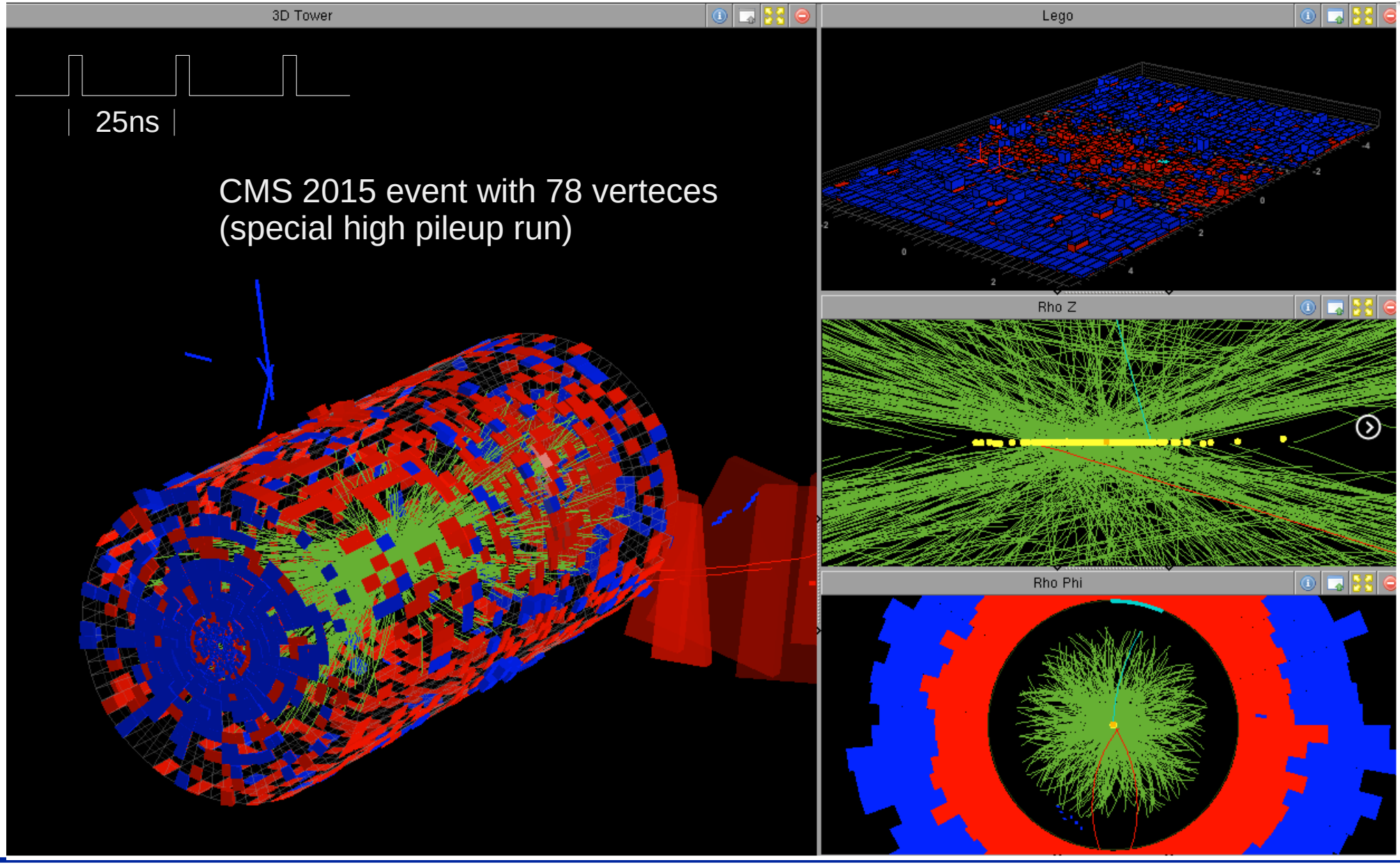


<1Gb/s /cm^2

5Gb/s /cm^2

40Gb/s /cm^2

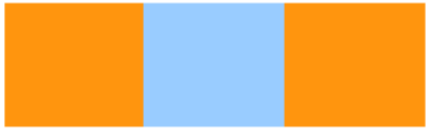
What Images Look Like



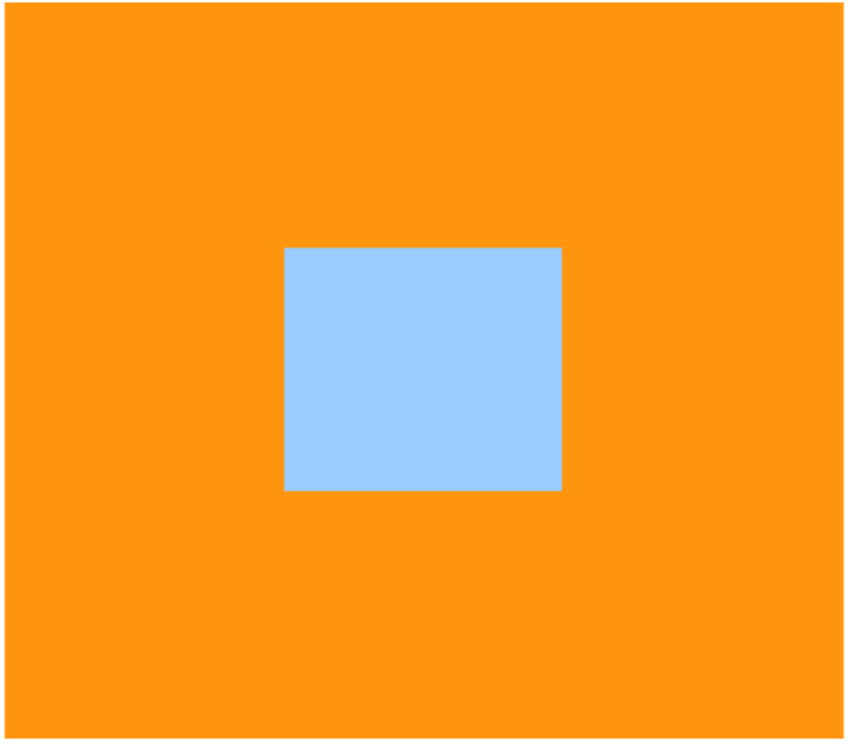
Rad Hard Logic Density Scaling

65nm

130nm

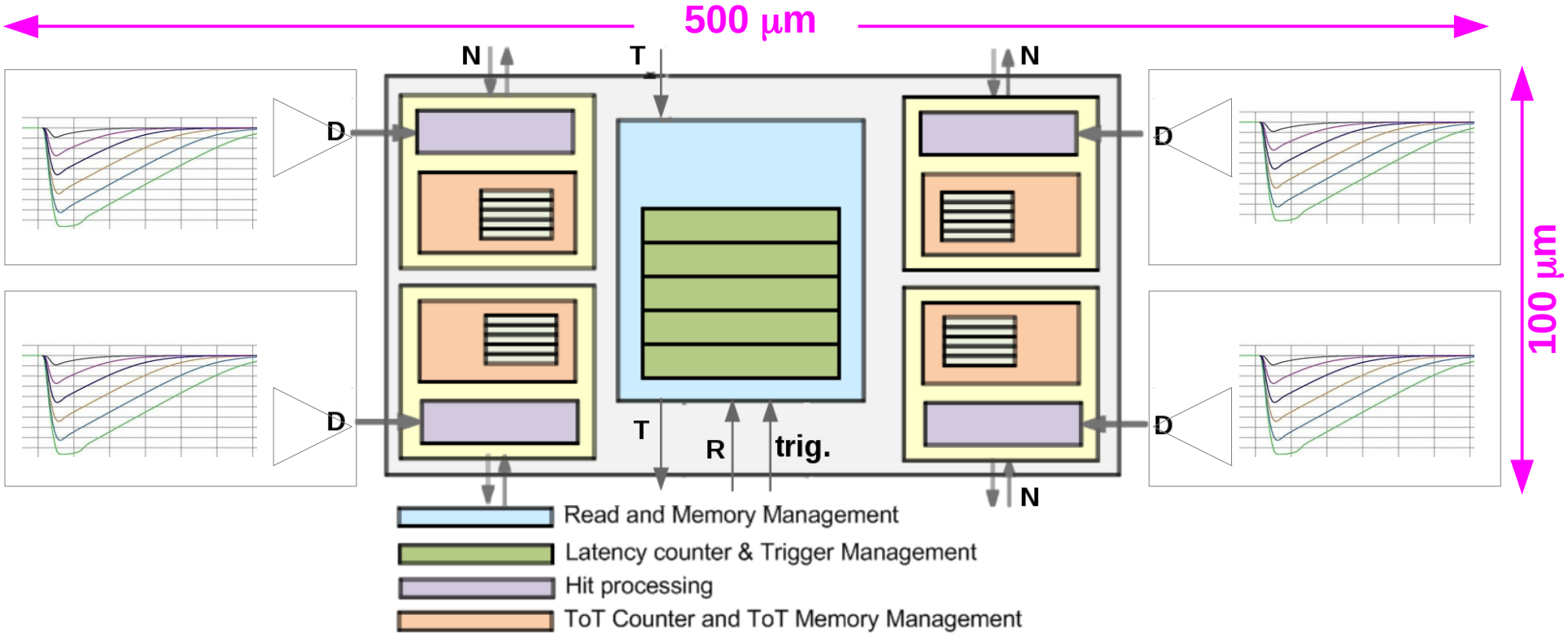


0.25um
ELT



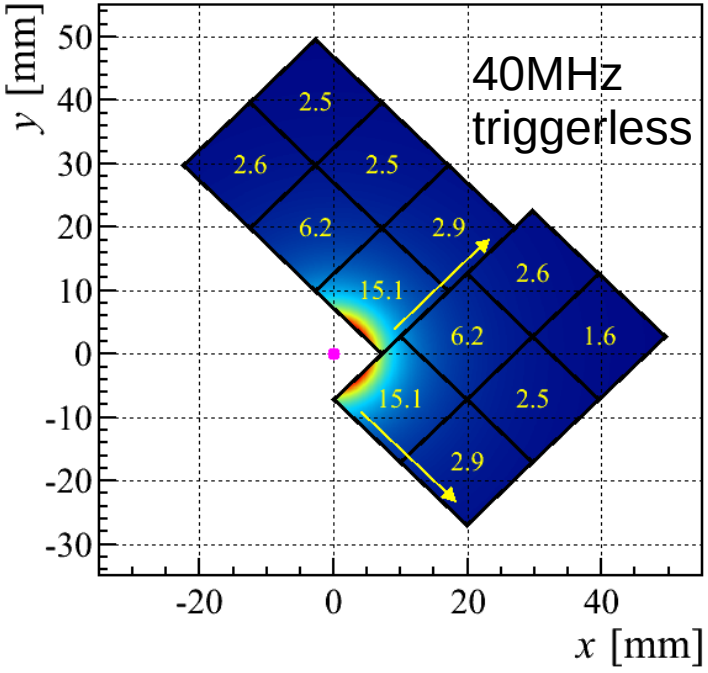
FE-I4 Digital Region

- **Digital block is shared with 4 inputs- each form an identical analog pixel.**

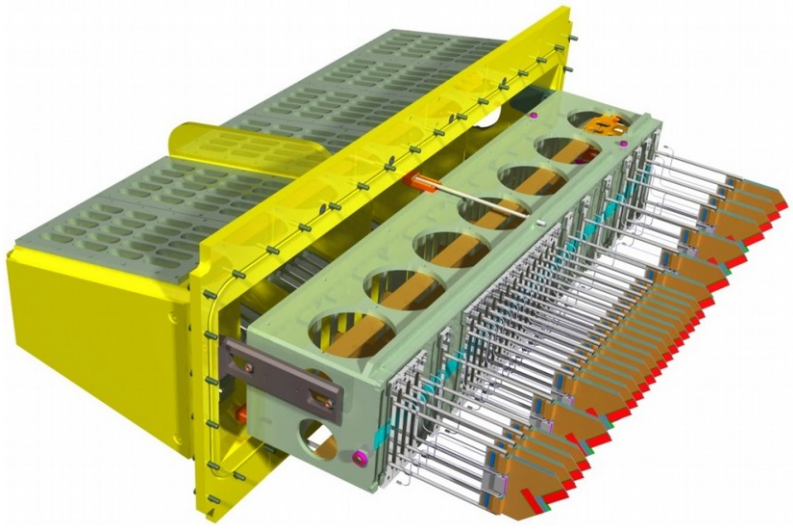


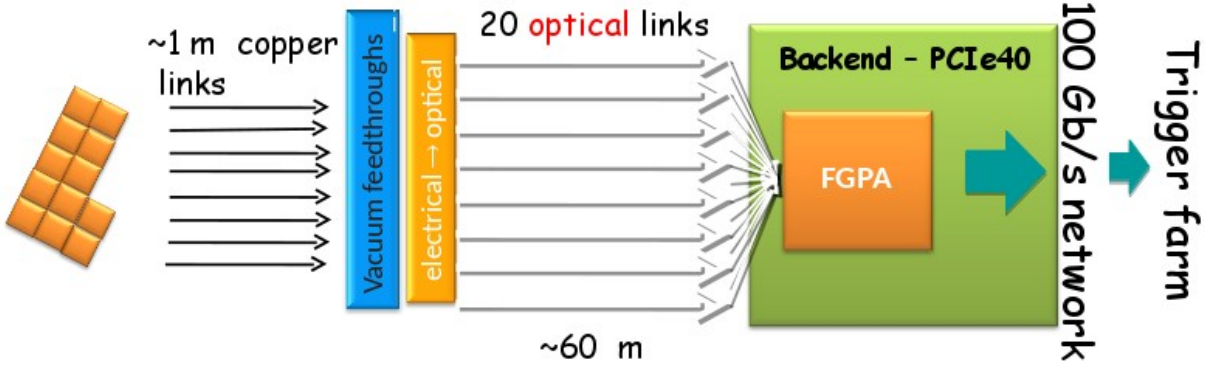
Velopix triggerless readout

Readout chips in LHCb Velopix plane
Output data rate per chip in Gbps



Velopix half with 26 planes





- Geometry looks like data flow diagram
- Lots of room outside physics acceptance
- Can have many cables out of each chip