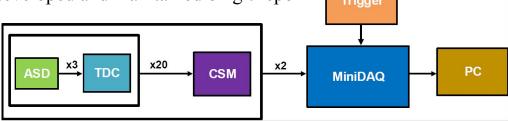


SiPM and drift tube readout and DAQ

Yuxiang Guo US Higgs Factory Planning, SLAC Dec 19, 2024

A portable MiniDAQ system with MDT front-end electronics

- New front-end electronics and DAQ developed for ATLAS MDT phase-2 upgrade to cope with HL-LHC requirements
- This MiniDAQ system is also used for FCC-ee R&D for straw tracker and drift chamber tests with cosmic rays and test beams
- System is lightweight and portable
- User friendly GUI is developed and maintained on git repo



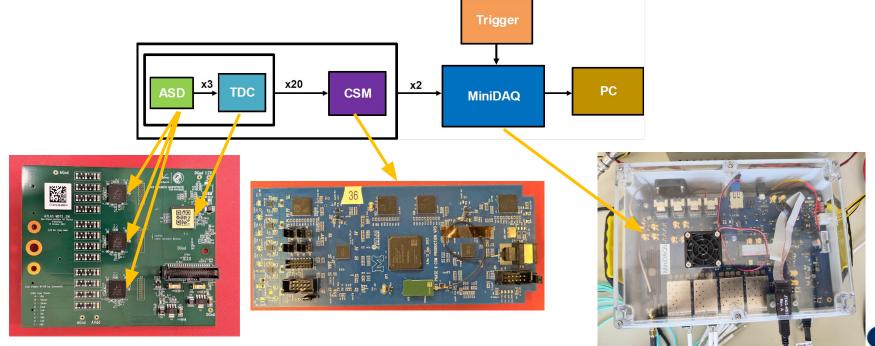
The MiniDAQ readout system used to read out data from 2 CSMs

- Basic readout channels = 960, data rate to DAQ = 40.96 Gbps, DAQ offline dump rate = 1 Gbps
- Readout channels and data rate can be doubled by adding one SFP+ FMC module
- Front-end voltage and temperature are monitored

A portable MiniDAQ system with MDT front-end electronics

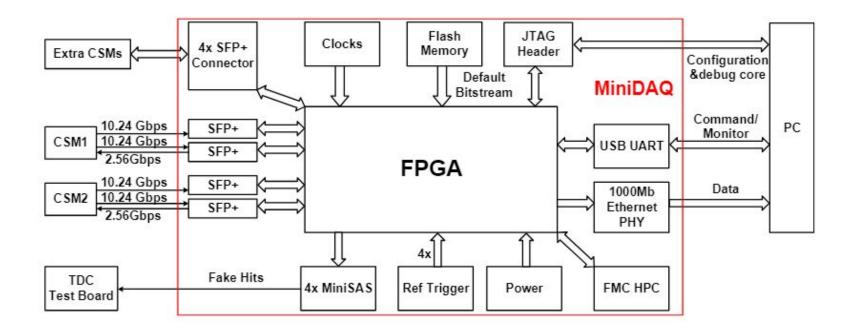
ASICs, front-end PCBs and MiniDAQ boards produced by various institutions

- ASD: Amplifier-shaper-discriminator circuit, 8 channels, peaking time 12 ns, small signal gain 18 mV/fC
- TDC: Time to digital converter, 24 channels, bin size 0.78 ns, 100 us dynamic range, output 2*320Mbps
- CSM: Chamber service module, 20 mezzanine readout and monitor, output 2*10.24Gbps
- MiniDAQ: 2 CSMs readout, mezz and CSM configuration, output 1Gbps



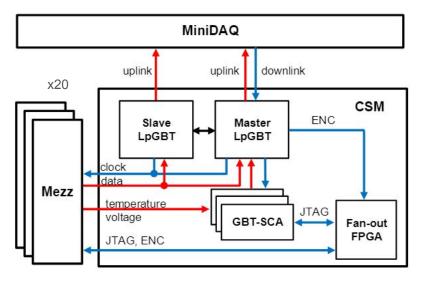
MiniDAQ board hardware

- FPGA: Xilinx Ultrascale KU035-1FBVA676C
- SFP+: 4 on board, 4 can be expanded through FMC connector
- On board oscillators for GTH reference clock and logic clock
- 4 High-speed comparators as external trigger
- Gigabit Ethernet for data dumping, USB UART for GUI communication

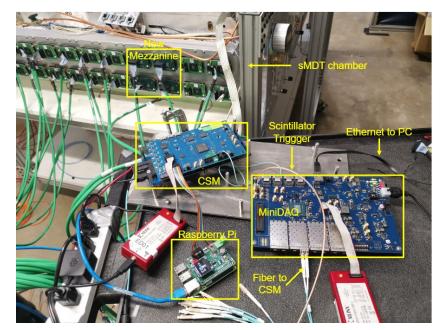


MiniDAQ data flow

- Data mode default: front-end triggerless, trigger matching in MiniDAQ for offline data storage
- Data mode optional: front-end triggered, all triggered data sent out for storage
- Each CSM contains 2 uplink fibers and 1 downlink fibers. Configurations, clocks and monitoring requests are distributed through downlink (2.56 Gbps), detector data and monitoring info are read back via uplinks

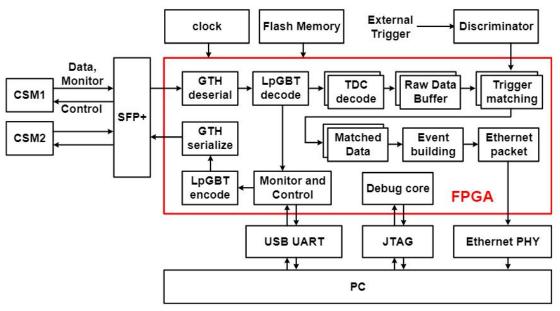


uplink (red) and downlink (blue) data flow



MiniDAQ firmware logic

- Multi-stage decoding: GTH deserial->LpGBT decode->TDC and monitoring data decode
- Idle word filtering: select valid hit data into RAMs
- **Trigger matching and event assembly**: External triggers are digitized by an FPGA-TDC. Timing info is compared with front-end TDC timing stored in the RAMs. Matched data are assembled with trigger and sent out as one event.



Functional block diagram of the miniDAQ system

MiniDAQ configuration GUI

- Configuration GUI Based on PyQt5
- Multi tabs for different hardware (LpGBT, SCA, Mezz)
- Multi-level popup windows for detailed configuration

A start																			
Mezz0	Mezz1	Mezz2	Mezz3	Mezz4	Mezz5	Mezz6	Mezz7	Mezz8	Mezz9	Mezz10	Mezz11	Mezz12	Mezz13	Mezz14	Mezz15	Mezz16	Mezz17	Mezz18	Mezz19
	~		v		v				•										
0	2.9863	0	2.9769	0	2.9989	0	0	0	2.9993	0	0	0	0	0	0	0	0	0	0
0	1.1931	0	1.1937	0	1.2039	0	0	0	1.2015	0	0	0	0	0	0	0	0	0	0
0	42.89	0	43.26	0	42.99	0	0	0	42.99	0	0	0	0	0	0	0	0	0	0
Mezz20	Mezz21	Mezz22	Mezz23	Mezz24	Mezz25	Mezz26	Mezz27	Mezz28	Mezz29	Mezz30	Mezz31	Mezz32	Mezz33	Mezz34	Mezz35	Mezz36	Mezz37	Mezz38	Mezz3
				V	V											\checkmark	\checkmark		
0	0	0	0	3.0033	2.9979	0	0	0	0	0	0	0	0	0	0	3.0011	2.9998	0	0
0	0	0	0	1.2037	1.2031	0	0	0	0	0	0	0	0	0	0	1.2046	1.2047	0	0
0	0	0	0	42.28	42.87	0	0	0	0	0	0	0	0	0	0	41.69	43.94	0	0
								cl	ear info										
59:08>>1	FDC16 D	VDD_GN	D= 0.017	73															
59:09>>1	TDC16 TI	EMP_GN	D= 0.010)3															
				0															
				0															
				05															
	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	○ 2.9863 0 1.1931 0 42.89 Mezz20 Mezz21 □ □ 0 0 0 0 0 0 0 0 0 0 0 0 59:08>>TDC16 D 59:09>>TDC16 T 59:09>>TDC17 A' 59:09>>TDC17 A' 59:09>>TDC17 D' 59:09>>TDC17 D' 59:09>>TDC17 D' 59:09>>TDC17 D'	Image: Constraint of the second sec	Image: Constraint of the second se	Image: Constraint of the second se	Image: Constraint of the sector of the se	Image: Constraint of the sector of the se	Image: Image	Image:	Image:	Image:	Image:	Image:	Image:	Image:	Image:	Image:	Image:	Image:

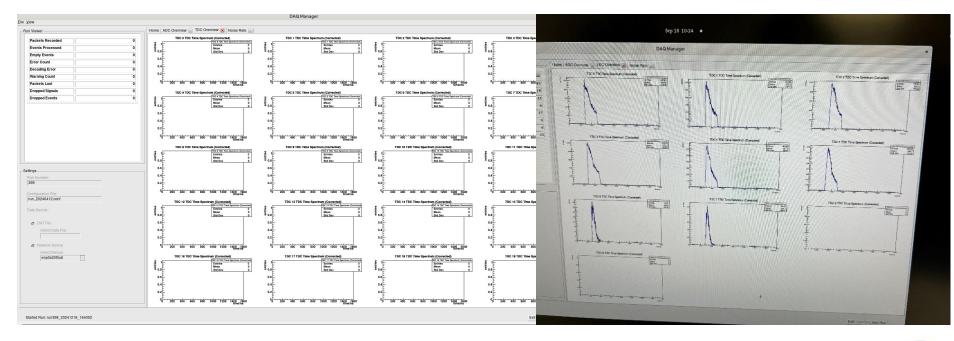
MiniDAQ configuration GUI

- Auto scan all connected mezzanine (blue=connected, gray=unconnected)
- JTAG configuration verification for TDC and ASD (green=success, red=failure)

	MiniDAQ	Single Mezz Config ×										
	LpGBT Config SCA Monitor Mezz Config	TDC Configuration										
	✓ All CSM0	Mezz Scan TDC Setup0										
	Mezz 0 🗸 Mezz 1 Mezz 2 🗸 Mezz 3 Mezz 4 🗸 Mezz 5 Mezz 6 Mezz 7 Mezz 8 🗸 Mezz 9	write_TDC_all TDC Setup1										
Main Tab		write_ASD_all TDC Setup2										
	Mezz 10 Mezz 11 Mezz 12 Mezz 13 Mezz 14 Mezz 15 Mezz 16 Mezz 17 Mezz 18 Mezz 19	TDC_input_disable TDC Control0										
		TDC_input_enable TDC Control1 2nd level popup										
	✓ All CSM1	TDC_setup ASD Configuration										
	Mezz 20 Mezz 21 Mezz 22 Mezz 23 V Mezz 24 V Mezz 25 Mezz 26 Mezz 27 Mezz 28 Mezz 29											
		ASDO Setup (0~ 7)										
	Mezz 30 Mezz 31 Mezz 32 Mezz 33 Mezz 34 Mezz 35 V Mezz 36 V Mezz 37 Mezz 38 Mezz 39	ASD1 Setup (8~15)										
		ASD2 Setup (16~23)										
	clear info	TDC Setup0 ×										
	Output Log											
	2024-12-18 15:49:52>>Valid TDI ASD2 DR seq: 000000000000000001110100001110010000000											
	Mezz Config enable_legacy full_width_res	enable 8b10b enable insert enable error packet										
	Mezzo Mezz1 Mezz3 Mezz4 Mezz5 Mezz6 Mezz7 Mezz8 M chable_error_notify	width_select 001 - 3rd level popup										
1st level p	DepupMezz11 Mezz12 Mezz13 Mezz14 Mezz15 Mezz16 Mezz17 Mezz18 Me											
		16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0										
	Mezz20 Mezz21 Mezz22 Mezz23 Mezz24 Mezz25 Mezz26 Mezz27 Mezz28 Me channel_enable_r all											
	Mezz30 Mezz31 Mezz32 Mezz33 Mezz34 Mezz35 Mezz36 Mezz37 Mezz38 Me	<u>v</u> 16 <u>v</u> 15 <u>v</u> 14 <u>v</u> 13 <u>v</u> 12 <u>v</u> 11 <u>v</u> 10 <u>v</u> 9 <u>v</u> 8 <u>v</u> 7 <u>v</u> 6 <u>v</u> 5 <u>v</u> 4 <u>v</u> 3 <u>v</u> 2 <u>v</u> 1 <u>v</u> 0										
	Save_setup Load_setup Save_default Load_default											
		V 16 V 15 V 14 V 13 V 12 V 11 V 10 V 9 V 8 V 7 V 6 V 5 V 4 V 3 V 2 V 1 V 0										

MiniDAQ online monitor GUI

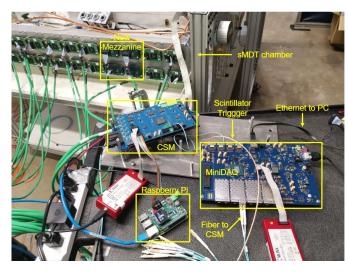
- Online monitor GUI Based on ROOT
- Real time spectra and hit rate display
- Warning/error info display (from decoded data)
- Examples shown below are the online dispay in the straw test beam experiment in Sept. 2024



MiniDAQ implementation

The system has been successfully used in:

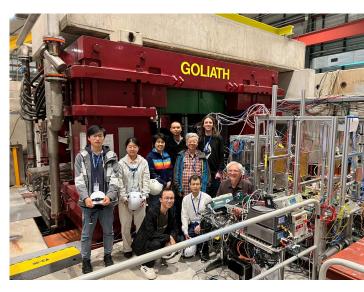
- Michigan sMDT construction commissioning for 50 chambers
- MDT chamber cosmic test with new mezzanine, CSM, CSM-MB for Phase 2 upgrade
- CERN GIF++ test beam study for sMDT under high gamma rate (July 2021)
- CERN DRD1/WP3 test beam study for straw chamber (September-October, 2024)



sMDT construction commissioning



Testing at CERN GIF++



Testing at CERN H4 and T9

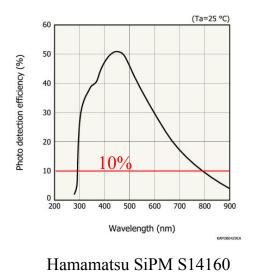


SiPM vs PMT

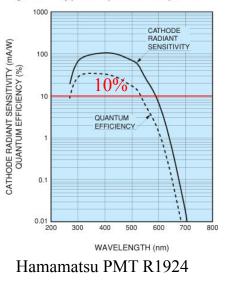
Why using SiPM?

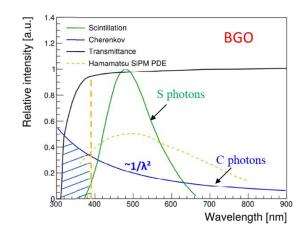
- Broader photo detection efficiency in wavelength (covers Cherenkov light)
- Not sensitive to magnetic field
- Small unit size (usually 1mm*1mm), not easy to break

Photon detection efficiency vs. wavelength (typi









SiPM vs PMT

Why using SiPM?

- Comparable gain (10⁶)
- Significant lower bias voltage (usually <70 V)
- Comparable rise time (slow fall time though)

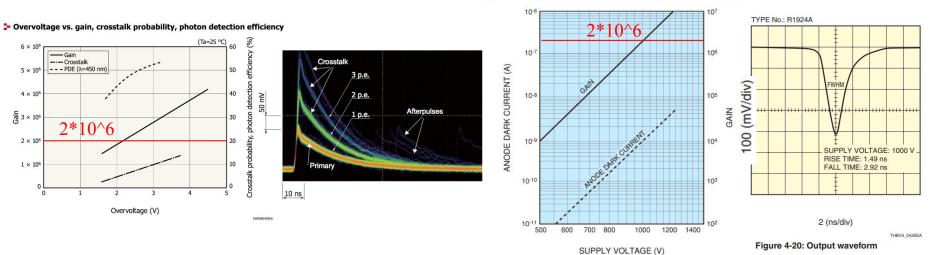


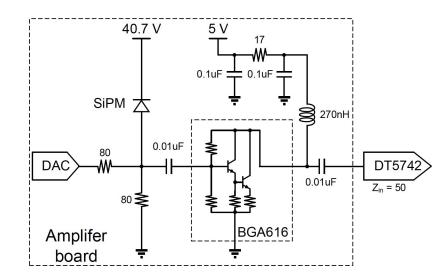
Figure 2: Typical gain and dark current character

Hamamatsu SiPM S14160

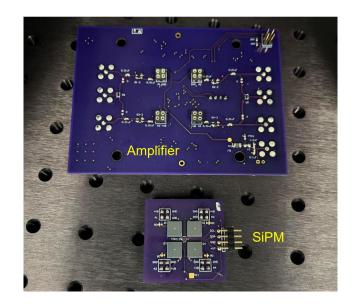
Hamamatsu PMT R1924

SiPM readout in FCC-ee R&D CalVision dual readout project

- Boards designed by the University of Virginia group
- Four S14160-6050HS (6 x 6 mm2) SiPMs on board, micro-cell pitch 50 um
- Single-stage RF amplifier for each channel (gain ~10)
- Domino-ring sampler4 (DRS4) digitizer, 5 Gsps, 200 ns window, 16+1 channel maximum



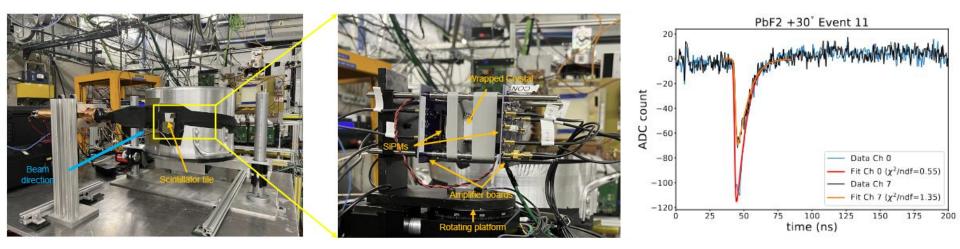
Single-channel schematic



4-channel amplifier board and SiPM board

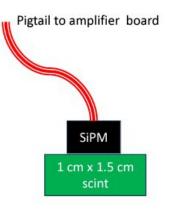
Test beam study for PbF₂ at Fermilab

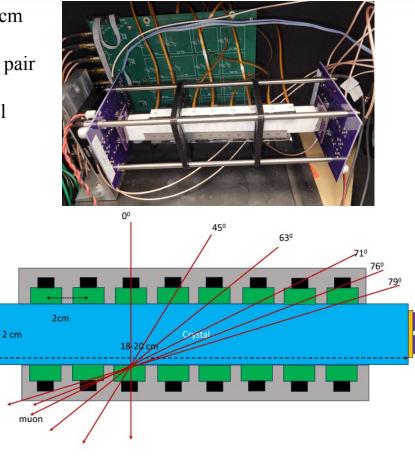
- PbF₂ crystal sits on a rotating platform
- Angular dependence studied for Cherenkov light with SiPM waveform
- If only leading edge info is needed (waveform digitization not required), can use MiniDAQ system as readout (such as scintillator strips with SiPM)



Angular study with cosmic ray

- 1 cm * 1.5 cm scintillator tile coupled with SiPM, spaced 2 cm apart along the crystal long surface as trigger
- Incident angle can be defined when choosing desired SiPM pair as coincidence trigger
- SiPM signal and bias routed out to amplifier board by pigtail cable
- Amplifier board designed by Fermilab





Summary

- MiniDAQ is a lightweight readout system, currently used for ATLAS MDT phase 2 upgrade chamber commissioning
- 960 channel basic, 1920 channel with expandable port, MiniDAQ can easily handle one or more drift chamber
- SiPM readout has been studied for CalVision dual readout
- Same scheme can be adopted for scintillator tiles coupled with SiPM and readout by MiniDAQ