Timing layer design and plans

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US Higgs Factory Planning
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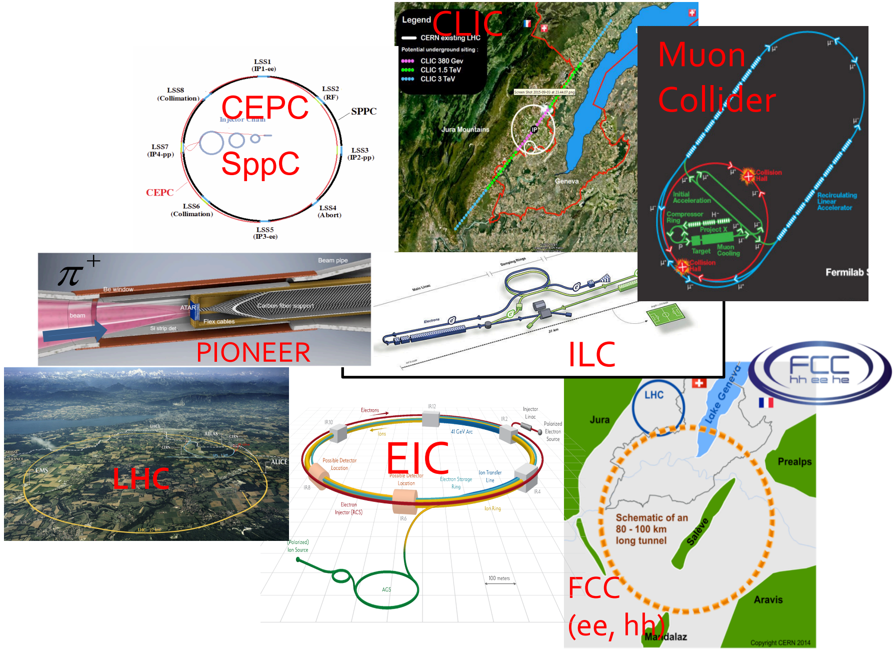
SLAC

The rise of 4D detectors

❖ **As 4D detector Technologies are becoming more advanced, we realize their benefit in collider experiments**

- **Pileup** suppression at hadron colliders
- Timing useful input to **Particle Flow** algorithms
- Timing as additional information from the **Calorimeters**: identification of slow from prompt shower components
- **PID capabilities/ Time-Of-Flight** across a wide momentum range is essential: flavor physics, H→ss…
- **Identify long-lived particles (LLPs)** and expand the reach for new phenomena
- Suppress **out-of-time Beam Induced Backgrounds** (e.g. Muon Collider)

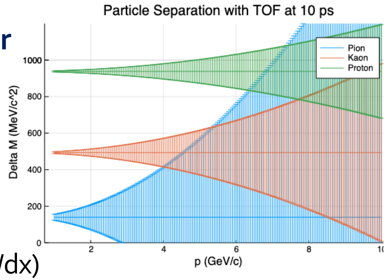


➢ Silicon technologies can meet the need for 4D detectors at Future Higgs Factories experiments

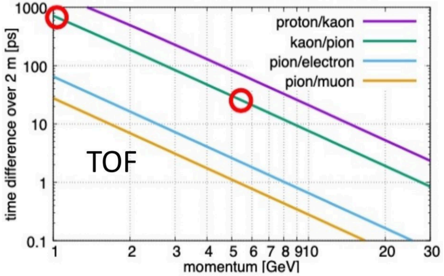
Timing Layer Specifications

- Large-radius timing layers in front of the calorimeter can provide Time-of-Flight (ToF) for PID
  ➔ Flavor physics, H→ss

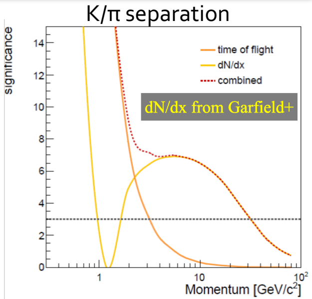
- **Need 10 ps resolution over 2 m lever-arm for K/π separation at low momentum (up to ~4-5 GeV)**
  - Drift chamber: PID by dE/dx or cluster counting (dN/dx)
    - 3σ for K/π separation up to 35 GeV
    - Complemented with TOF for hole at 1 GeV



Study for SiD at ILC (arXiv:2110.09965)



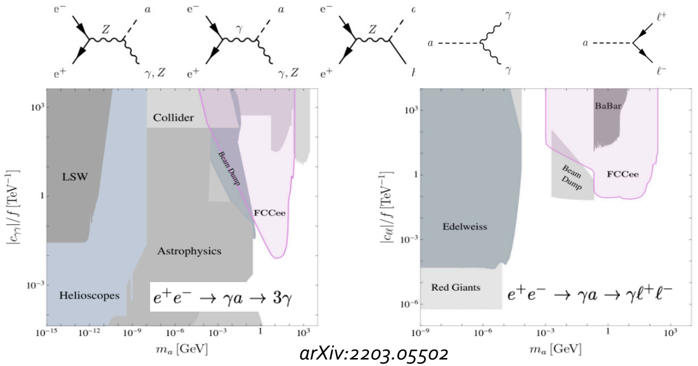
N. Morange,
https://indico.mit.edu/event/876/contributions/2672/attachments/1042/1708/allegro-concept.pdf



P. Giacomelli,
https://indico.mit.edu/event/876/contributions/2670/attachments/1034/1765/IDEA_detector-concept-FCC-US-2024.pdf

- **Exploit high luminosity Z run of FCC-ee to search for LLP**:
  - Heavy Neutral Leptons
  - Axion-like particles
  - Exotic Higgs decays
- **Timing information:**
  - Simultaneous determination of mass and proper decay time combining decay path and ToF
  - Combination with displaced vertex reconstruction for enhanced performance

Ariel Schwartzman,
https://indico.slac.stanford.edu/event/8992/contributions/10627/attachments/4753/12818/4DTracking_physics.pptx.pdf

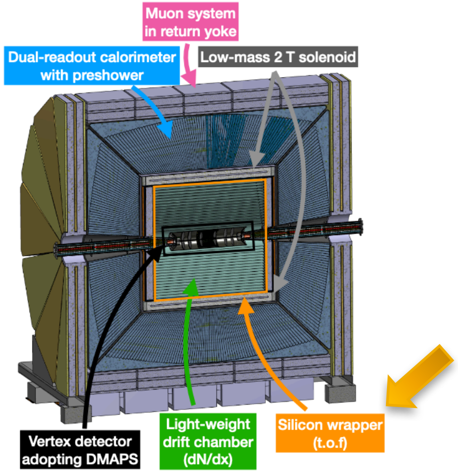


arXiv:2203.05502

Current Silicon Wrapper Design

***ALLEGRO** Detector Concept (FCC-ee)*

***IDEA** Detector Concept (FCC-ee)*



In Simulation (Full-Sim):

Barrel

	R [mm]	L [mm]	Si eq. thick. [μm]	X0[%]	Pixel size [mm^2]	area [cm^2]	# of channels
Layer 1	2040	±2400	450	0.5	0.05×100	616K	12.3M
Layer 2	2060	±2400	450	0.5	0.05×100	620K	12.4M

Endcap

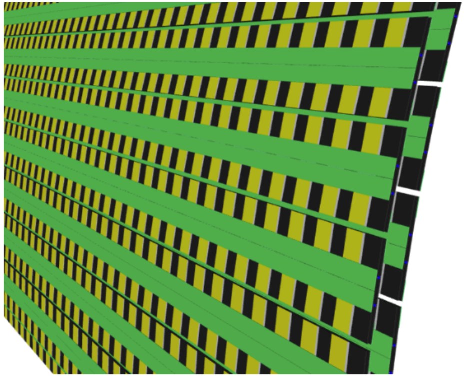
	R^{in} [mm]	R^{out} [mm]	z [mm]	Si eq. thick. [μm]	X0[%]	Pixel size [mm^2]	area [cm^2]	# of channels
Disk 1	350	2020	±2300	450	0.5	0.05×100	250K	5M
Disk 2	354	2020	±2320	450	0.5	0.05×100	250K	5M

https://fcc-ee-detector-full-sim.docs.cern.ch/IDEA/

❖ Tracking Information
- Improve momentum resolution thanks to long lever arm
- Extend tracker coverage in forward regions
- Precise and stable ruler for acceptance definition

- Covered area: ~100 m^2
- Low material budget: ~ 1% X/Xo
- Two barrel layers and two disks, to have at least one silicon hit, but most of the cases we have two silicon hits
- Multi-module tiles on staves (ATASPIX3 quad module concept)
- No detailed layout of the mechanical structure yet

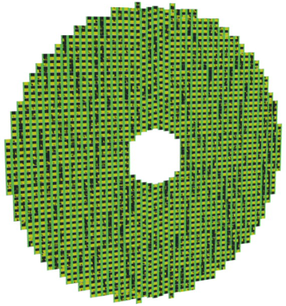
Current Silicon Wrapper Design



Two layers to cover gaps

Disks:

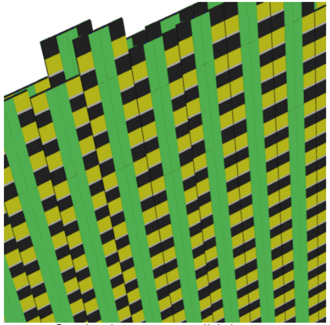
- Tiling the disks with tiles of 6, 12 and 24 modules
  ➔ Total of 30,432 modules



One disk

Front

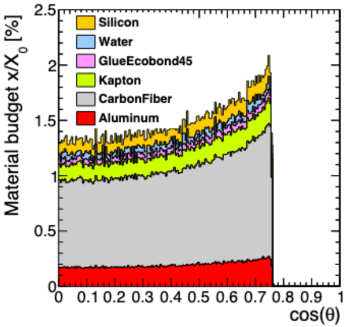
Back

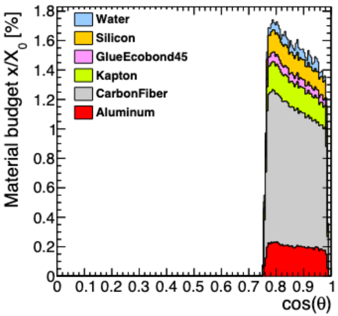


Overlap between two disk layers

Barrel:

- Each stave is a long tile
- Each layer made up of 151 staves with 129*2 modules
  ➔ Total of 77,916 modules





Material:

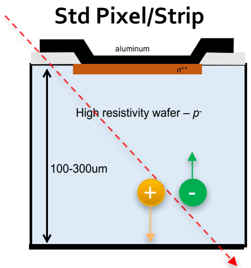
- Flex and cooling pipes (same as in vertex outer barrel and disk)
- 50 µm silicon
- 1.4 mm of carbon fibre

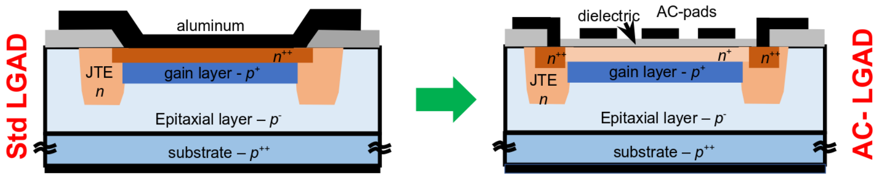
Detector Technologies for Si-Wrapper

❖ **Proposed detector technologies for Si-Wrapper: Strips**

- **Microstrips** (available) ← Tracking only
- **DMAPS** (advanced) ← Low mass tracking
- **LGAD** (advanced) ← Timing in addition to Tracking (4D)
- ***Monolithic LGAD !?*** *(interesting idea)* ← *4D + Low mass*

Adding timing capabilities to Si-Wrapper comes with limited extra effort/resources

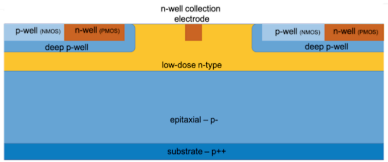




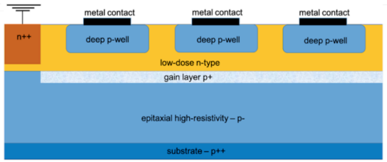
Large pads (~1 mm²) → Timing only

Can be finely pixelated → Time+Space (4D)

➢ **100% fill factor and fast timing information at a per-pixel/strip level → 4D**



CMOS sensor



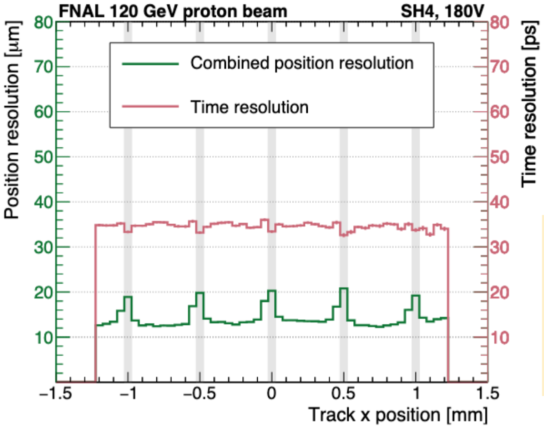
Monolithic AC-LGAD

➢ **4D detector capabilities as an AC-LGAD + readout circuitries in same substrate**

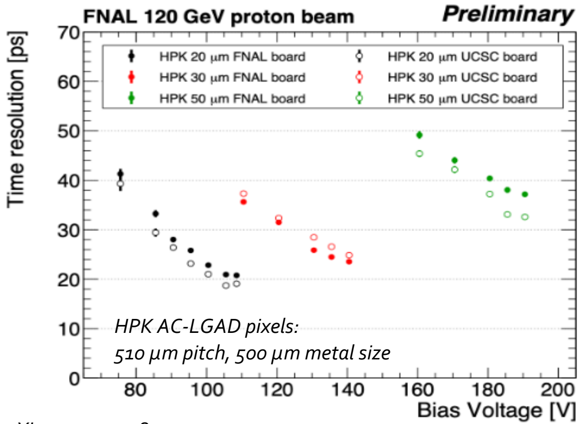
LGAD Sensor Performance

❖ **Long AC-LGAD strip sensors performance**

- **Position reconstruction**
  - Achieve **15-20 µm** resolution in *1 cm strips, 500 µm pitch*
  - ➔ Same resolution as microstrips with larger pitch
- **Excellent time resolution**
  - Achieve **30-35 ps** for *1 cm strips, 50 µm active thickness*
  - ➔ Same time resolution as LGAD



Signal shared between neighboring electrodes in AC-LGADs:
Measure position based on signal ratios



arXiv:2407.09928

- **AC-LGAD with smaller thickness: 20, 30 µm**
  - Faster Rise-Time
  - Time resolution improves with smaller active thickness
  - For 20 µm time resolution <20 ps

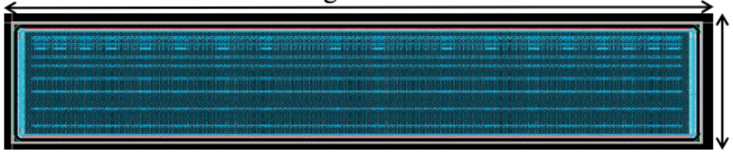
➢ **Fast-time readout ASICs for 4D detectors are also becoming available**

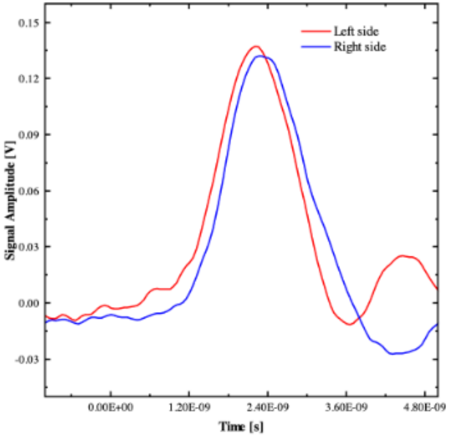
LGAD Sensor Performance

❖ Long LGAD strips can be read from both ends ➔ longer strips

original idea by UCSC

- **Position reconstruction**
  - Based on time-lag between two ends
  - Good linearity
  - Position resolution along z~0.9 mm (intrinsic 5.5 mm) for a total strip length of 19mm
- **Time resolution**
  - Achieve ~37 ps with 19 mm strip length





Waveform Variation at two ends

Weyi Sun
https://indico.cern.ch/event/1439336/contributions/6242215/attachments/2977964/5243205/4d_aclgad_swy_7.pdf

4D Detector Challenges

- **Complexity**
  - Short strips (~1-2 cm) are needed for good timing
  - Many readout channels
- **Material Budget**
  - Silicon detector adds considerable material before calorimeter
  - Can be minimized with monolithic technologies
- **Readout**
  - Advanced 4D ASICs are needed (under development)
  - Power consumption depends on technology used
- **Cooling**
  - Depending on technology, active cooling may be needed
- **Costs**
  - Large surface area for silicon
  - Development of advanced electronics

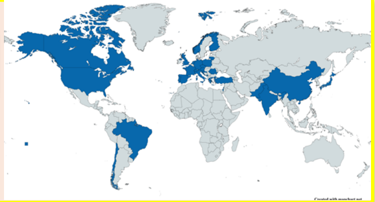
→

- No showstoppers
- Progress is made fast in this field
- Large interested community: multiple scientific applications
- We have time and human resources for innovation

Synergies

DRD3
Semiconductor Det.
https://drd3.web.cern.ch/

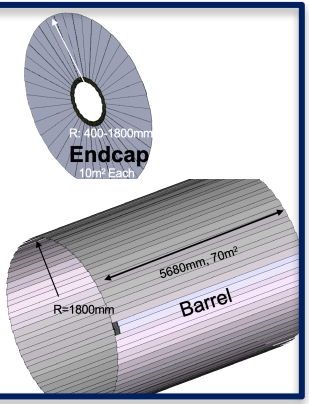
- 143+ institutions
- 600++ people



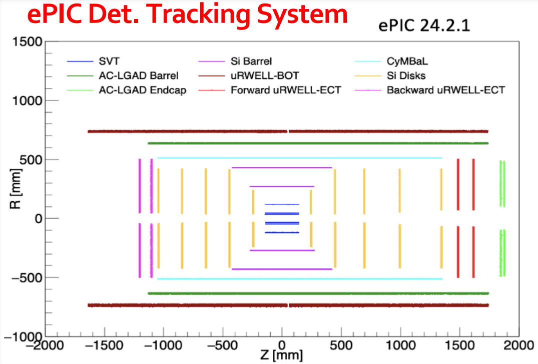
WG2 research goals <2027	
	Description
RG 2.1	Reduction of pixel cell size for 3D sensors
RG 2.2	3D sensors for timing ($\leq 55 \times 55$ μm, < 50 ps)
RG 2.3	LGAD for 4D tracking < 10 μm, < 30 ps, wafer 6” and 8”
RG 2.4	LGAD for ToF (Large area, < 30 μm, < 30 ps)

Design target of CEPC ToF Barrel

Area	~ 70 m^2
Radius	1.8m
Length	5.8m
Strip Length	20 mm (to be determined)
Strip Pitch	100-500 µm (to be determined)
Channel number	~ 10^7 channels
MIP Time resolution	~50 ps
Spatial resolution	~ 10 µm (R-Φ)

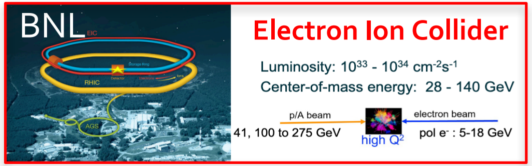


ePIC Det. Tracking System



❖ **AC-LGAD:**

- **PID Time of Flight** detectors to cover PID at low pT
  - Also provide time and spatial info for tracking
  - Resolution: ~30 ps, 30 um (with charge sharing)
- **Barrel (BTOF):** 0.05 x 1 cm strip, 1% X/Xo
- **Forward disk (FTOF)** : 0.5 x 0.5 mm² pixel, 8% X/Xo
- **Far-Forward Detectors:** Luminosity Monitor (strips), Bo (pixels), Roman Pots (pixels)
- **ASICS** being developed



Opportunities

- ❖ The Silicon Wrapper a 4D detector (Time+Space)
  - Adding time information comes with small overhead to tracking, and may reduce with AC-LGADs channel count with same tracking resolution
- ❖ More extensive 4D capabilities
  - Timing in calorimeter, e.g. Crystal ECAL + Timing Layer?
- ❖ Other experiments and R&D are stepping stones and opportunities for collaborations (HL-LHC, ePIC, CEPC, DRD3, RDC)
  - Work collectively on common challenges
- ❖ Great opportunity for innovation
  - Let's be ambitious!
  - High risk & high returns

Activity Focus:

1. **Define performance specifications based on physics benchmark processes**
   - Strong physics case must be made for timing layer
2. **Narrow-down technologies based on physics specifications**
3. **Layout optimization**
   - Strip length, pitch → reduce complexity (e.g. no. of channels)
   - Module, Tile, Stave layouts (experience from LHC)
4. **Sensor R&D**
   - Thin & Fast (~20 ps),
   - Precise Tracking (~10 μm)
5. **Readout Challenges**
   - Low power, low jitter, TDC/ADC, pulse sampling, ML?
6. **Mechanical Challenges**
   - Minimize support material but preserve reliability
   - Cooling

Interests from US Institutes (FCC-ee EoI list):

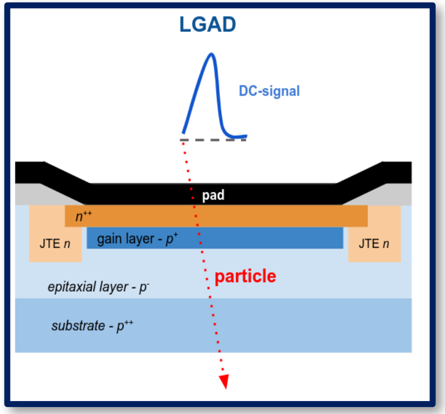
- **Timing/LGADs in Vertex Det and Si-Wrapper+TOF**
  - BNL, FNAL, Boston U., SCIPP, U. New Mexico, SLAC, ORNL
- **Calorimeter:**
  - SLAC

Conclusions

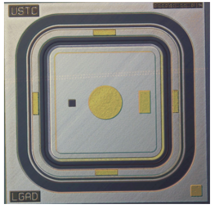
- R&D to investigate the **full potential of fast timing detectors at future Higgs Factories** is an exciting opportunity for the particle physics community
- **Silicon Wrapper** in IDEA and ALLEGRO is a great opportunity for innovation in 4D technologies
- **Physics case for timing layers** is to be strengthened
    - Specifications need to be defined
- **R&D on 4D detectors is world-wide** and we can leverage other projects and scientific applications
    - The US can **focus on strategic R&D** that complements international developments
        - Specific deliverables, e.g. 4D Silicon Wrapper
            - Define goals, specs, layout
            - Study physics performance
        - Development of specific/complementary technologies, foundries and processes for sensors and chips
            - e.g. AC-LGAD, monolithic sensors
            - e.g. low power 4D ASICs
- **Let's be ambitious and focused!**

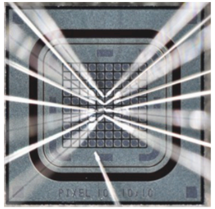
Backup

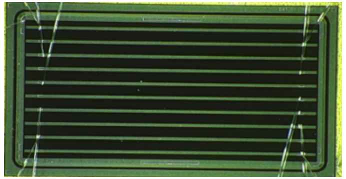
LGAD Technologies



- **Low Gain Avalanche Diode (LGAD) is advanced technology for precision timing**
  - Used in ATLAS and CMS for HL-LHC timing detectors
  - Several foundries in China, Europe, US and Japan
- **Thriving field of research for 4D detectors: pixels or strips with various processes**

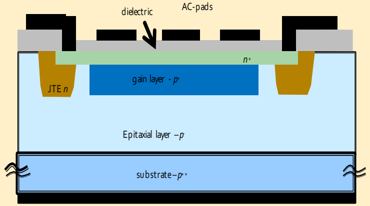






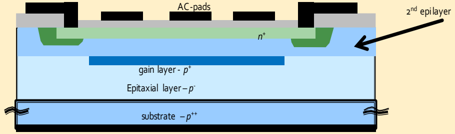
AC-LGAD

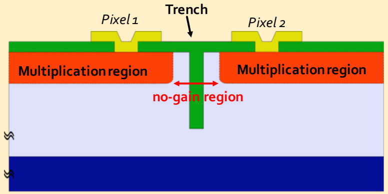
100% fill factor, excellent spatial resolution with signal sharing, for low interaction rates



Deep-Layer AC-LGAD

an AC-LGAD with higher rad-hardness



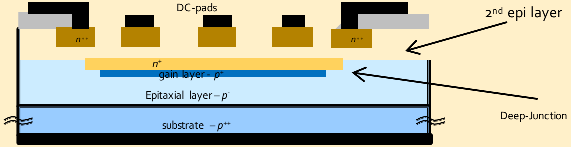


Trench-Isolation LGAD

~100% fill factor, signal in single pixel (no share)

Deep-Junction LGAD

Position resolution given by pitch, as in std pixels/strips



DRD WG2 – Readout Challenges

- **ASICs for HL-LHC Timing detector (pitch of 1.3 mm x 1.3 mm):**
  - **ATLAS HGTD** ***ALTIROC*** chip in 130 nm CMOS
  - **CMS ETL** ***ETROC*** chip in 65 nm CMOS

- **From the ECFA Roadmap: Technology Choice**
  - The selection and adoption of the *28 nm CMOS* technology as a "mainstream" process will "fuel" the developments of "near-future" experiments
  - A few chips are being developed at the moment for *4D tracking*:
    - *Ignite* and *PicoPix*, focused on LHCb VELO upgrade in 28 nm CMOS
    - *EICROC* for ePIC detector at EIC in 130 nm CMOS
    - Fermilab's *FCFD* for 4D trackers in 65 nm CMOS Etc.
  - but nothing readily available at the moment

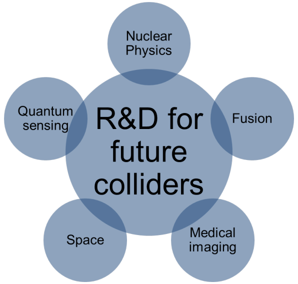
❖ DRD3 WG2 will help to collect requirements for future ASICs and unify efforts

Monolithic Detectors

Chip name	Experiment	Subsystem	Technology	Pixel pitch [μm]	Time resolution [ns]	Power Density [mW/cm²]
ALPIDE	ALICE-ITS2	Vtx, Trk	Tower 180 nm	28	< 2000	5
Mosaic	ALICE-ITS3	Vtx	Tower 65 nm	25x100	100-2000	<40
FastPix	HL-LHC		Tower 180 nm	10 - 20	0.122 – 0.135	>1500
DPTS	ALICE-ITS3		Tower 65 nm	15	6.3	112
NAPA	SiD	Trk, Calo	Tower 65 nm	25x100	<1	< 20
Cactus	FCC/EIC	Timing	LF 150 nm	1000	0.1-0.5	145
MiniCactus	FCC/EIC	Timing	LF 150 nm	1000	0.088	300
Monolith	FCC/Idea	Trk	IHP SiGe 130 nm	100	0.077 – 0.02	40 - 2700
Malta	LHC, ..	Trk	Tower 180 nm	36x40	25	> 100
Arcadia	FCC/Idea	Trk	LF 110 nm	25	-	30

C. Vernieri: https://indico.mit.edu/event/876/contributions/2694/attachments/1039/1721/MIT-workshop-Detector.pdf

CERN's DRD Collaborations



ECFA Detector R&D Roadmap

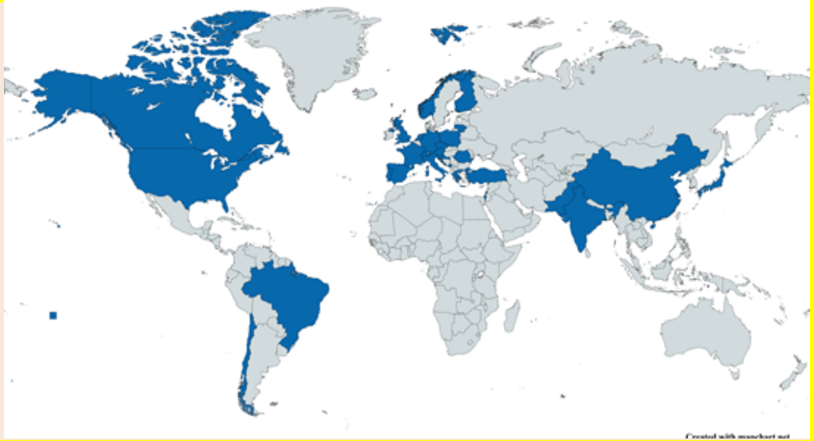
Detector R&D (DRD)

- **DRD1** Gaseous Det.
- **DRD2** Liquid Det.
- **DRD3** Semicond. Det.
- **DRD4** Photo-Det./PID
- **DRD5** Quantum Det.
- **DRD6** Calorimetry
- **DRD7** Electronics

DRD3
Semiconductor Det.

https://drd3.web.cern.ch/

- **143+ institutions**
- **600++ people**



DRD3 Working Group 2 (4D Hybrid Detectors)

❖ Broad scope:

- Sensors with *4D capabilities* foreseen in many systems, from *Time-of-Flight* systems with only 1-2 layers of sensors with the best possible timing resolution to large *4D trackers* with many layers.
- Two main technologies assumed in WG2: *3D and LGAD sensors* (in all their flavors)
- *Additional technologies* can be explored in the future if new ideas will come forward

❖ Challenges:

- **Hadron colliders:** high radiation levels and high occupancies
- **Lepton colliders:** requirement of low material budget and low power dissipation

Webpage (under development): https://drd3.web.cern.ch/wg2

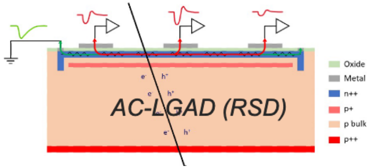
WG2 – Activities (LGAD detectors)

RG 2.3

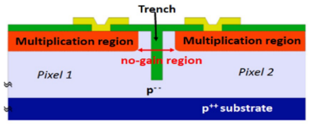
- **Full scale detector with pixelated LGAD sensors to achieve a position resolution <10 µm, with a timing resolution <30 ps before irradiation, also in high occupancy environments.**
  - Possible application for the replacement of outer pixel layers or disks in the CMS/ATLAS pixel dets. in Phase-III. Requested radiation tolerance for HL-LHC can be in the range of $1\text{-}5 \times 10^{15}\ n_{eq}/cm^2$

RG 2.4

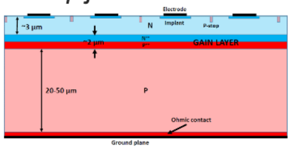
- **LGADs for particle identification (Time of Flight)**
  - Possible applications: *ALICE 3 (Run5), Belle2, Electron Ion collider (Tracking+TOF@ePIC) >2031) and Future Lepton colliders (>2040)*.
  - Larger surfaces (several m²) have to be covered
  - Yield and reproducibility of the process have to be demonstrated while radiation hardness is less of a problem
  - *Electron Ion Collider*: a spatial resolution ~30 µm and timing resolution <30 ps are required. An area up to 13 m² has to be instrumented. Proposal: pad size of 0.5 mm with a spatial resolution ~ 10 µm
  - *Future lepton colliders*: a ToF could be placed as the most external tracking layer, with a surface of around 100 m², < 30 ps, and spatial resolution ~10 (90) µm (r-ϕ, z).



Trench Isolated LGAD



Deep junction LGAD



Inverse-LGAD (I-LGAD)