MAPS developments

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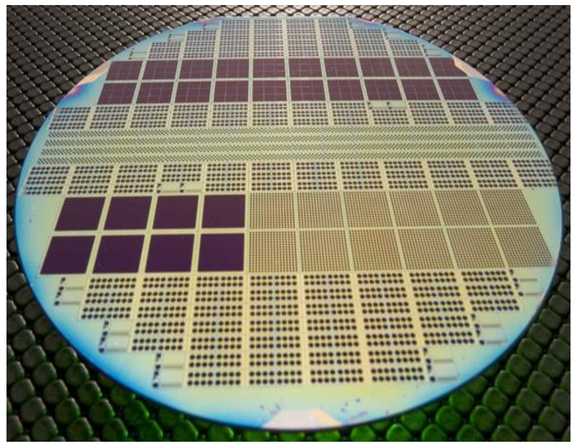
HFCC December 19, 2024

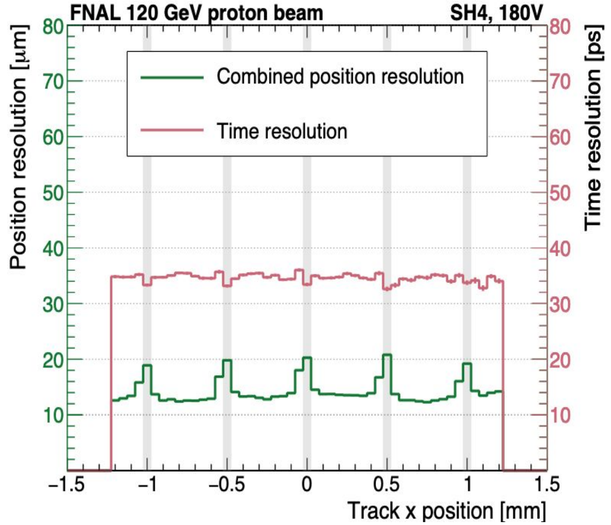
SLAC NATIONAL ACCELERATOR LABORATORY

Stanford University | U.S. DEPARTMENT OF ENERGY

Projects at Fermilab

- Build on technologies developed for CDF/D0, CMS, EIC, etc
  - Unique resource of strong instrumentation groups
  - Expertise in physics simulations and tracking reconstruction
- Fermilab is actively engaged in R&D on MAPS design
  - Sensor design, simulation studies, collaborations with vendors
  - Collaborative efforts with US and international universities
  - Extensive experience in characterization and testing, developments of electronics, testing infrastructure, DAQ
- Developments with **SkyWater** 90 nm process to demonstrate domestic production for future HEP experiments
- Developments with **INFN** on ARCADIA in 110nm: several demonstrators produced, very low-power 10 mW/cm^2





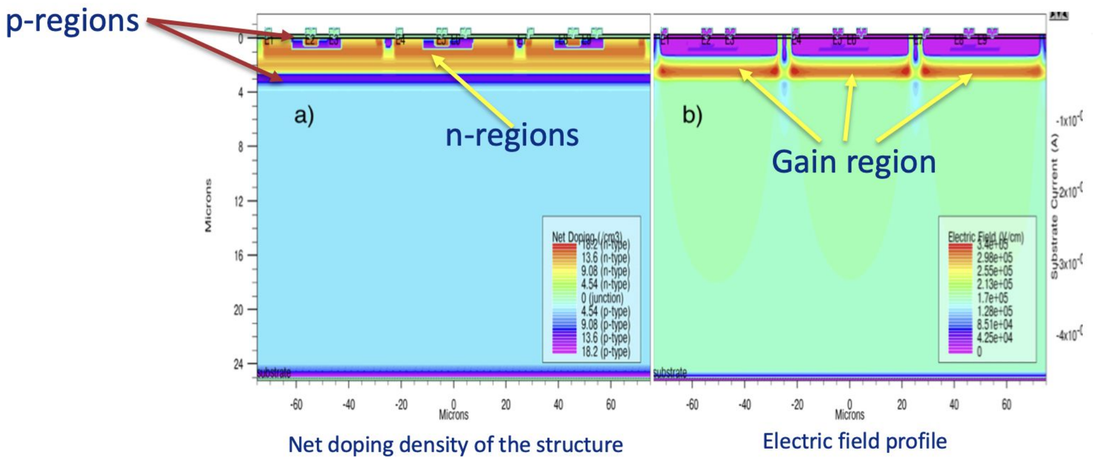
R&D program with SkyWater for FY25

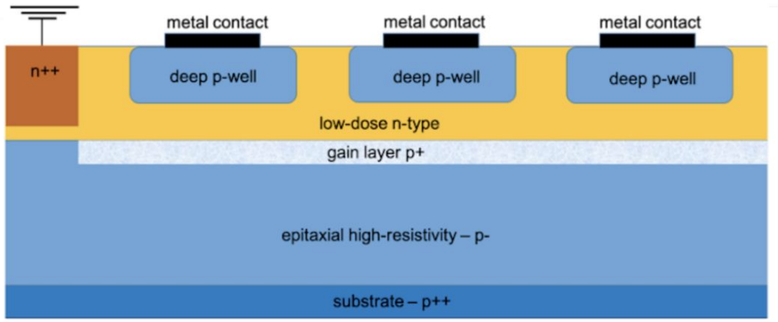
Collaboration with BNL, LBNL, UCSC, KEK

- Adapt and optimize SkyWater process to develop particle detectors
- Use thicker, higher-resistivity epitaxy with deep-well implants
- Optimize the design and geometry of AC-LGADs that will serve as the basis of the MAPS design.

Produce small-scale prototypes, from which the most promising architectures will be determined.

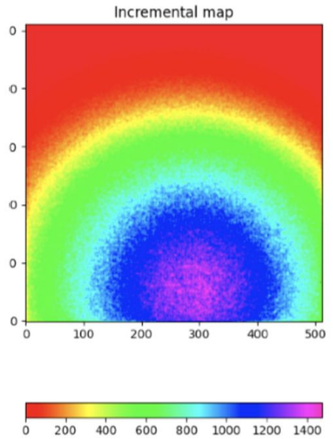
- Optimize isolation of signal collection from the readout electronics.

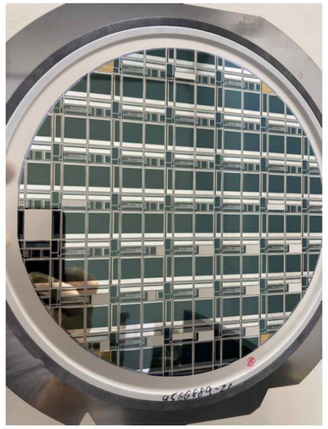


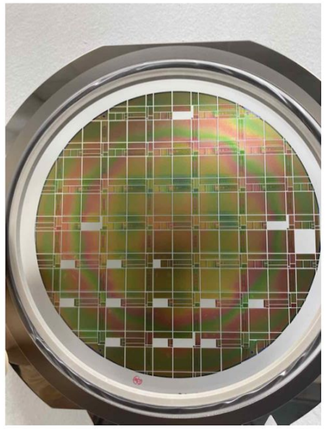


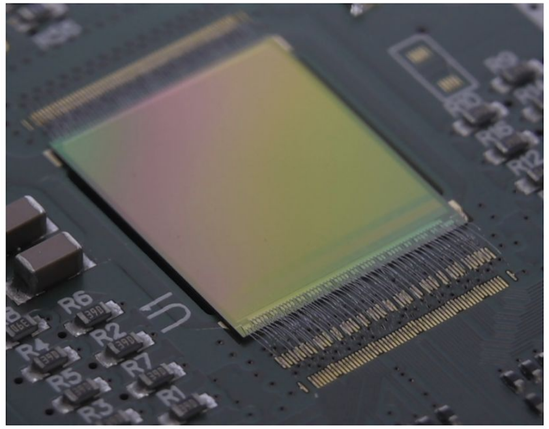
R&D program with ARCADIA

- Sensor design and fabrication platform on LF110 is technology
  - Full-chip FDMAPS for Future Lepton Colliders and Space Instruments
  - Scalable architecture with very low-power: 10 mW/cm^2
- Technology demonstrators
  - Main demonstrator (512 x 512 pixels) 25x25 μm^2 pixels
  - Several other demonstrators produced: pixel and strip test structures down to 10 μm pitch, small-scale demonstrator for fast timing, etc



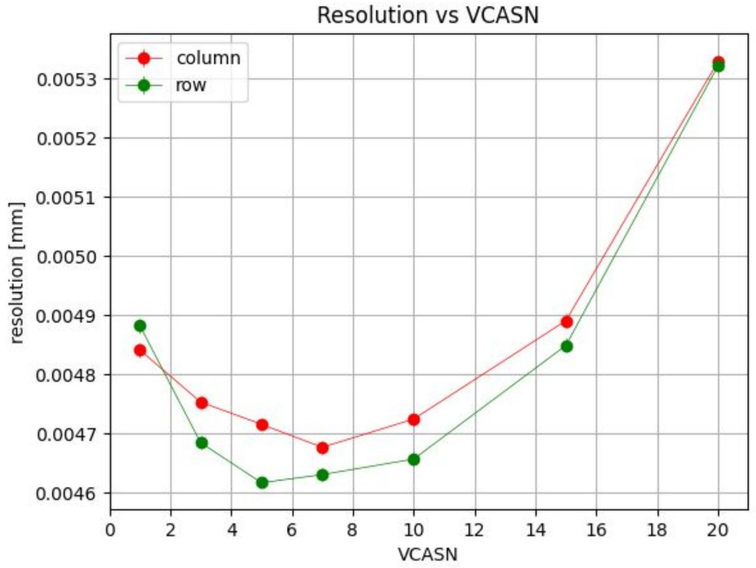


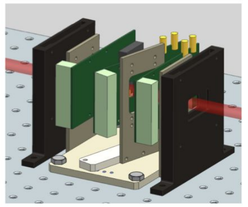


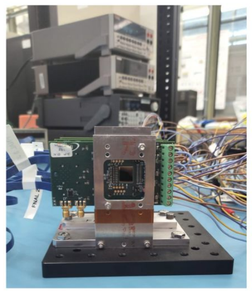


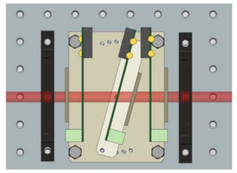
Characterization of ARCADIA-MD3

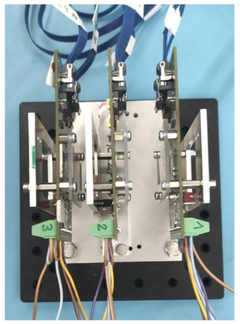
- Test beam at FNAL (120 GeV protons) in Summer 2024
- Excellent performance demonstrated in test-beam
  - Position resolution around 5 μm
  - Efficiency near 100%
- Detailed measurements are now continuing with laser
- Developments of the next round of prototyping is starting now

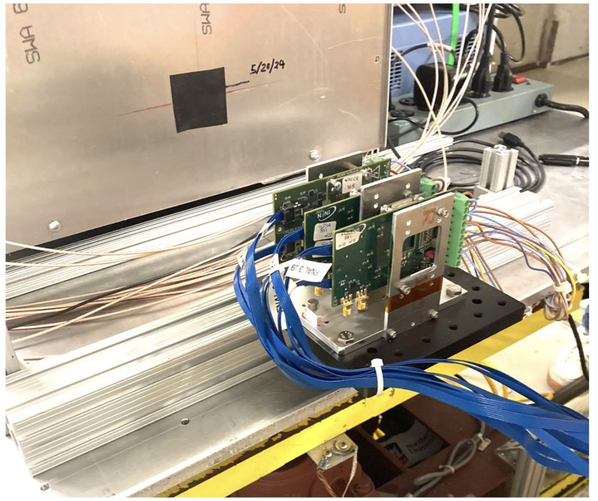












SLAC effort

Co-design approach: close interaction between physics studies and technology R&D [4]

- Novel CMOS process for MAPS has recently become available, CERN (WP1.2 Collaboration) provides access to scientific community: TowerJazz-Panasonic (TPSCO) 65 nm CMOS imaging process with modified implants
  - Builds on sensor optimization done for the TJ180 process[1-2], excellent charge collection efficiency and low capacitance [3]
  - Increased density for circuits: Higher spatial resolution, better timing performance at same power consumption.
  - Supports stitching: enable wafer-scale MAPS → **potential to greatly reduce costs of future experiments**
- ALICE ITS3 upgrade is the main driver of CERN WP1.2 efforts
  - SLAC is the only US institute involved in Enginering Runs fabrication
- Several challenges towards wafer-scale devices → **large international effort needed to address all of them**
  - Large collaboration is interested in designing solutions for power distribution compatible with stitching and enabling O(ns) timing precision

[1] M. van Rijnbach *et al.*, *Radiation hardness and timing performance in MALTA monolithic pixel sensors in TowerJazz 180 nm*, 2022 *JINST* C04034
[2] M. Munker *et al.*, *Simulations of CMOS pixel sensors with a small collection electrode, improved for a faster charge collection and increased radiation tolerance*, 2019 *JINST* 14C05013
[3] S. Bugiel *et al.*, *Charge sensing properties of monolithic CMOS pixel sensors fabricated in a 65 nm technology*, *NIMA Volume 1040, 1 October 2022, 167213*
[4] J. E. Brau et al., *The SiD Digital ECal based on Monolithic Active Pixel Sensors*, https://agenda.linearcollider.org/event/9211/sessions/5248, 2021.

Large area MAPS – Highlights & Next Steps

Approach:

- Focus on long-term R&D, targeting simultaneously:
  - ~ns timing resolution
  - Power consumption compatible with large area and low material budget
  - Fault-tolerant circuit strategies for wafer-scale MAPS

Highlights:

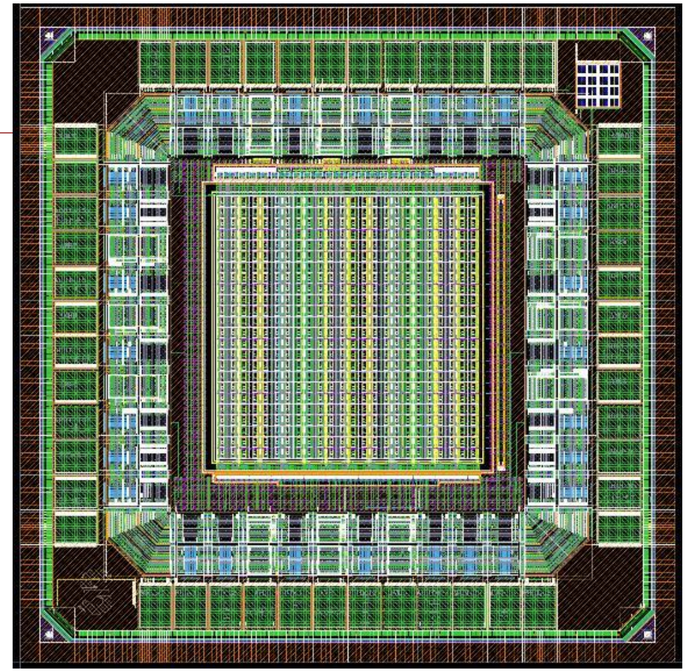
- 1st SLAC prototype on TJ65nm (2023) as part of a CERN WP1.2 shared run
  - NAPA_p1: NAnosecond Pixel for large Area sensors – Prototype 1
- 2st SLAC prototype on TJ65nm (2024) as part of a CERN WP1.2 shared run

Next steps:

- New design combining O(ns) timing precision and low-power (2024/2025).
- **Stretch Goals:** design of a wafer-scale ASIC (2025/2026, design only)

Engagement :

- DRD 7.6 on common issues of power distributions compatible with stitching



Layout of SLAC prototype for WP1.2 2022 shared submission on TowerSemi 65nm

Beam induced backgrounds at future HF

G. Marchiori (2023)
TDAQ@Annecy2024

Same tools and methodology between ILC & FCC within Key4HEP

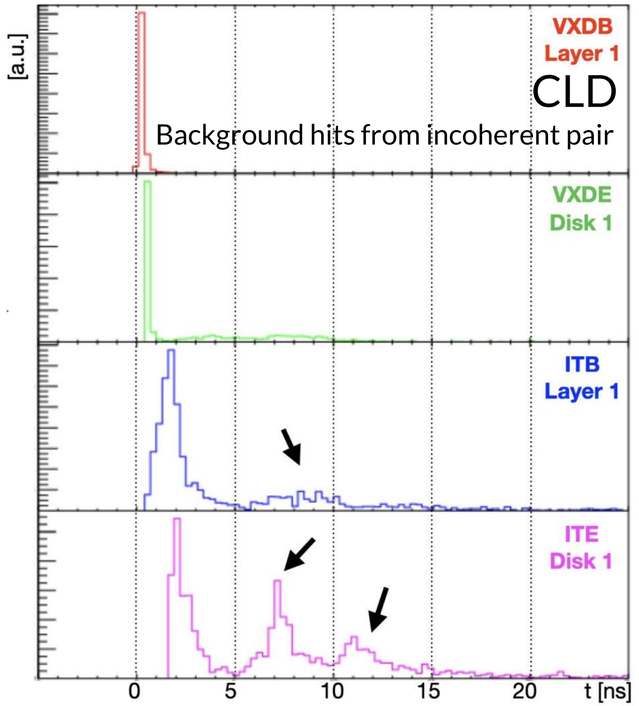
- ILC physics studies are based on full simulation data and some have been recently repeated for C^3
  - Time distribution of hits per unit time and area on 1st layer ~ $4.4 \cdot 10^{-3}$ hits/(ns · mm^2) ≈ 0.03 hits/mm^2 /BX
- CLD detailed studies @FCC show an overall occupancy of 2-3% in the vertex detector at the Z pole
  - assuming 10μs integration time

$$occupancy = hits/mm^2/BX \cdot size_{sensor} \cdot size_{cluster} \cdot safety$$

$$size_{sensor} = \frac{25\mu m \times 25\mu m\ (pixel)}{1mm \times 0.05mm\ (strip)} \qquad size_{cluster} = \frac{5\ (pixel)}{2.5\ (strip)} \qquad safety = 3$$

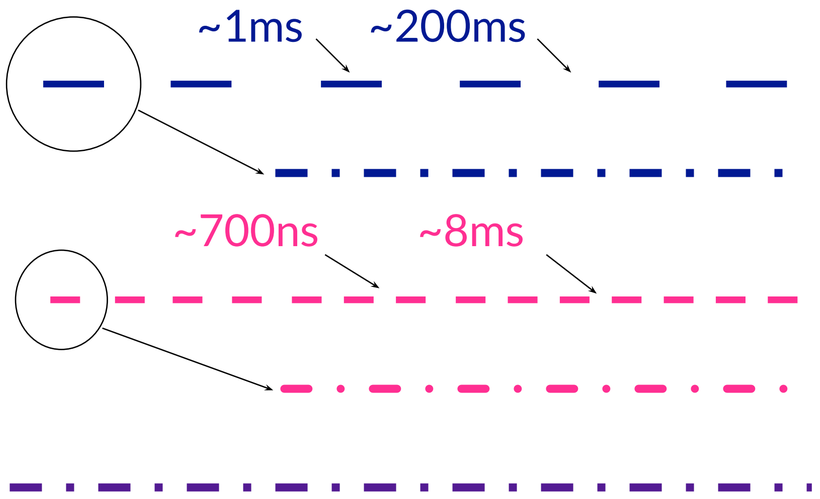
	Z	WW	ZH	Top
Bunch spacing [ns]	30	345	1225	7598
Max VXD occ. 1us	2.33e-3	0.81e-3	0.047e-3	0.18e-3
Max VXD occ.10us	23.3e-3	8.12e-3	3.34e-3	1.51e-3
Max TRK occ. 1us	3.66e-3	0.43e-3	0.12e-3	0.13e-3
Max TRK occ.10us	36.6e-3	4.35e-3	1.88e-3	0.38e-6

Occupancy in readout window (10μs)



Beam Format and Detector Design Requirements

arXiv:2003.0111
FCC Mid Term Report



ILC Trains at 5Hz, 1 train 1312 bunches
Bunches are 369 ns apart

C^3 Trains at 120Hz, 1 train 133 bunches
Bunches are 5 ns apart

FCC@ZH Bunches 1 μs apart
FCC@Z Bunches 20 ns apart

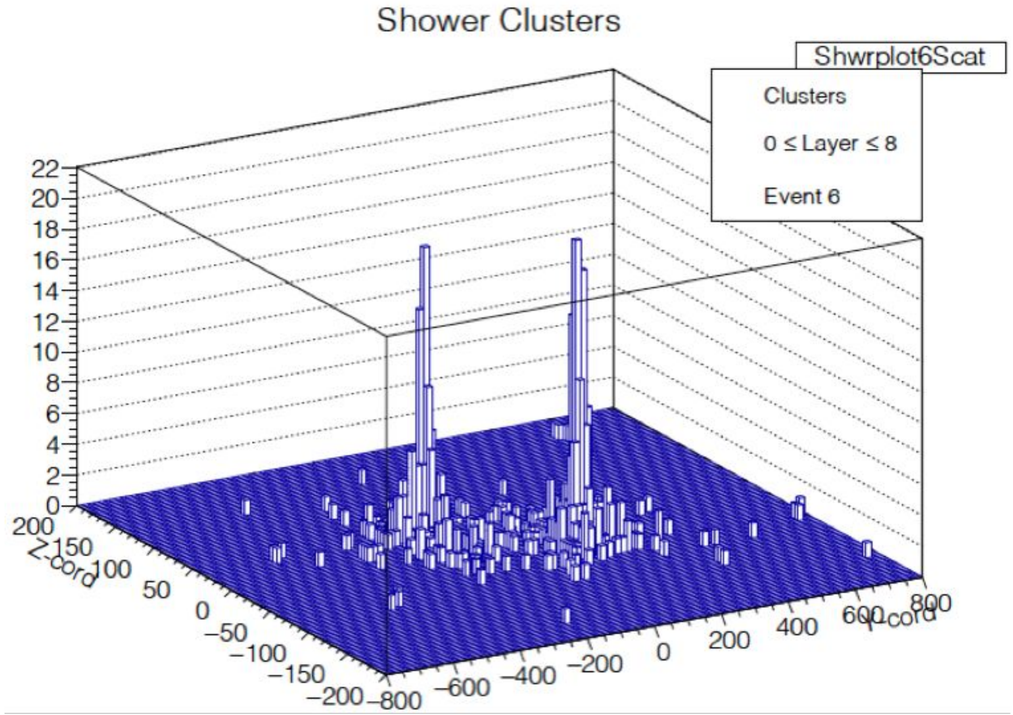
- Very low duty cycle at LC (0.5% ILC, 0.03% C^3) allows for trigger-less readout and power pulsing
  - Factor of 100 power saving for front-end analog power
  - **O(1-100) ns bunch identification capabilities**
- Impact of beam-induced background to be mitigated through MDI and detector design
  - Timing resolution of O(ns) can further suppress beam-backgrounds and keep occupancy low
  - **O(1-10) ns for beam background rejection and/or trigger decision before reading out the detector**
  - Tracking detectors need to achieve good resolution while mitigating power consumption

Instruments 2022, 6(4), 51

MAPS for ECal

Fine granularity allows for identification of two showers down to the mm scale of separation

- SiD detector configuration with 25x100 μm^2 pixel in the calorimeter at ILC
  - With no degradation of the energy resolution
- ***The design of the digital MAPS applied to the ECal exceeds the physics performance as specified in the ILC TDR***
- The 5T magnetic field degrades the resolution by a few per cent due to the impact on the lower energy electrons and positrons in a shower
- Future planned studies include the reconstruction of showers and π^0 within jets, and their impact on jet energy resolution



GEANT4 simulations of Transverse distribution of two 10 GeV showers separated by one cm

Target Specs vs. State of the Art

JINST 19 (2024) 04, C04033

Chip name	Technology	Pixel pitch [µm]	Pixel shape	Time resolution [ns]	Power Density [mW/cm^2]
Target Specification	?	25 x 100	Sq / rect	1	< 20
ALPIDE [2][3]	Tower 180 nm	28	Square	< 2000	5
FastPix [4][5]	Tower 180 nm	10 - 20	Hexagonal	0.122 – 0.135	>1500
DPTS[6]	Tower 65 nm	15	Square	6.3	53
Cactus [7]	LF 150 nm	1000	Square	0.1-0.5	145
MiniCactus [8]	LF 150 nm	1000	Square	0.088	300
Monolith [9][10]	IHP SiGe 130 nm	100	Hexagonal	0.077 – 0.02	40 - 2700

No design fulfills all target specification → The need to develop a custom design

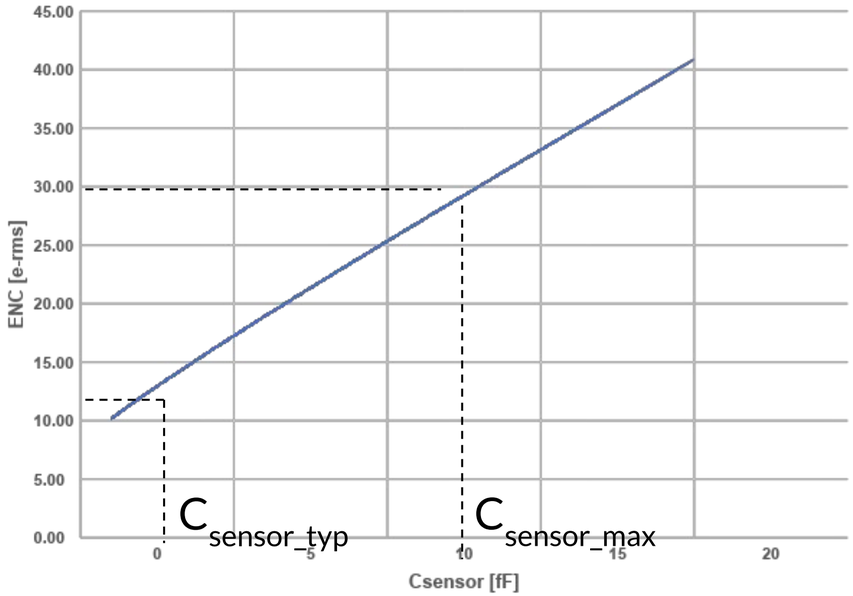
We decided to go with the Tower 65nm technology, which has been optimized by CERN WP1.2 to have low sensor capacitance allowing very good performance with low power consumption.
+ it has the possibility of a wafer-scale stitched sensor
+ it has been proven to be radiation tolerant

Summary of NAPA-p1 Performance

JINST 19 (2024) 04, C04033

	Specification	Simulated NAPA-p1
Time resolution	1 ns-rms	0.4 ns-rms ✓
Spatial Resolution	7 µm	7 µm ✓
Noise	< 30 e-rms	13 e-rms ✓
Minimum Threshold	200 e-	~ 80 e- ✓
Average Power density	< 20 mW/cm^2	0.1 mW/cm^2 for 1% duty cucle ✓

ENC = 13 e-rms for C_{sensor_typ} 2 fF

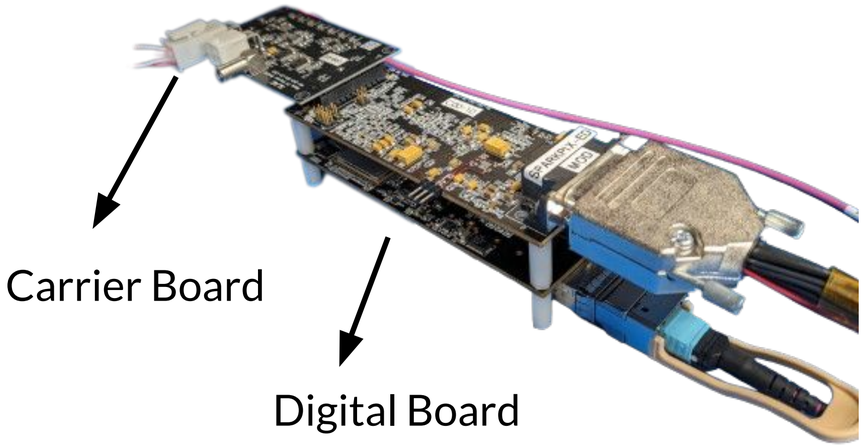


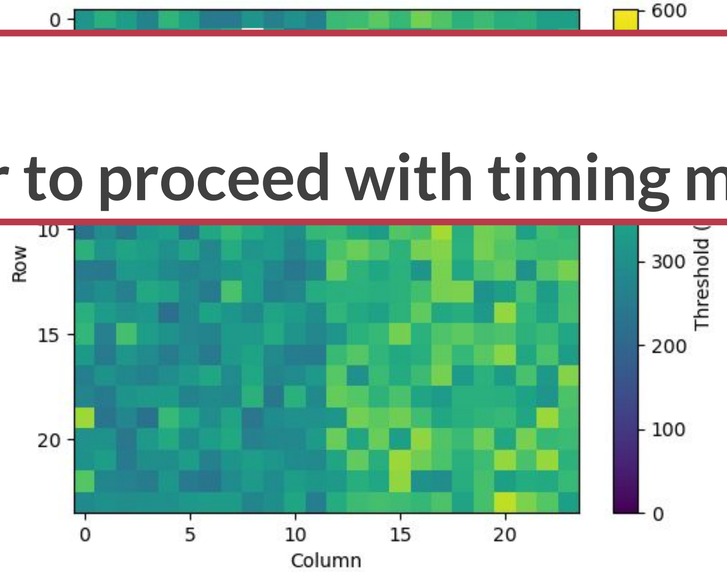
Acknowledgement: to CERN WP 1.2 for the excellent cooperation: NAPA-p1 uses the pixel masked developed and optimized by CERN, and was fabricated in a MLR led by CERN

Characterization of NAPA

- A custom carrier was designed at SLAC for the NAPA-p1 chip providing all analog references
- The chip was wire-bonded at SLAC
- The carrier boards connects to a digital board containing an FPGA and several DAC's

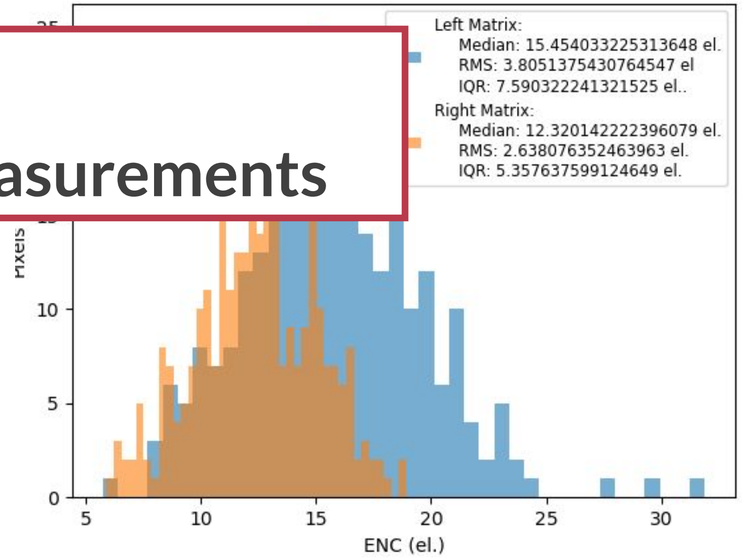
Acquired a laser to proceed with timing measurements





Left Matrix:
Nominal Pixel Variant

Right Matrix:
Pixel Variant with DC leakage current compensation

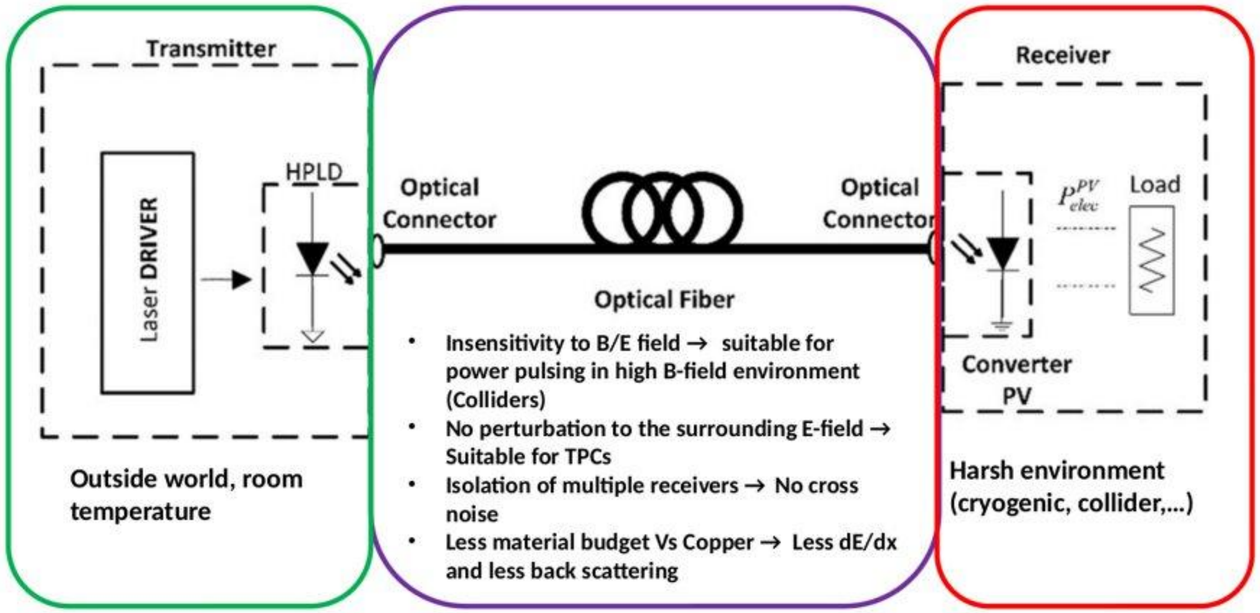


DC leakage current variant has less nosie

Power over fiber

New effort at SLAC targeting various experimental applications

- Power over Fiber (PoF) offers an innovative solution by delivering power through optical fibers, which are immune to electric and magnetic fields, and boast 1000X lower thermal conductivity compared to coax.
- We are developing radiation-hardened photonic links that can be used in future e+e- collider environments, where radiation levels can exceed 100 krad.
- This approach will investigate advanced photovoltaic materials like perovskites and their potential to surpass current GaAs-based photodiodes in power-to-weight ratio and radiation tolerance.



Strategic MAPS Development: FY24 Progress and FY25 Goals

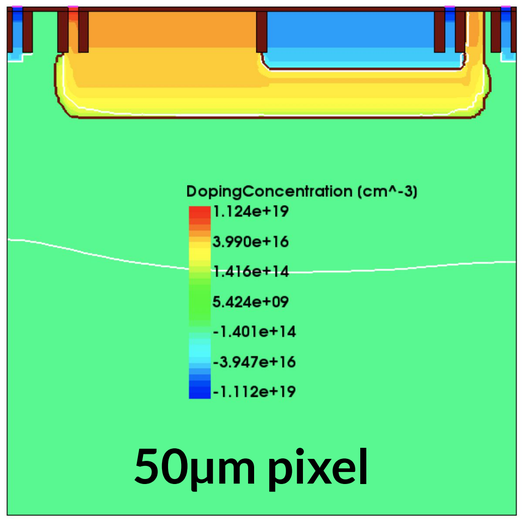
- The MAPS development program leverages international collaboration and unique US national lab capabilities.
  - In FY24, FNAL and SLAC teams achieved significant progress through design simulations, prototyping, and test-beam characterization.
    - Two foundries are being explored - a US based one in 110nm and TJ65nm within the CERN collaboration
  - Continued support is essential to maintain US leadership.
  - These programs require significant collaboration and effort for rigorous prototype testing.
  - Without continuity in ASIC development, the US risks falling behind Europe in MAPS technology.

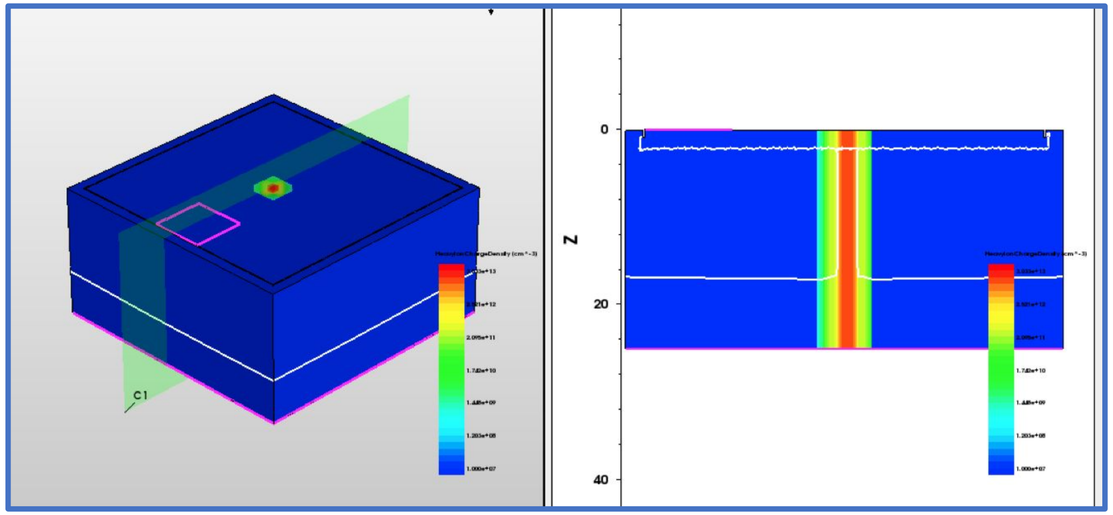
Thank you!

MAPS on novel CMOS technologies

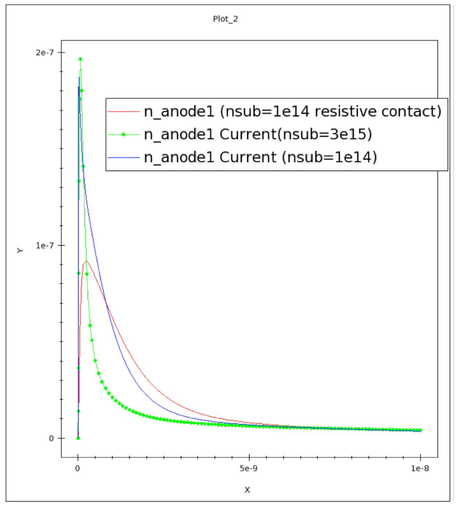
Blue-sky R&D on CMOS 22nm FDSOI

- Fully-Depleted Silicon-On-Insulator process enables implementation of sensor in substrate
- Promising CMOS process with excellent mixed-signal performance
- TCAD simulations and initial pixel design to evaluate key performance parameters:
  - Detector capacitance
  - Charge collection time
  - Cross-talk





3D Charge collection simulations (MIP)

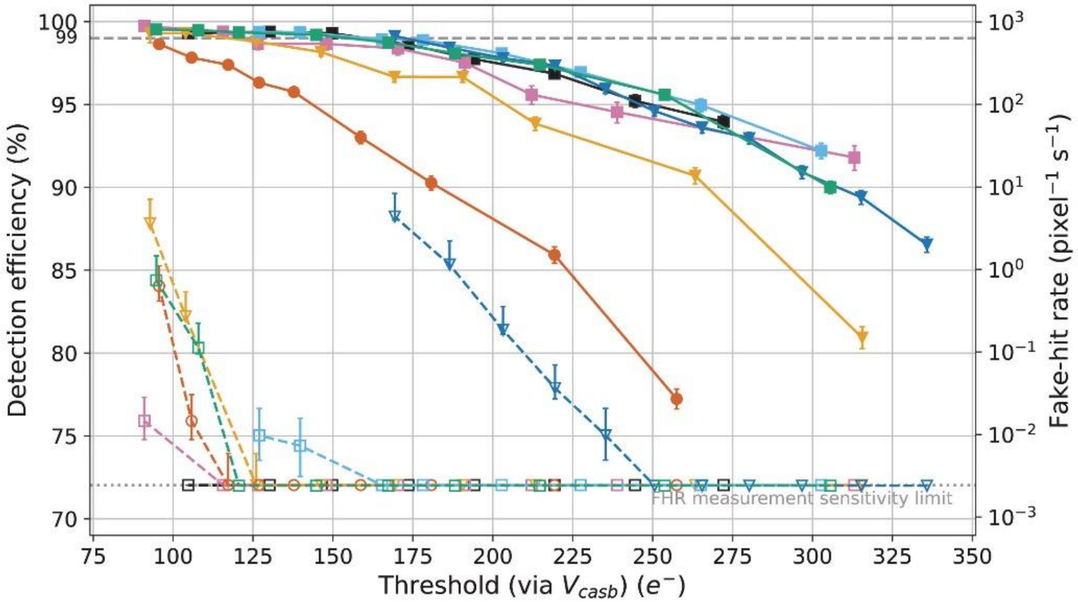


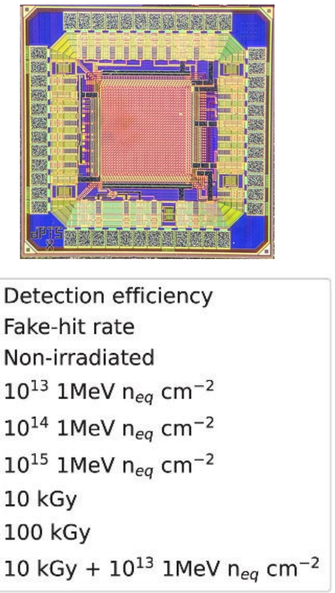
Read-out current: compare three process options

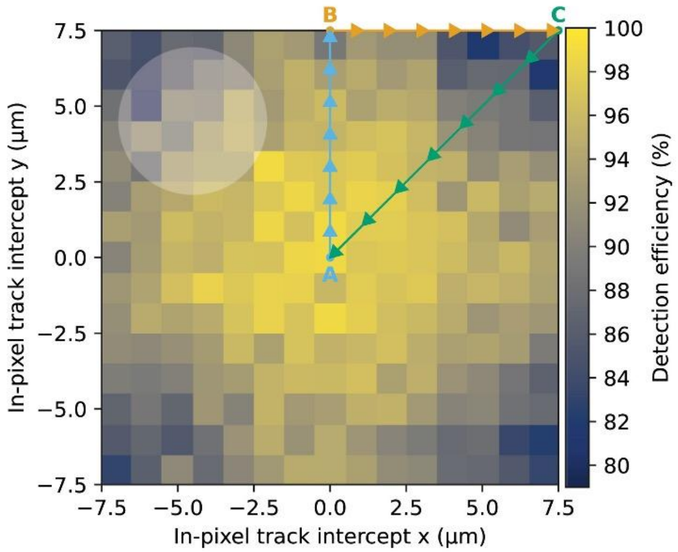
Recent results with Digital Pixel Test Structures

Synergies with DPTS characterization at CERN test beam facility within ALICE Collaboration

Characterization done up to 10^{15} 1 MeV n_{eq} cm^{-2}



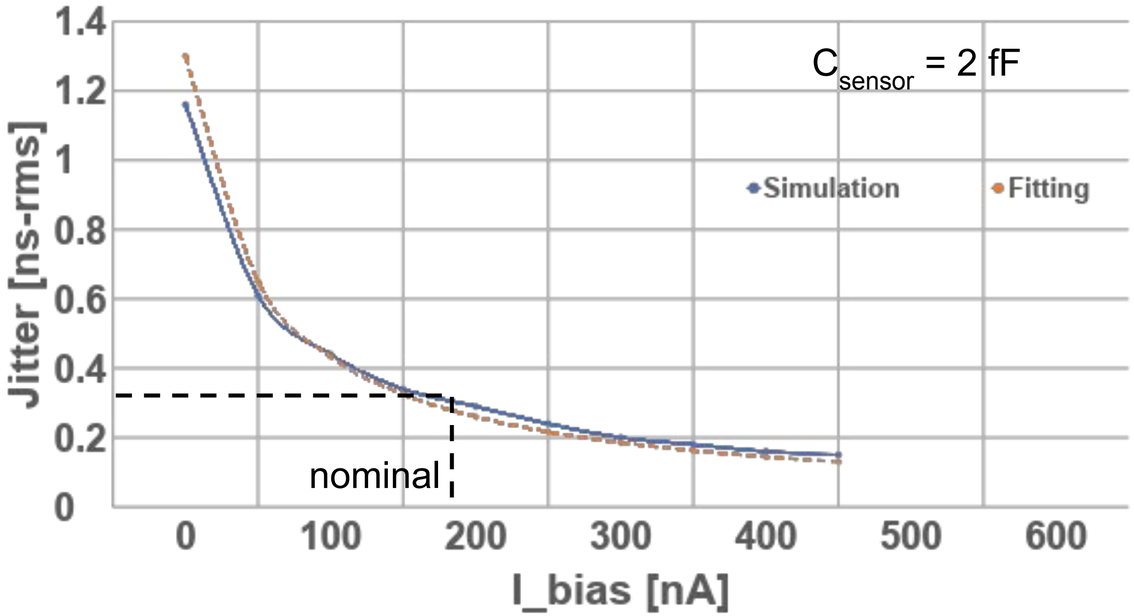




Digital pixel test structures implemented in a 65 nm CMOS process
A Compact Front-End Circuit for a Monolithic Sensor in a 65-nm CMOS Imaging Technology

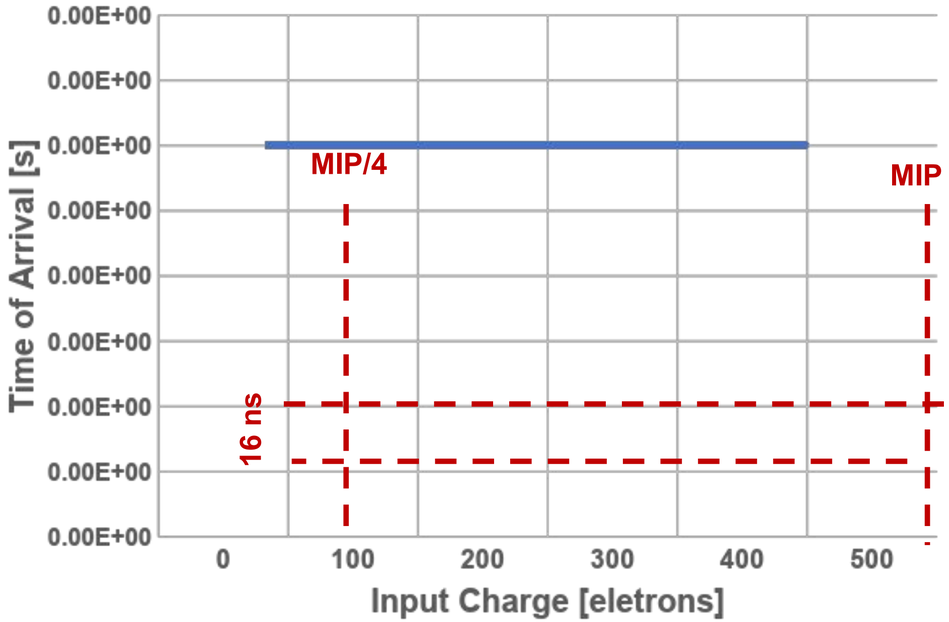
Simulation Results : Jitter and Time Walk

Jitter



I_bias = 200 nA pixel current = 600 nA
From theory we expect :

Time Walk



Time walk for MIP MIP/4 = 16 ns
Not negligible and must be corrected
(in pixel? In balcony? Offline? TBD)