HFCC AIM - MICROELECTRONICS

History, priorities and gaps

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NSF

Microelectronics in 2024

It's an exciting time for ASICs!

- Advanced AI/ML processors with integrated sensors are "everywhere."
- New packaging techniques are available, including 2.5D and 3D stacking for high performance computing.
- Heterogeneous integration with multiple die "chiplets" integrated in a single package is becoming more common.
  - And more… quantum sensors, open source/open hardware foundries, intelligent power management, neuromorphic computing…

Support from 2022 CHIPS and Science act working its way into R&D.

Image: Waymo

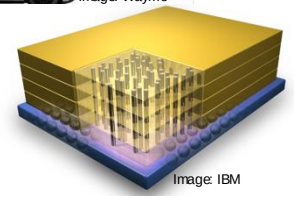


Image: IBM

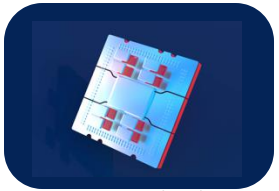


Image: MIT Tech. Review

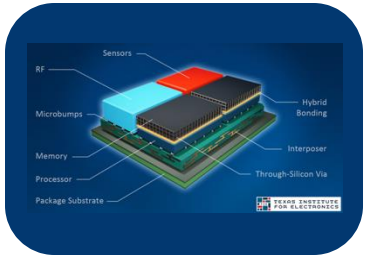
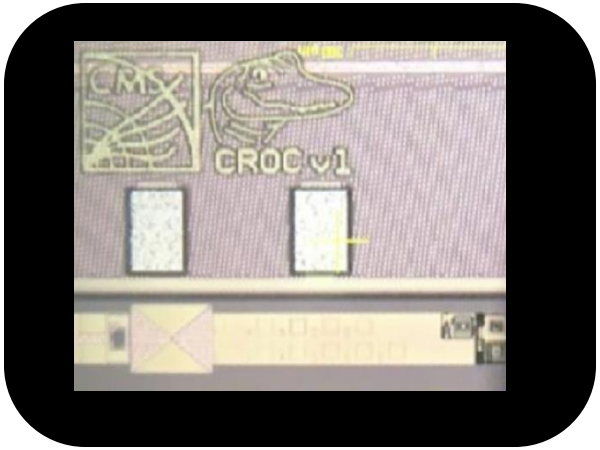


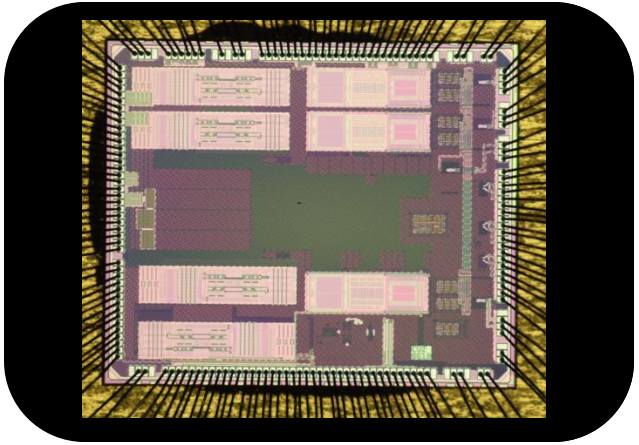
Image: Texas Institute for Electronics

US leads in ASIC development



CMS Pixel - RD53B

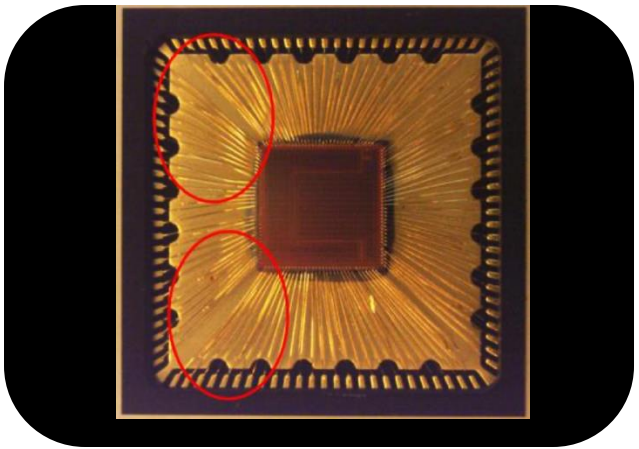
ATLAS LAr ADC



US involvement has been critical to ASIC development for HL-LHC CMS and ATLAS upgrades. *Expertise exists in our labs now… but for how much longer?*

CMS HGCAL readout

ATLAS Muon TDC



Success of the past

LHC/HL-LHC and before: readout and ASIC design for colliders focused on moving as much precision data off the detector as fast as possible (making the firehose bigger).

- Performance limited by detector/sensors and technology.
- Data provided to trigger/DAQ which accepted as much as possible.
  - Power/heat a concern.
- Reconstruction/computing/analyzers figure out how to drink from the firehose.

Image: ChatGPT

Challenges for the future

HL-LHC and beyond: we need an integrated approach. Readout and ASIC design is one part of the data analysis chain.

- We are now limited by computing power for analysis. We have to be smarter about how we take data, starting on the detector.
- Power (carbon costs), heat dissipation (esp. for ASICS in cryogenic environments) are key factors.

Image: ChatGPT

Organizing

HFCC – AIM: Microelectronics

- We are very broad. We connect to essentially all L2s. However, in general sub-detector specific ASIC developments should be developed in that L2.

The charge:

- Defining and prioritizing US community R&D efforts required during the pre-project funding phase (with an immediate need to define the program for potential near-term funding),
- coordinating US efforts with respective DRD counterparts at CERN, and
- helping to prepare required input for the upcoming European Strategy process.

Opinion: focus on common, but future Higgs factory-specific, issues:

- "New" technologies : silicon photonics, 3D hybrid integration, novel materials / devices
- Intelligence on detector : FE programmability, advanced data reduction – coordinate with AIM AI/ML
- Development of common IP

Evolving from “ASICS”

HFCC AIM: Microelectronics L3 has evolved from “Readout/ASICs” in P5 Higgs factory costing exercise. “AIM-Microelectronics” takes on the “ASICS” aspect.

- Broad interest across 4 main labs and ~10 universities
- Community surveys led to 4 main labs and 6-10 universities interested
- Broad interest from **approximately 20 scientists, 50 engineers, 20 postdocs, 10 students**

Collecting names from our EOIs, CPAD meeting, DRD groups, full-detector concept EOIs, HEPIC… **but please get in touch.**

Meeting the challenges

We've already done some homework:

Identified areas in BRN and P5 study ECFA roadmap.

Main Activity Areas	Related BRN PRDs
DRDT 1: Increased data density	
High data rate ASICs & systems	PRD17-1: low power high speed I/O
New link technologies (fibre, wireless, wireline)	PRD17-3: Power management blocks (DC/DC, regulators, pulsed power)
Power and readout efficiency	PRD17-9: multi-channel RF digitizers
DRDT 2: Intelligence on the detector (AI/ML)	
FE programmability, modularity, and configurability	FE programmability/Fast ML inference for FPGAs
Intelligent power management	
Advanced data reduction/compression	
DRDT 3: 4D- and 5D-techniques	
High performance sampling (TDCs, ADCs)	
High precision timing distribution	PRD17-8: precision clock & timing circuits
Novel on-chip architectures	
DRDT 4: Extreme environments and required longevity	
Radiation hardness	PRD16-1: Extreme radiation & rate
Cryogenic temperatures	PRD16-2,3: Cryogenics (intermediate, deep/quantum)
Reliability, fault tolerance, detectro control	PRD17-7: fault tolerant communications
Cooling	
DRDT 5: Emerging technologies and data processing	
Novel microelectronics technologies, devices, materials	PRD16-4: Automated design & verification (int. CMOS with photonics nodes, IoT/self-assembly or assembly-free)
Silicon photonics	PRD17-2: wireless control/monitoring blocks
3D integration and HD interconnects	3D integration & high-density interconnects
Keeping pace with, adapting, and interfacing to COTS	
Open-source fabrication harmonization & development	
DRDT 6 (new): Monolithic sensor ASICs	PRD17-4: Monolithic designs with integrated sensor & readout
DRDT 7 (new): Technologies & tools	

Schedule and priorities

Possible schedule for potential US contributions

FY24	FY25	FY26	FY27	FY28	FY29	FY30	FY31	FY32	FY33
Pre-approval of the collider stage				*Post-Approval/Pre-CD-0*			*Post CD-0 Stage*		

- Need to discuss priorities,
- while considering ramp-up and possible funding envelope.

Initial prioritization

R&D Topic	Priority
AI/ML in ASICs	1
Monolithic sensor ASICs	1
High performance ASICs for 4D/5D detectors	1
IP blocks for 28 nm technology	1
3D / hybrid integration	1
Silicon photonics	1
Increased data density	2
Emerging tech including open source design/fab, wireless ctrl/monitoring, automated design/verification	2
Extreme environments & longevity, such as reliability & fault tolerance, radiation hardness, or cryogenic temperatures	3

Focusing the effort

Scope (for discussion) : build common ASIC technology and explore new technologies useful for adoption in the development of electronics for HF detectors. We need to organize this into WPs.

Research Area	Ongoing and future effort
AI/ML in ASICs, intelligence on detector	UT Austin, U Chicago, Cornell, UIC, UIUC, JHU, Kansas, ANL, LBNL, BNL, FNAL, SLAC, ORNL
Common IP for future MOSFET process nodes (28 nm e.g.)	LBNL, BNL, FNAL
3D / hybrid integration	USSC, LBNL, BNL, FNAL
Silicon photonics	ANL, LBNL, FNAL
High data density (including fast optical links	UPenn, ANL, LBNL, FNAL
Novel materials / devices	LBNL, FNAL
Novel design tools : open source, automated, AI/ML enhanced	UPenn, LBNL, BNL, FNAL, HEPIC
MAPS, 4D/5D sensor + ASICs, electronics for precision timing (now covered in Tracker L2 area)	U Michigan, ND, Oregon, UCSC, ANL, LBNL, BNL, FNAL, SLAC, ORNL

Not included:

- MAPS (belongs in Tracking/Calo)
- Detector specific analog very-front-end will be covered separately by each sub-detector
- Fast timing for signals (belongs in Tracking/LGAD)
- Off-detector electronics (belongs in TDAQ)

Time for discussion

AIM-Microelectronics is a critical need for HFCC and well aligned with national interests. Support is urgent. ASICs for HL-LHC are nearly finished and unique expertise could be lost.

- **First step – your input for ESG:**
  - What do you want to deliver from your L3 area to a Higgs Factory detector?
  - Need to highlight unique capabilities and leadership of US.
  - What do we want to contribute in the near-term and longer term?
  - What funding do we need?
  - What input do we need?
  - Connections to other areas?

There is a long road ahead!

Add to notes here: https://docs.google.com/document/d/17ILe_gQKisxntrQcU3ZOP_VEz-7XBd7__B6liE4zVt0/edit?tab=t.0