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Si-tungsten (SiW) Calorimetry for the Higgs Factory

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SiW Calorimetry for the Higgs Factory

- There have been many applications of silicon-tungsten calorimetry
  - Luminosity monitors (SLD, Opal, Aleph)
  - Pre-shower detector (ZEUS, FASER)
  - Test-beam prototypes (SiD, CALICE, EPICAL)
  - Forward calorimeter at LHC (CMS HGCAL, ALICE FOCAL)
- ECal requirements for particle flow motivate SiW ECal for Higgs Factory
  - Isolate showers and nearby particles in a jet
  - Measure energies of each shower in jet
  - Measure energy and position of isolated gamma showers
  - Power management is critical

SiW Calorimetry for the Higgs Factory

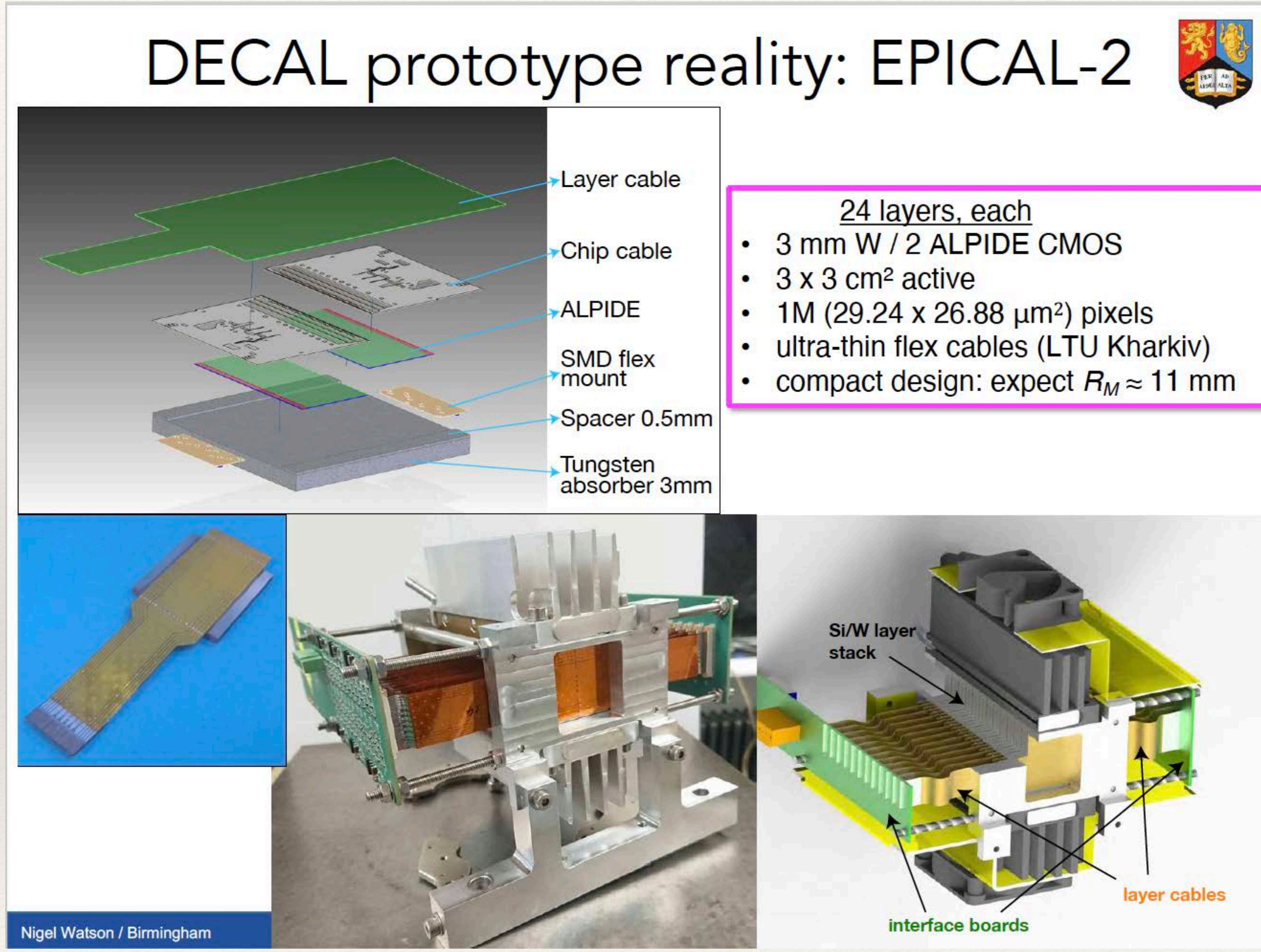
- There were three group responses to our call for input from colleagues interested in participating in the HFCC Si-W ECal activity
  - Graham Wilson (Luminosity monitor and forward calorimetry)
    - Graham will discuss his interests
  - CMS HGCAL group
    - Lindsey Gray, Murtaza Safdari, Zoltan Gecse
    - "Interested in exploring the simulation and electronics design of a pixellated Si-W electromagnetic sampling calorimeter employing MAPS sensor technology as the sensing mechanism. Pending funding, we will develop further simulations of a full detector, and use those simulations to understand data rate considerations and readout implementations possible using real-time machine learning, working towards fabrication. Furthermore, we will work with the other calorimetry efforts at FNAL towards a proposed calorimetry testbeam area. We will seek to gain practical experience by working with collaborations that have already developed small-scale MAPS-calorimeter prototypes already developed."
  - SLAC/Oregon
    - Caterina Vernieri, Lorenzo Rota, Martin Breidenbach, Jim Brau, David Strom

Digital ECal with Monolithic Active Pixel Sensors

- MAPS development driven by needs of tracking system

- Applied to ECal offers improved capability over larger, analog pixels
    - counting mips improves energy resolution
        - for example, 5000 um^2 pixel enables this
            - approximate separation of mips near shower max
    - containment of shower enables individual particle separation in jets
        - smaller than Moliere radius beneficial (not just Moliere radius)
    - shower position measurement contributes to jet reconstruction
    - timing of sub-nanosecond required to separate accelerator bunches.

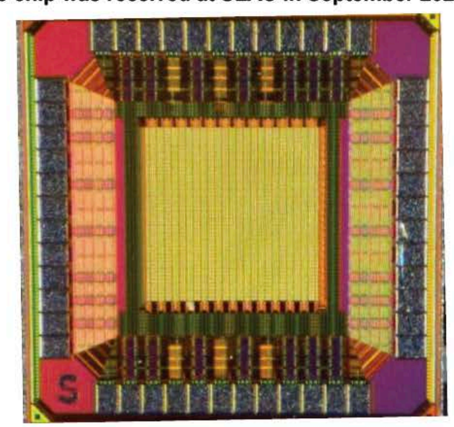
Digital MAPS ECal R&D



❖ SiD MAPS Project

	Specification	Simulated NAPA-p1
Time resolution	1 ns-rms	0.4 ns-rms ✓
Spatial Resolution	7 µm	7 um ✓
Noise	< 30 e-rms	13 e-rms ✓
Minimum Threshold	200 e-	~ 80 e- ✓
Average Power density	< 20 mW/cm²	0.1 mW/cm² for 1% duty cucle ✓

The chip was received at SLAC in September 2023

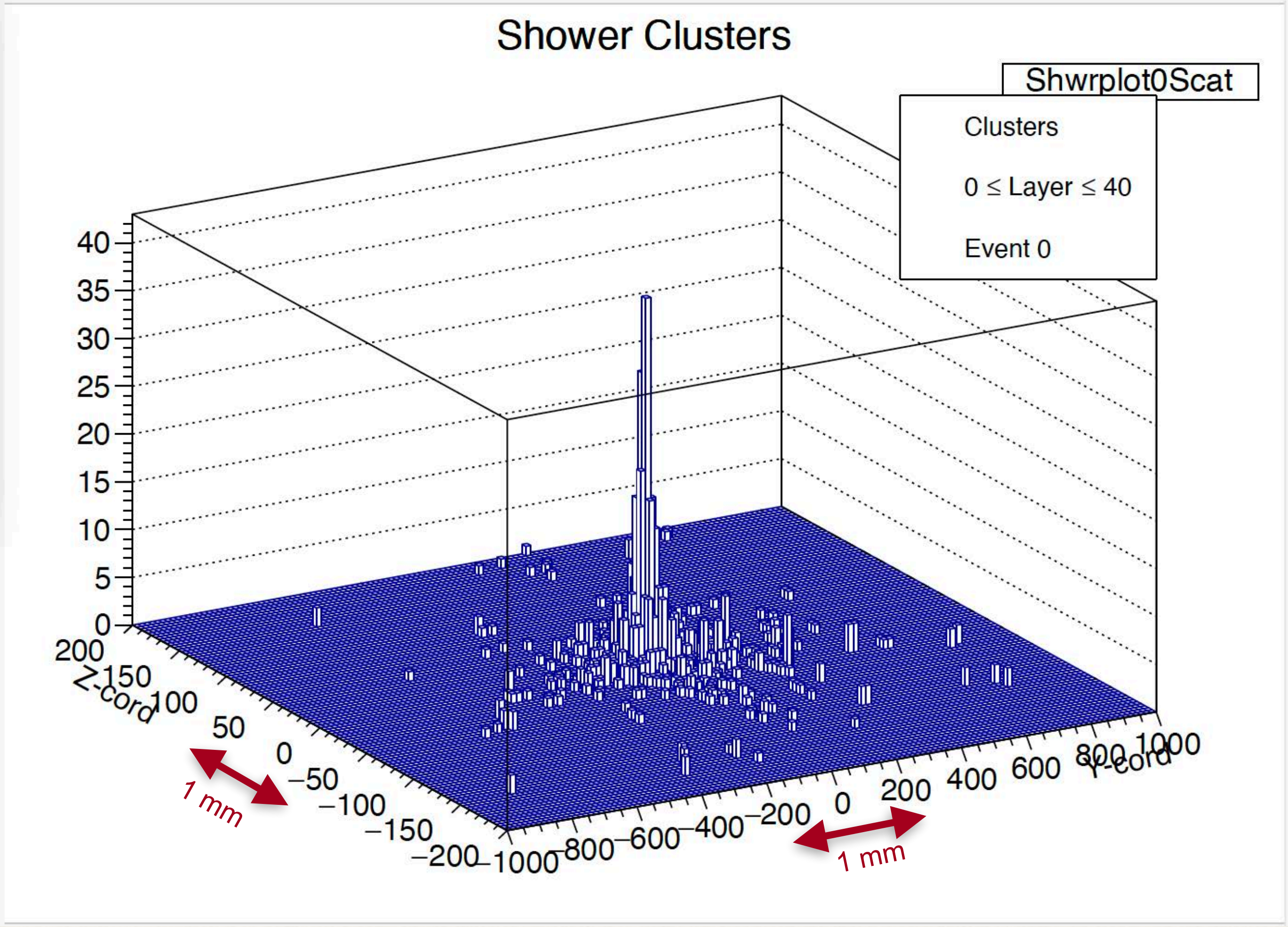


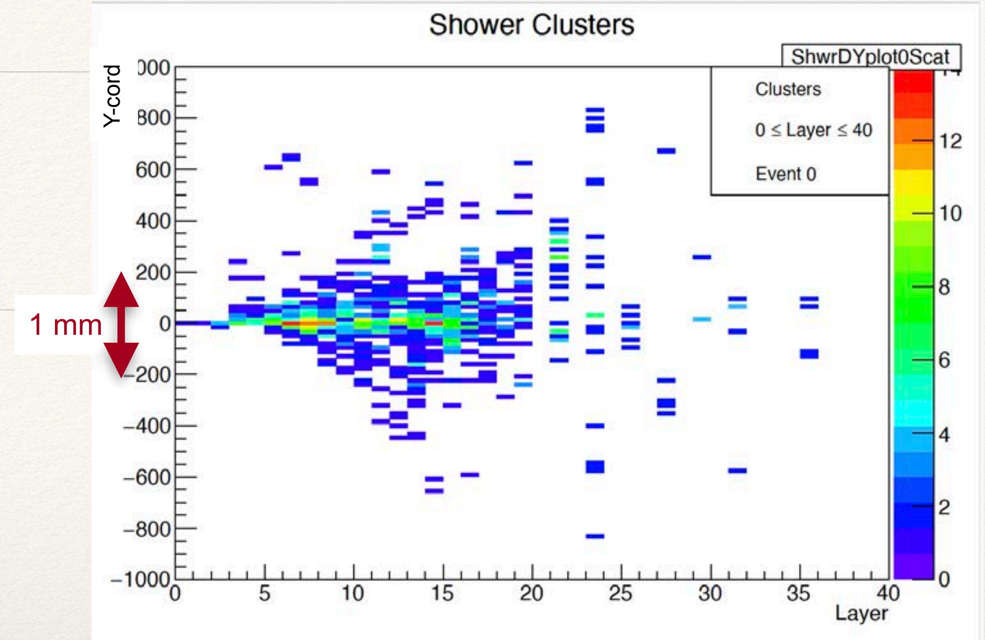
Microscope photo of NAPA-p1

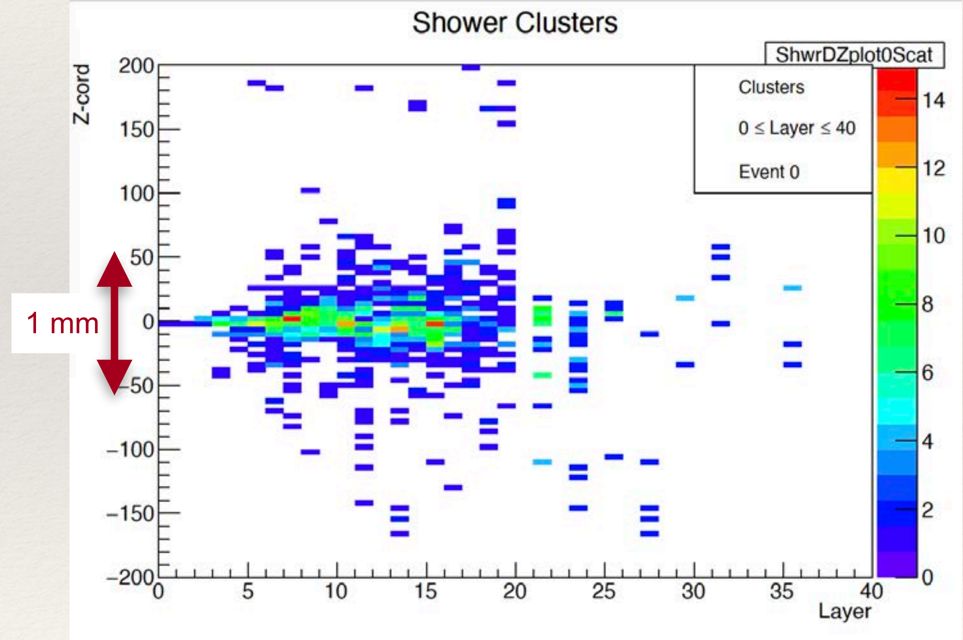
Acknowledgement: CERN WP 1.2 for the excellent cooperation: NAPA-p1 uses the pixel masked developed and optimized by CERN, and was fabricated in a shared run led by CERN

❖ includes ALICE FoCAL collaborators

10 GeV Shower in 25 x 100 μm²







Digital MAPS ECal R&D

- EPICAL - full calorimeter tested by European group

24 layers, each
- 3 mm W / 2 ALPIDE CMOS
- 3 x 3 cm² active
- 1M (29.24 x 26.88 μm²) pixels
- ultra-thin flex cables (LTU Kharkiv)
- compact design: expect $R_M \approx 11$ mm

- SiD - developing sensor optimized for Higgs Factory

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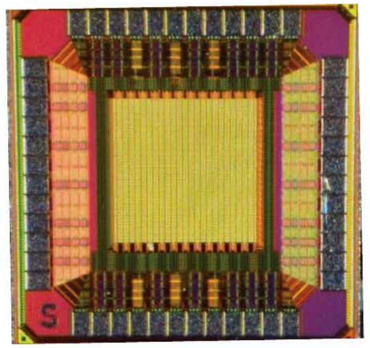


Microscope photo of NAPA-p1

Working with CERN WP 1.2 ; Sensor fabricated in a shared run led by CERN.

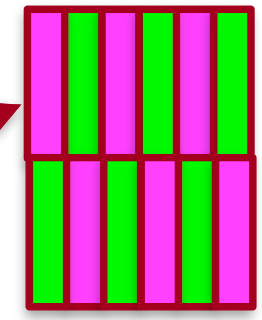
Two groups engaged in active discussions - EPICAL includes FoCAL collaborators

Main specifications for Large Area MAPS development

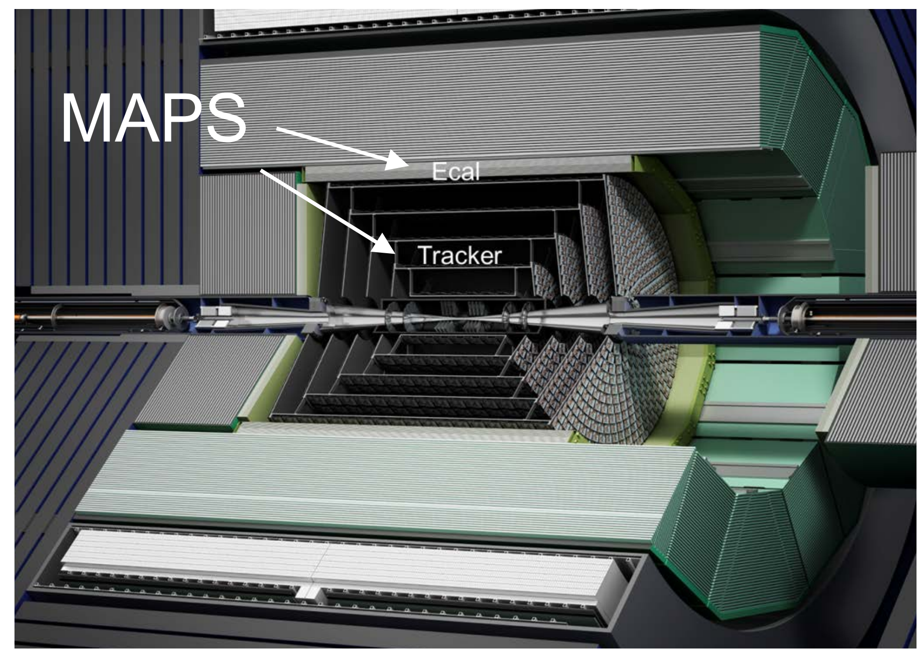
TID-AIR SLAC

L. Rota

Parameter	Value	Notes
Min Threshold	140 e^-	0.25*MIP with 10 μm thick epi layer
Spatial resolution	7 μm	In bend plane, based on SiD tracker specs
Pixel size	25 x 100 μm^2	Optimized for tracking (or 25x50/25 μm^2)
Chip size	5 x 20 cm^2	Requires stitching on 4 sides
Chip thickness	300 μm	<200 μm for tracker. Could be 300 μm for EMCal to improve yield.
Timing resolution (pixel)	~ ns	Bunch spacing: C^3 strictest with 5.3->3.5 ns; ILC is 554 ns
Total Ionizing Dose	100 kRads	Total lifetime dose, not a concern
Hit density / train	1000 hits / cm^2	
Hits spatial distribution	Clusters	Due to jets
Balcony size	1 mm	Only on one side, where wire-bonding pads will be located.
Power density	20 mW / cm^2	Based on SiD tracker power consumption: 400W over 67m^2



25 x 100 μm^2 ECal performance same as 50 x 50 μm^2



SiD Tracker and the ECal

<1 mW/cm^2 for 1% duty cycle

Proposed US Effort on MAPS for ECal

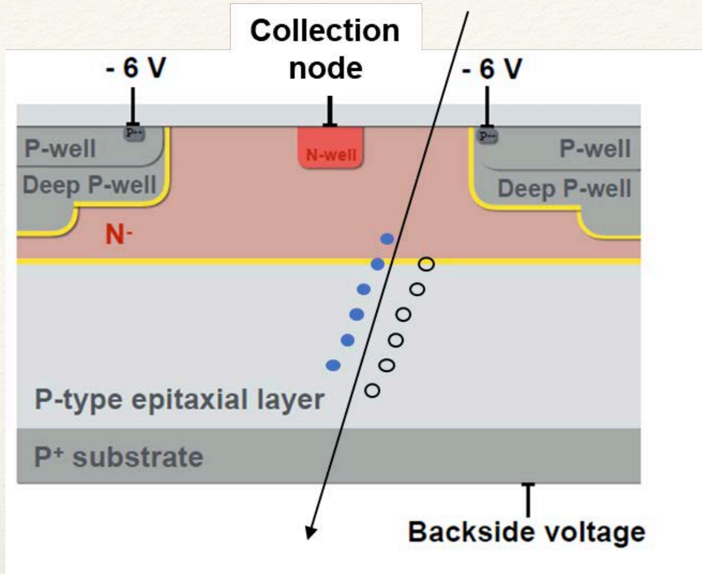
arXiv:2306.13567

US MAPS ECal development will proceed in parallel with US Tracking Sensor Development Efforts (CPAD RDC3) and ECFA DRD3 to enable large scale production at competitive cost.

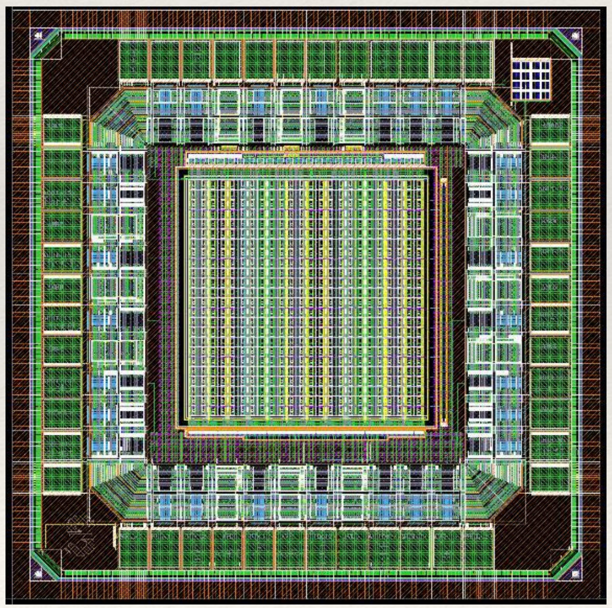
- **FY23-24:** Develop power and signal distribution schemes compatible for cal and tracking, in addition to evaluating first pixel results.
- **FY25:** Design PCBs with variations for the services balcony at the edge of sensors. Submission for sensors for large prototype active layers. Understand options for alternative foundries.
- **FY26:** Prototype attachment of sensors to PCB, probably with a conveyor oven so large production is feasible.
- **FY27:** Build prototype multilayer section with edge cooling and prepare/begin beam test.
- **FY28:** Complete beam tests with technical verification.
- **FY29-32:** Design, construct and test MAPS ECal modules based on final design of sensors and sampling layer configuration.
    - Physics and detector simulation throughout this effort to back up project.

US MAPS ECal Institutes: SLAC, University of Oregon

Large Area MAPS - Highlights and Next Steps



Current sensor optimization in TJ180/TJ65 nm process
Effort to identify US foundry on going



Layout of SLAC prototype for WP1.2 2022 shared submission on TowerSemi 65nm

Approach:

- Focus on long-term R&D, targeting simultaneously:
  - ~ns timing resolution
  - Power consumption compatible with large area and low material budget
  - Fault-tolerant circuit strategies for wafer-scale MAPS

Highlights:

- 1st SLAC prototype on TJ65nm (2023) from CERN WP1.2 shared run
- Performance of 1st SLAC prototype on TJ65nm (2023) evaluated

Next steps:

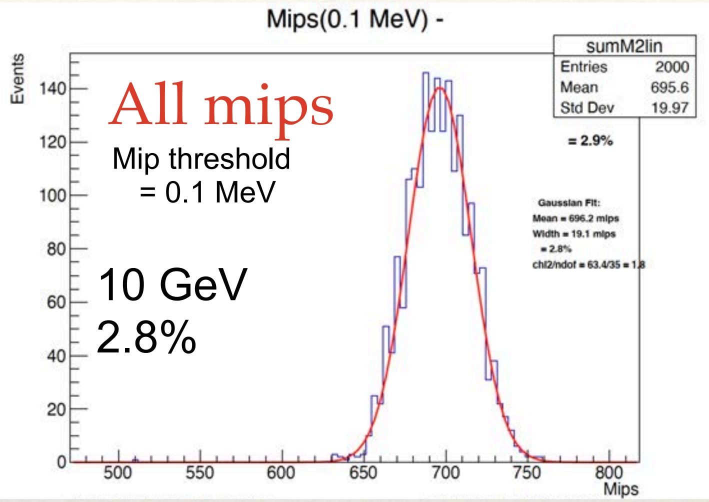
- New design combining O(ns) timing precision and low-power (2024/2025).
- **Stretch Goals:** design of a wafer-scale ASIC (2025/2026, design only)

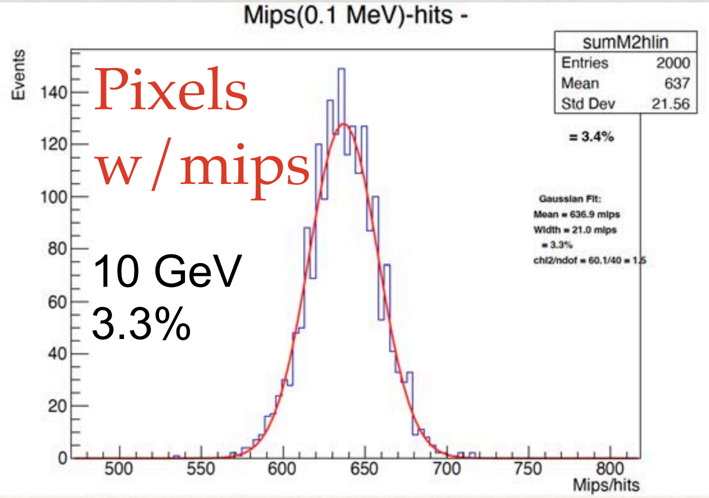
Engagement :

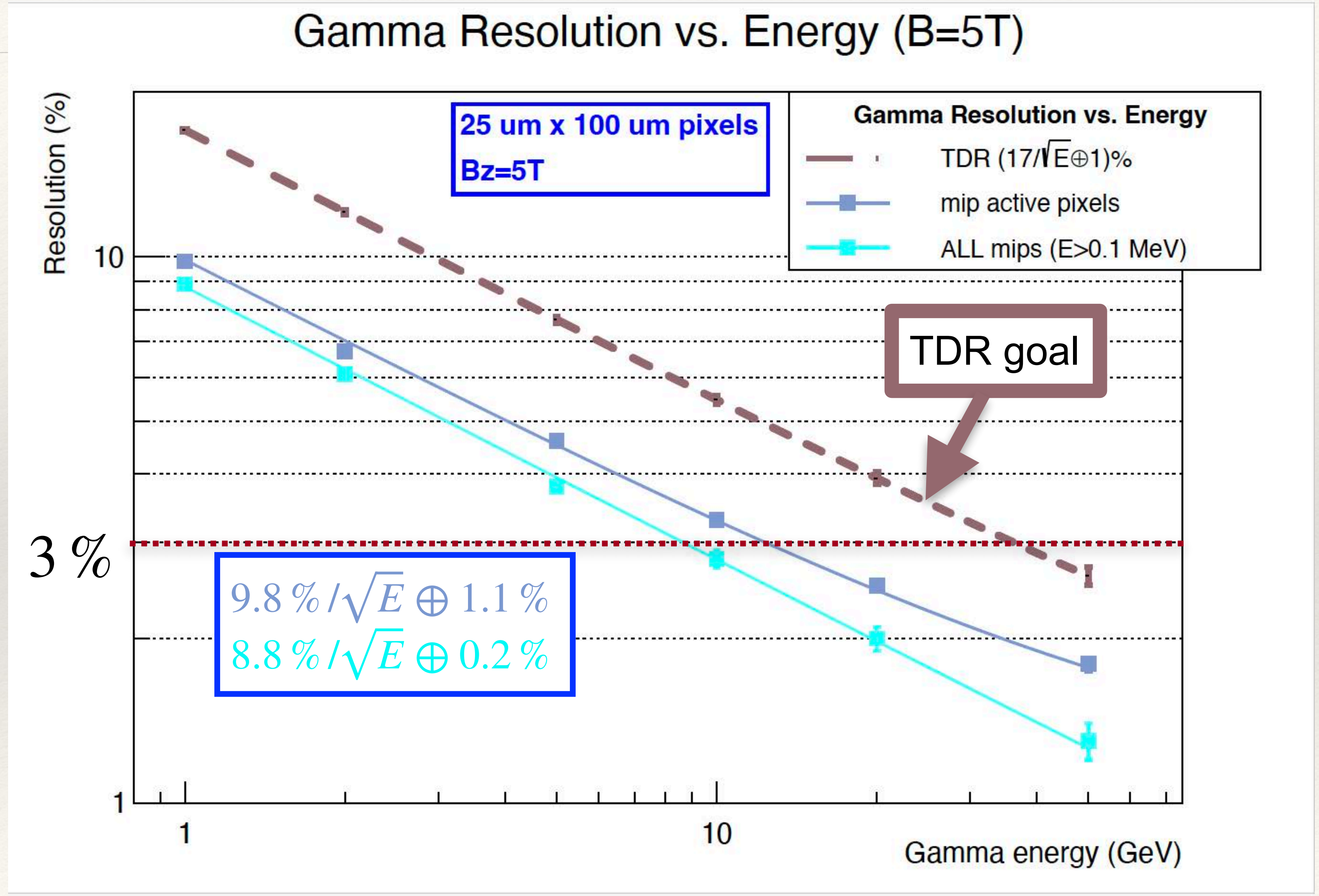
- Higgs Factory detector initiative R&D
- DRD 3 silicon sensors
- DRD 7.6 on common issues of power distributions compatible with stitching

A. Habib *et al* 2024 *JINST* **19** C04033
C. Vernieri, MAPS DRD 3.1 talk

Ultimate Resolution (mips)

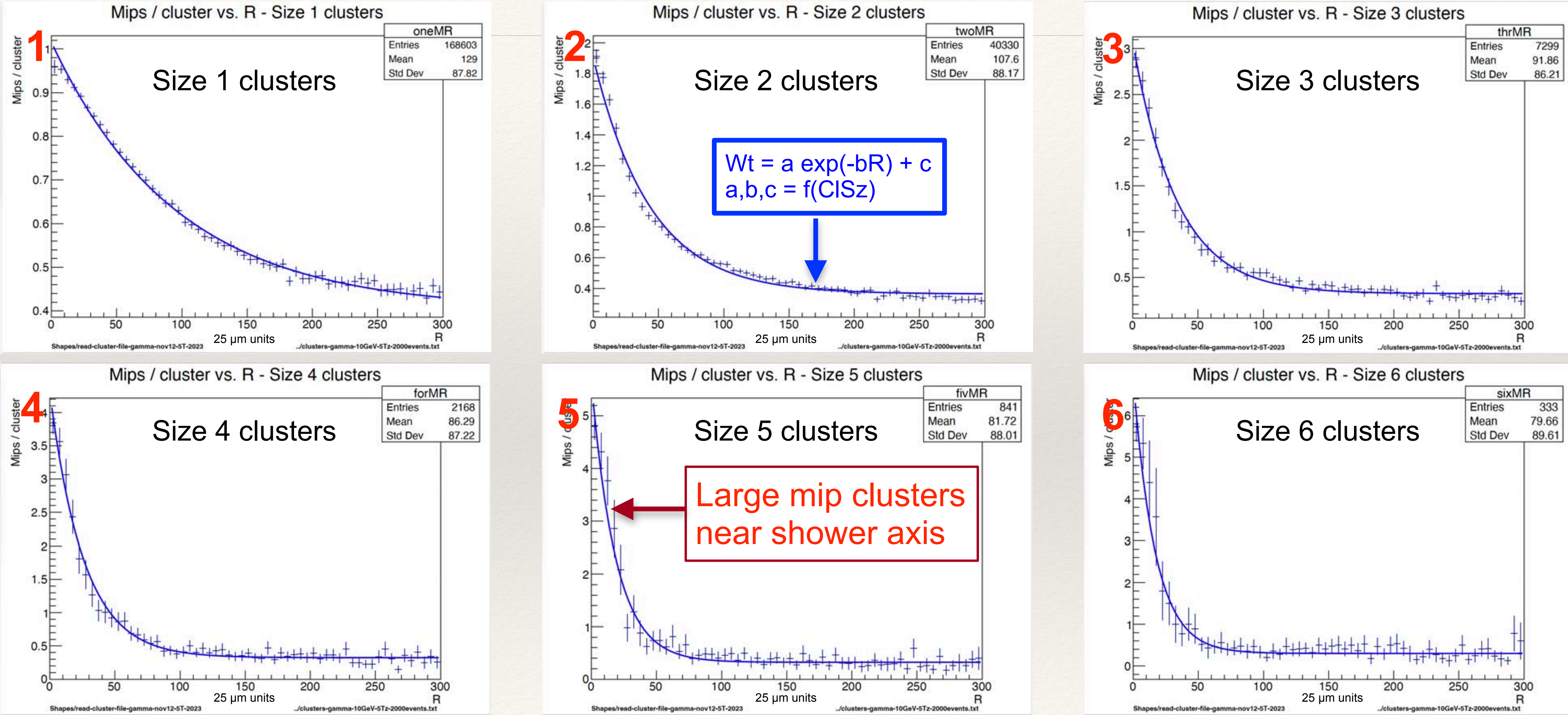






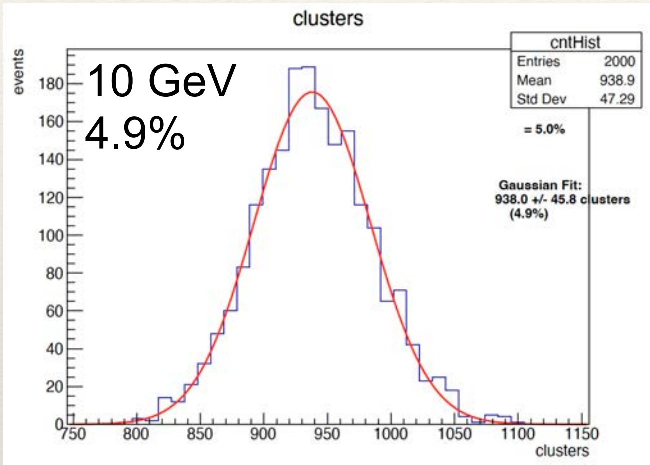
mip counted once in a layer,
when it enters sensor.

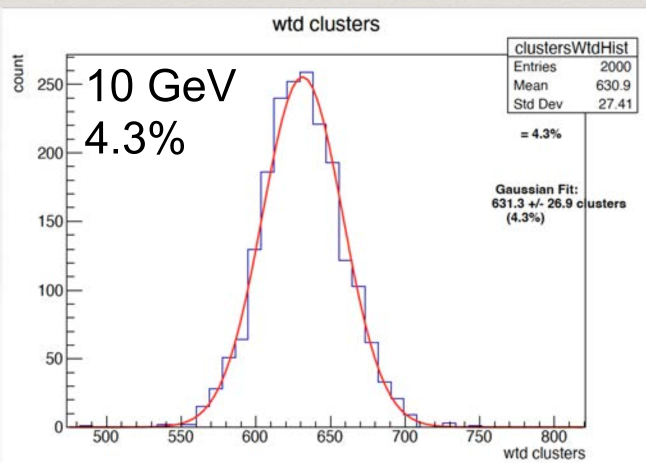
Mips/cluster vs. showerR   10 GeV γs - 2000 showers

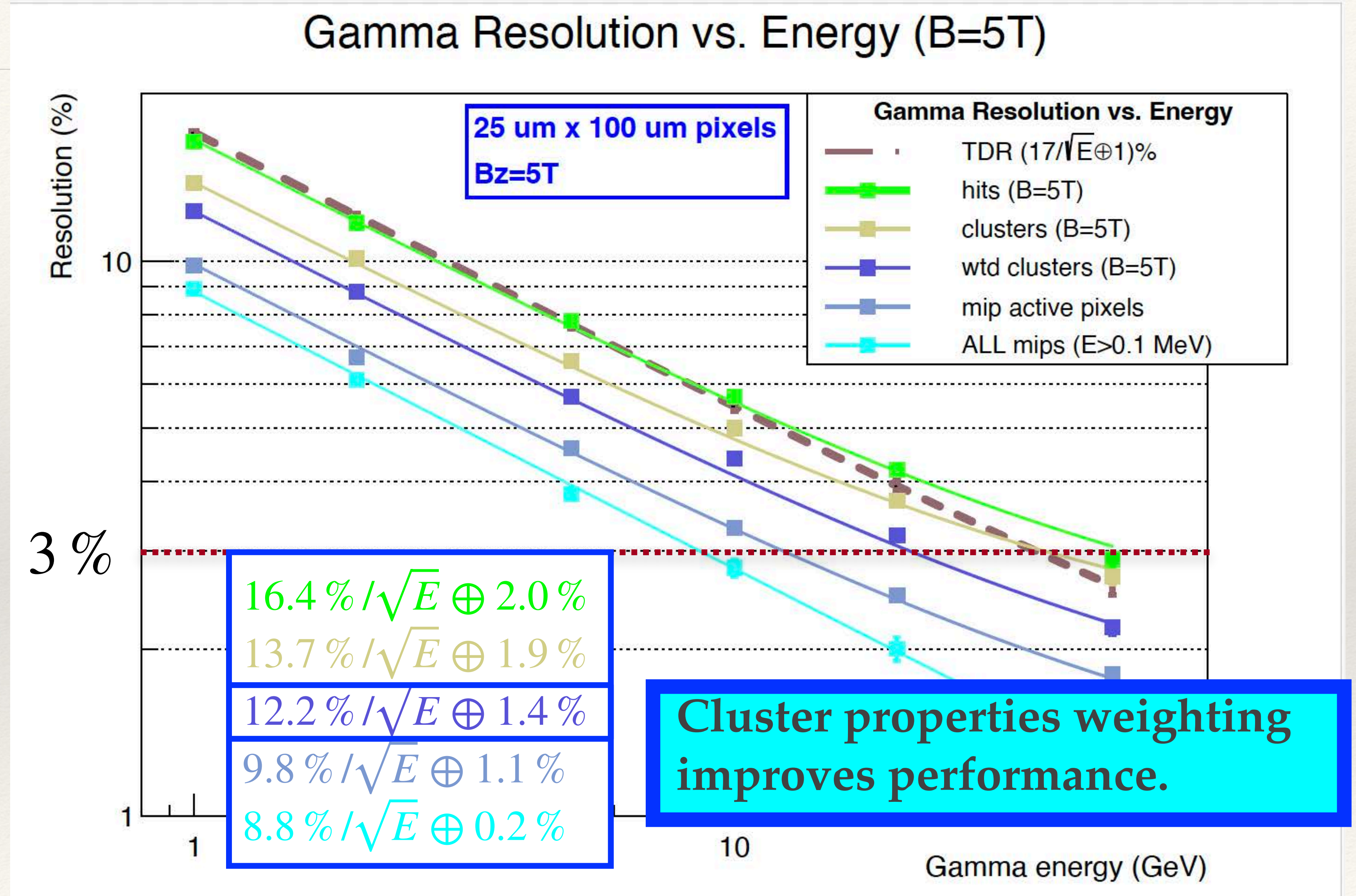


Resolution vs. Energy (hits/clusters/mips)

Resolution vs. Energy (hits/clusters/mips)
& weighted clusters.

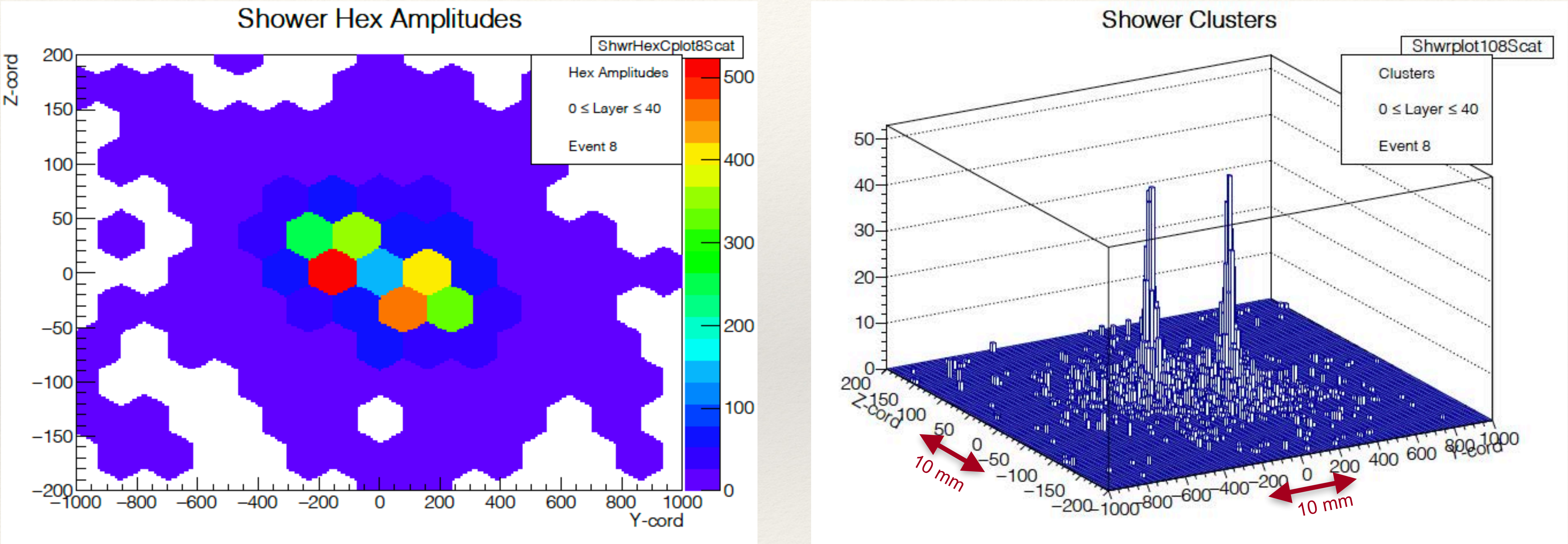






Multi-shower of SiD MAPS compared to SiD TDR

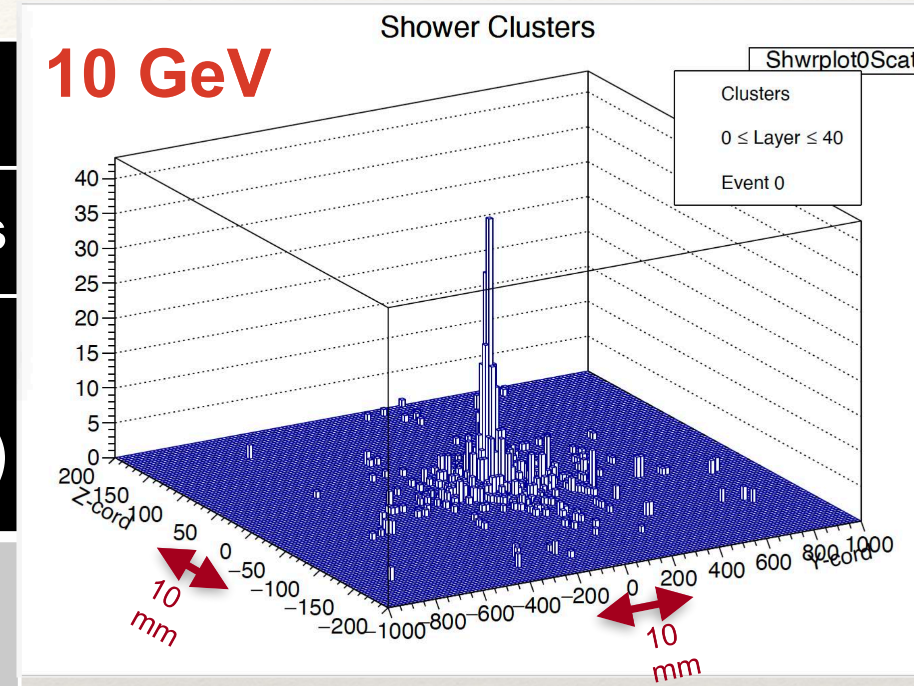
40 GeV $\pi^0 \rightarrow$ two 20 GeV γ's



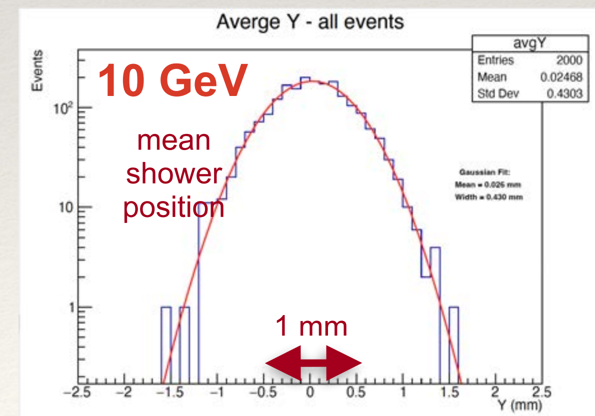
Illustrates PFA Potential

Improved shower transverse position measurement

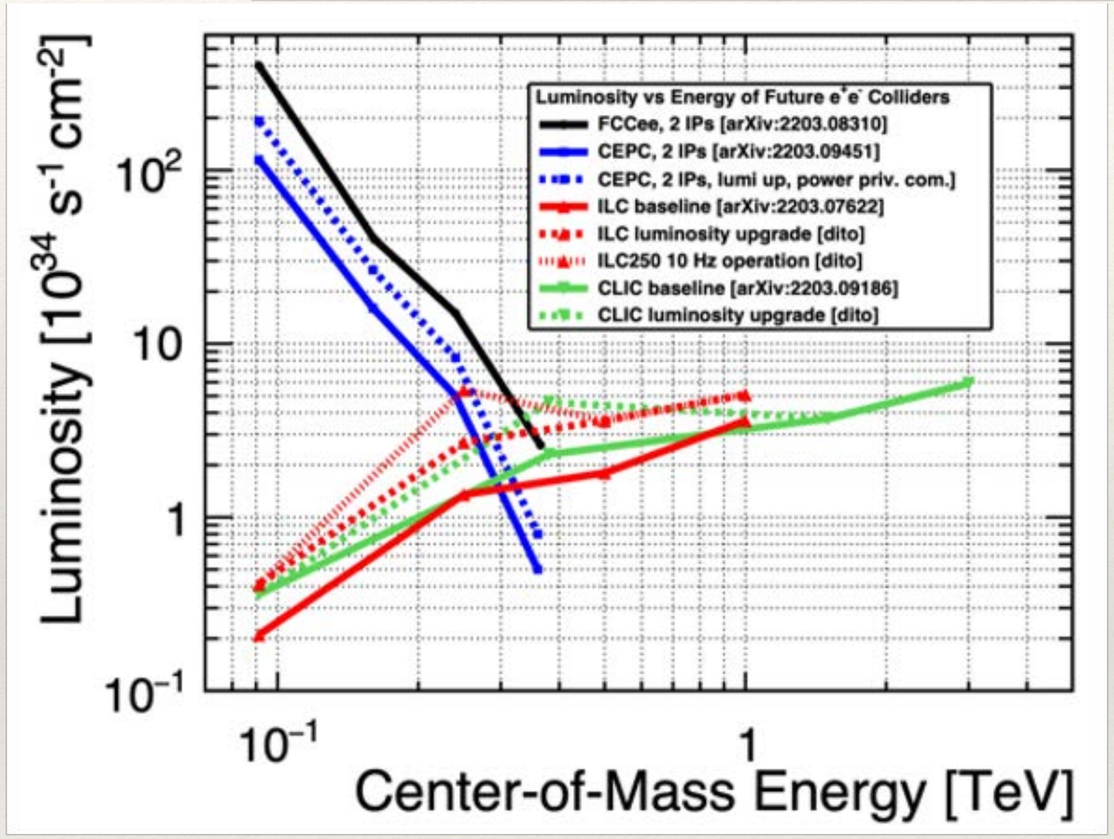
	Shower spread		Shower position measurement					
			all clusters		within 4 mm		1st 20 Layers	
Eγ (GeV)	Y (mm-rms)	Z (mm-rms)	δY (mm)	δZ (mm)	δY (mm)	δZ (mm)	δY (mm)	δZ (mm)
1	4.7	4.2	1.17	1.04	0.77	0.64	0.68	0.55
10	4.8	4.3	0.43	0.37	0.22	0.18	0.17	0.15
50	5.1	4.6	0.21	0.20	0.12	0.11	0.11	0.10

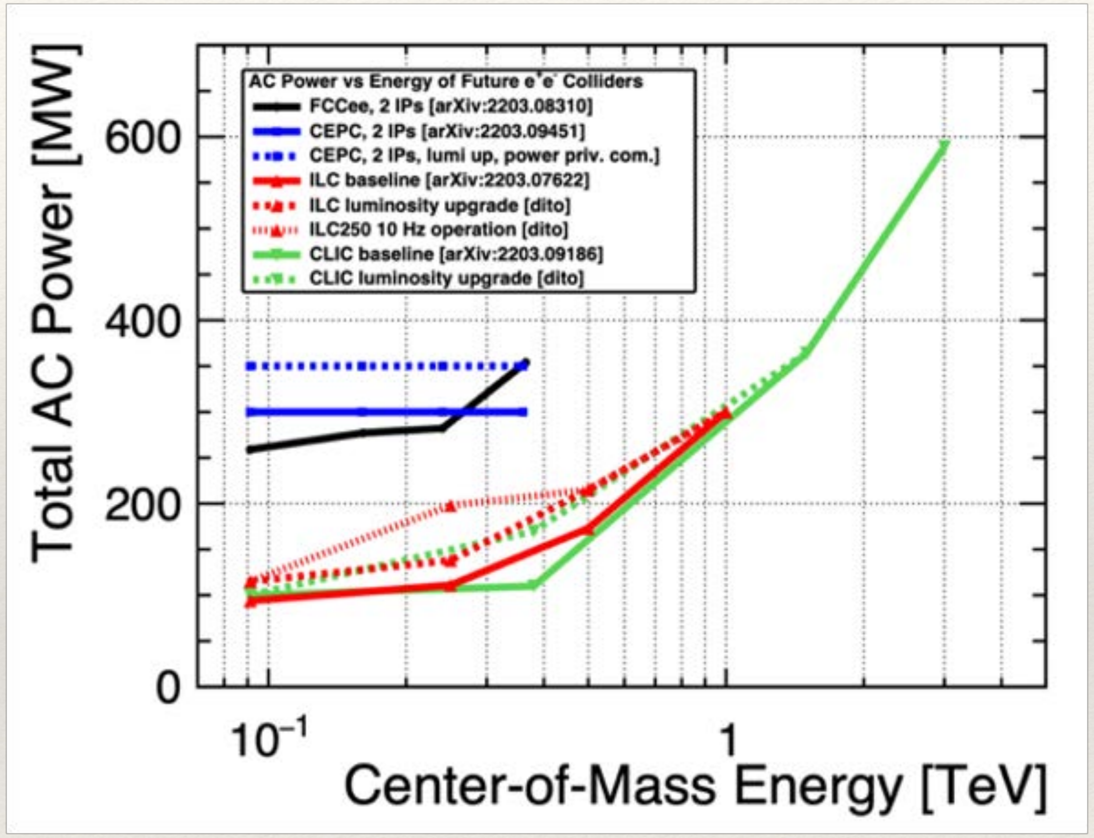


Bz=5 T



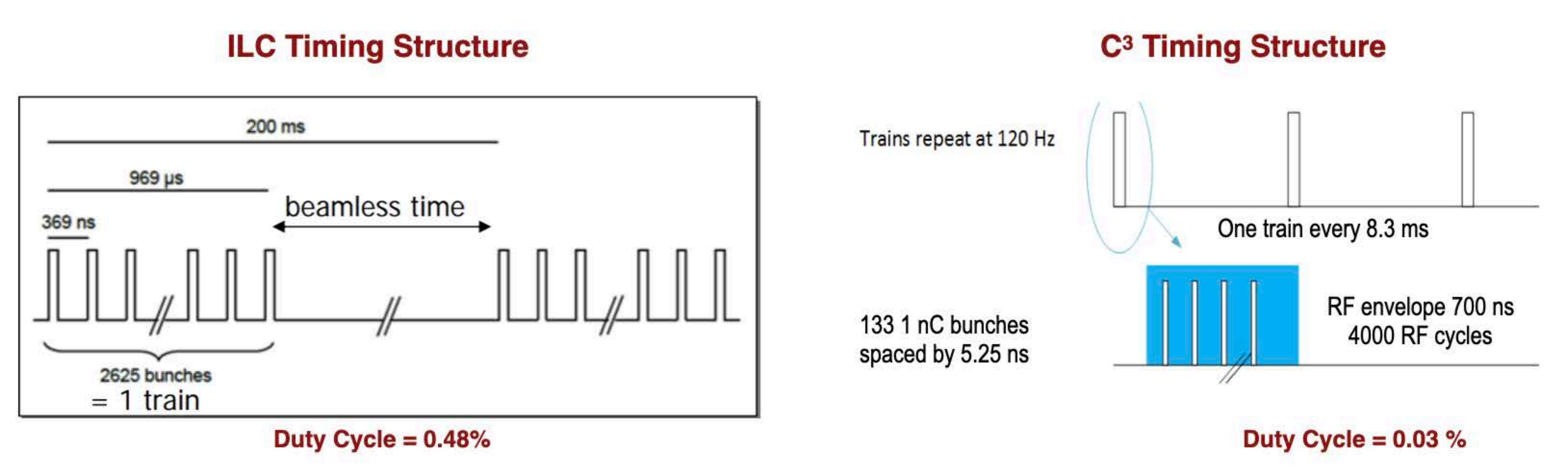
Different challenges for Linear & Circular Colliders





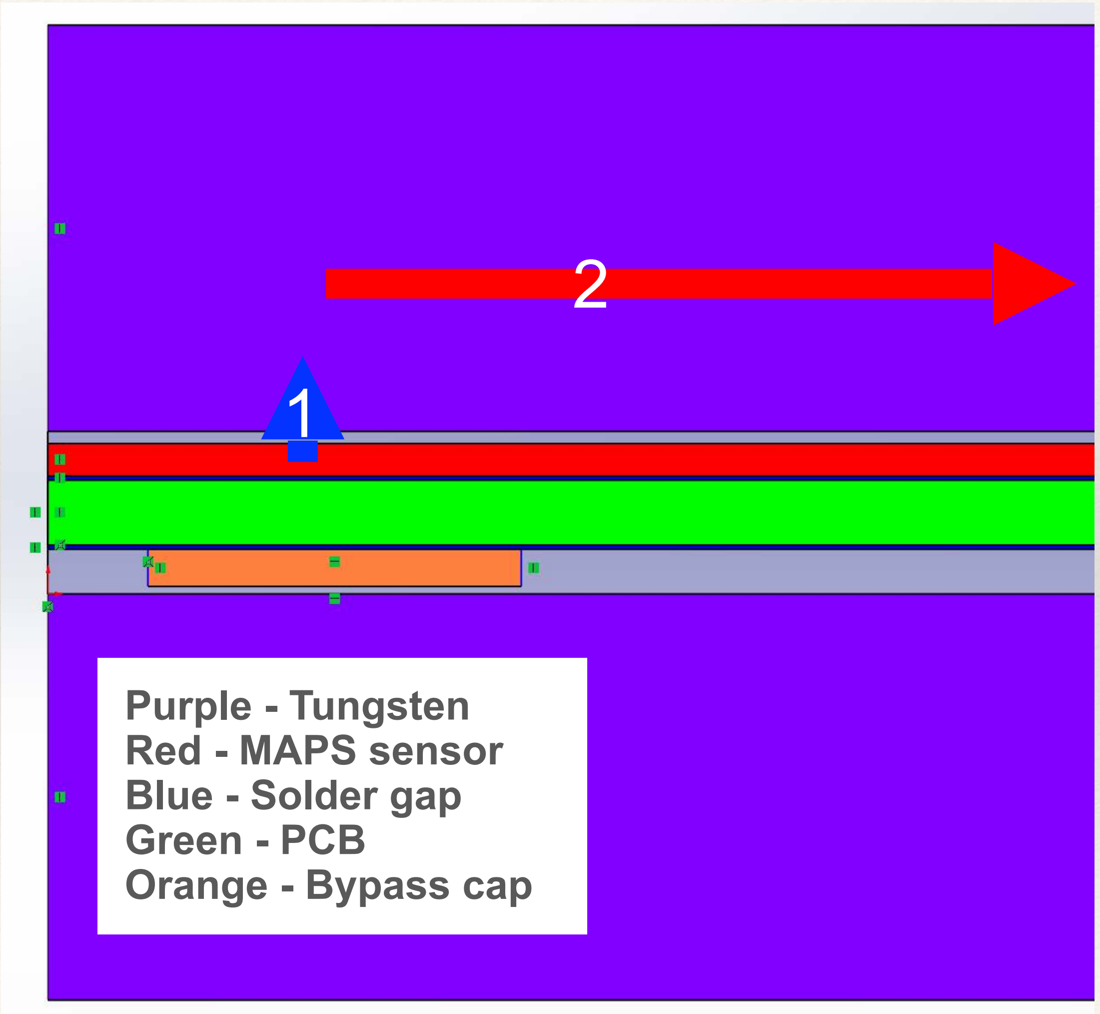
- Important, driving motivation for linear colliders is high energy reach.

Different challenges for Linear & Circular Colliders



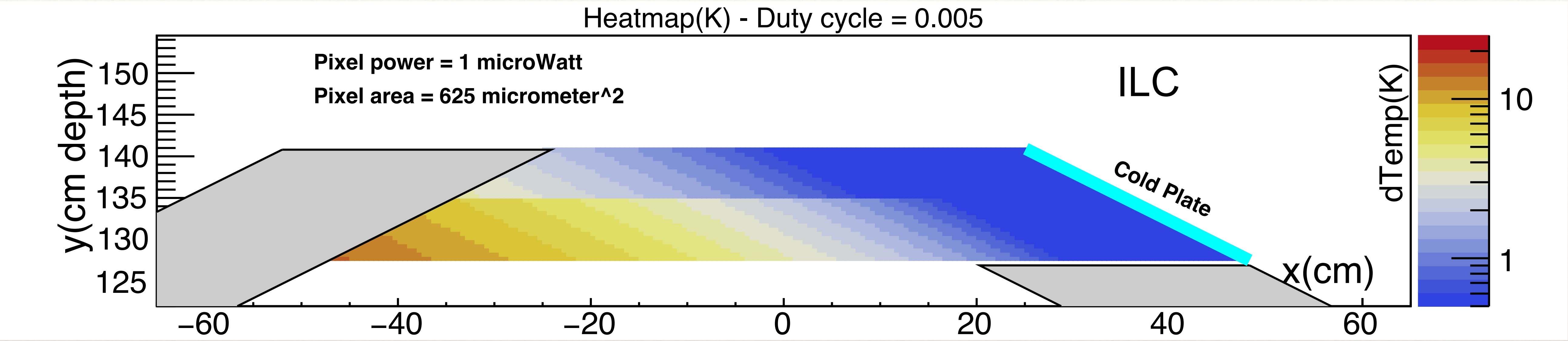
- Linear Colliders use bunch trains, with significant time between trains
  - compare to FCC bunch spacing at 250 GeV ~ µsec
- This enables LC power pulsing, reducing heat load by two orders of magnitude, or more

Heat conduction from ECal sensor to cold plate



- MAPS generates ~kW/m² when powered
  - each sensor is 100 cm²
  - power pulsing can reduce heat load
- First heat flows through 300 μm N_2 to tungsten
  - $\Delta T \ll 1$ K
- Then heat flows thru tungsten to cold plate
  - Tungsten absorber lengths 0.5-1.0 m
  - Temperature rise is length dependent

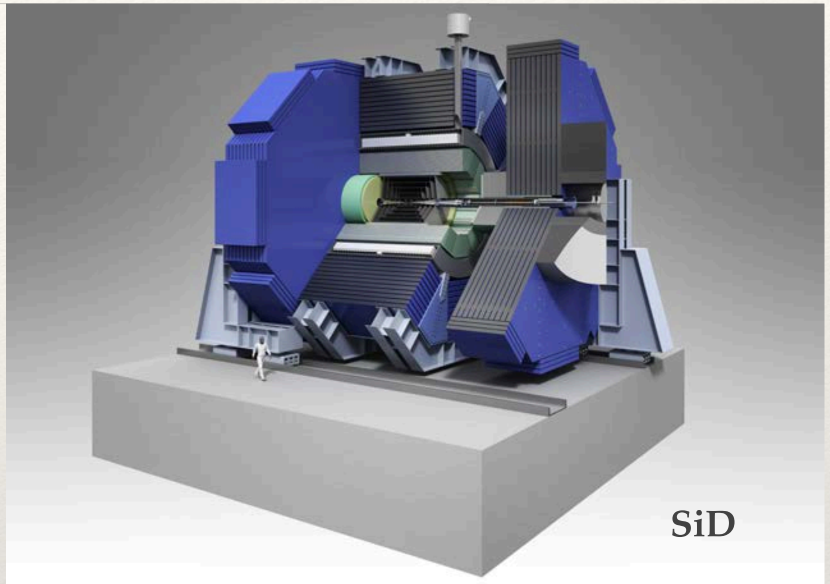
Heat conduction from ECal sensor to cold plate



- Duty cycle - 0.07% (C3/CLIC) - ΔT ~ 0.5 - 2 K
- Duty cycle - 0.5% (ILC) - ΔT ~ 4 - 16 K
  - Without power pulsing temperature blows up and needs active cooling
    - design for FCC/CEPC (bunch spacing ~μsec)?
    - learn from CMS HGCAL

Digital ECal Based on MAPS

- Higgs Factory digital MAPS ECal offers excellent performance.
  - Well defined EM shower structure allows simple algorithmic optimization of energy measurement.
  - Neural net studies may improve over "informed" algorithm.
  - Excellent transverse containment & particle flow separation.
- MAPS ECal effort underway for the SiD design.
  - Digital pixels for ECal and tracker.
  - An effort led by SLAC, with CERN, is progressing on the ideal MAPS design.
- Heat management is critical to successful operation.
  - Power pulsing for Linear Collider
  - Need FCC solution - design with cooling?
- The digital ECal provides excellent performance for particle flow reconstruction.
- Future - simulation of full SiD detector with high granularity of MAPS ECal.
  - What are the limits of transverse separation and measurement?



J. Brau et al., "The SiD Digital ECal Based on Monolithic Active Pixel Sensors," EPJ Web of Conferences 315, 03005 (2024)

Conclusion

- Silicon-tungsten calorimetry offers potentially exceptional particle flow performance in a Higgs factory detector.
- MAPS is advancing SiW designs over analog devices.
- Further studies needed to understand optimized application of silicon-tungsten calorimetry to each collider concept (linear or circular).
    - Each collider brings specific and different constraints.
- We welcome colleagues who are interested in joining this effort.