Feature Extraction with Waveform Sampling

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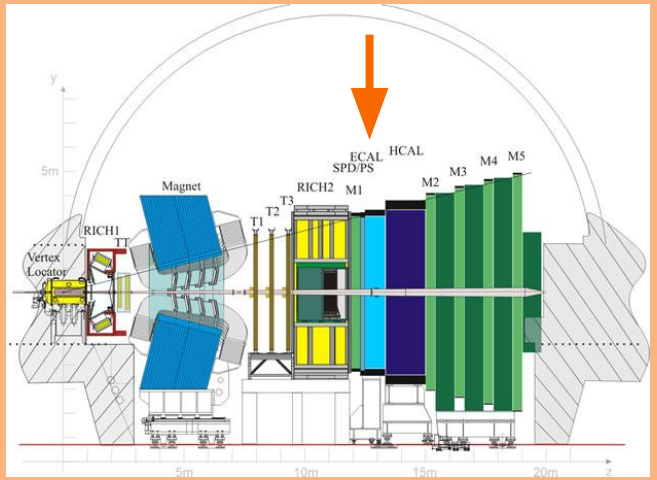
Time Stamping Introduction

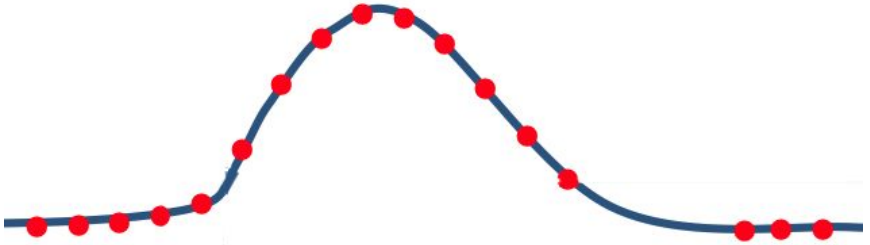
- Timing information is critical for reducing pileup
- The future electromagnetic calorimeter upgrade (PicoCal) will experience significant pileup with the increase in luminosity during HL-LHC
- R&D has begun on a proposed timing layer option that would reside inside calorimeter modules
  - Aimed to improve timing for photons, electrons and positrons with energies above a few GeV
- Feature extraction through waveform sampling methods could prove useful for future collider experiments
  - Calorimetry, Hadron ID

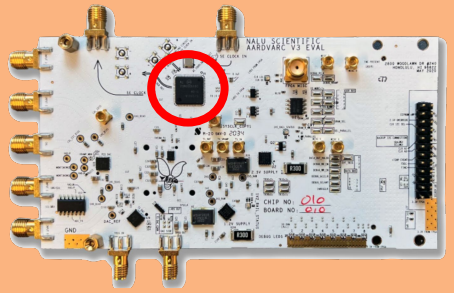


The current ECAL is critical for reconstruction of neutral particles

Waveform Sampling with the AARDVARC

- Pileup disentanglement and pulse timestamps can be achieved by repeated sampling of the waveform



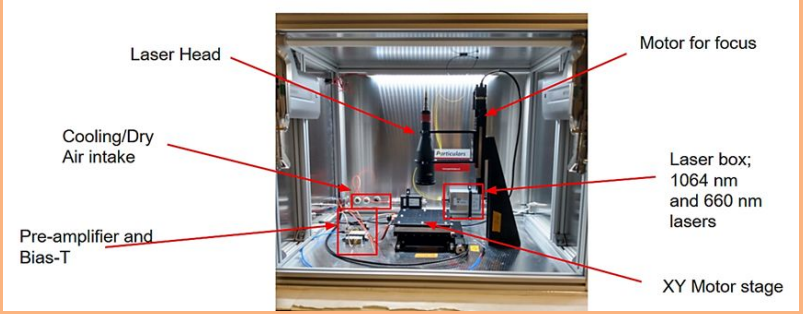


Currently working with the AARDVARCv3 chip from Nalu Scientific

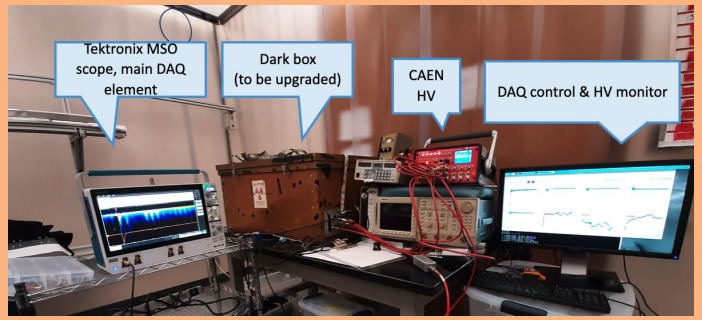
Pros	<10ps timing resolution, driven by 40MHz clock, multichannel, 10GS/s sampling rate
Cons	Large analog pipeline, slow digitization rate <20kHz, cumbersome calibration procedure

Laboratory Setup

The AARDVARC is ideal for evaluating potential timing layer solutions currently investigated at Syracuse

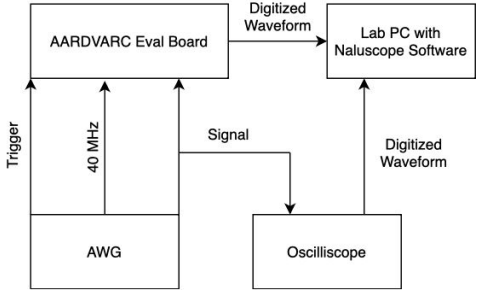


LGAD testing station



LAPPD testing station

- A clean pulse from a Tektronix AWG can be used to evaluate the AARDVARC's intrinsic time resolution for a given pulse shape
- These pulses can themselves be characterized via oscilliscope

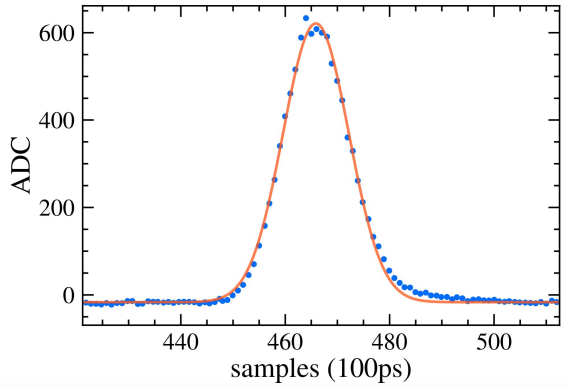


Measuring Time Of Arrival (TOA): dCFD and Fits

Waveform Fitting

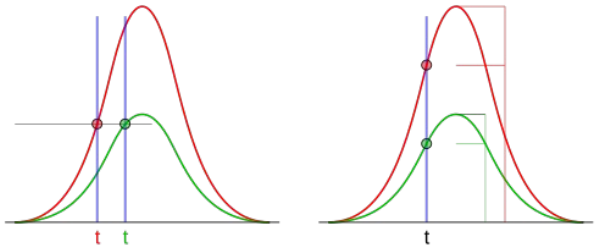
A least squares fit of the digitized samples to the shape of the generated waveform

- Computationally intensive
- Very precise
  - σ < 4ps



Digital Const. Fraction Discrimination

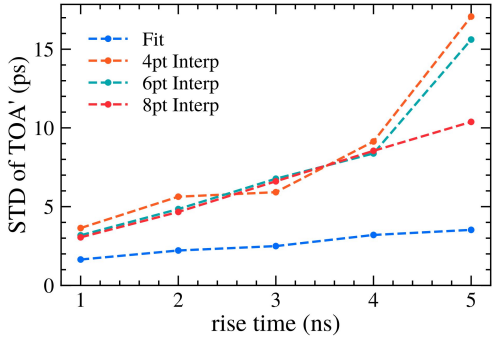
A constant fraction of the pulse's height is used as a threshold to determine TOA



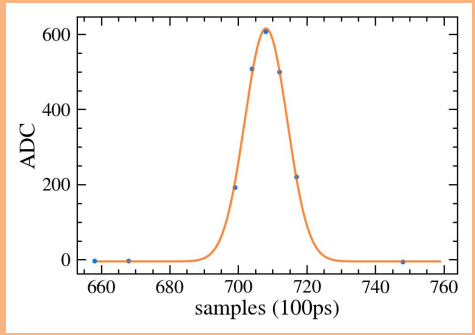
- No "time-walk" effect as with constant threshold discriminator
- Easily implementable in FPGA
- Currently used by LHCb PicoCal team in test beam to derive time resolution

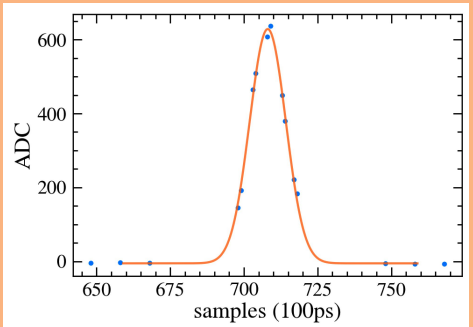
Influence of Signal shape on Timing: Case Study

- A sensor and amplifier configuration ideal for ps level timing provides good S/N and maintains a sharp rising edge
- Measurements made with 250mV Gaussian pulse from AWG
- 4,6,8 points used in dCFD interpolation
- ~100 points used to fit waveform
- RT's calculated as 10%-90% of amplitude



- Of course, fitting many points of a waveform isn't realistic.
- Performance mostly retained when fitting less pts
- 8pt, 16pt and 100pt fits have jitters of 2.4ps, 1.9ps and 1.6ps respectively for a RT of 1ns

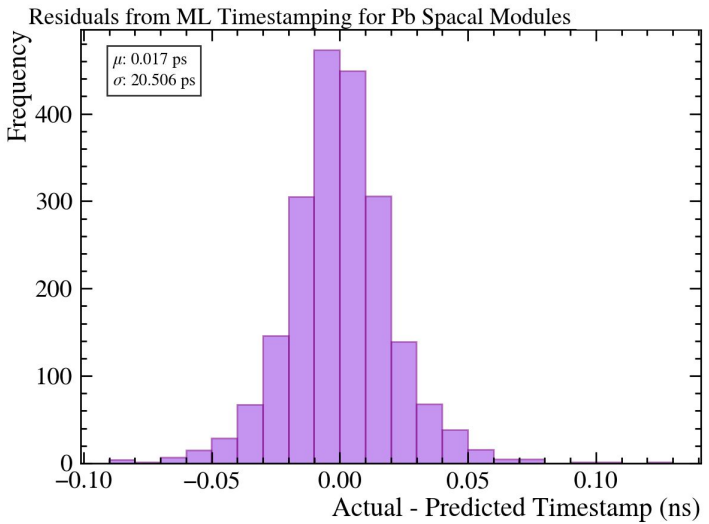


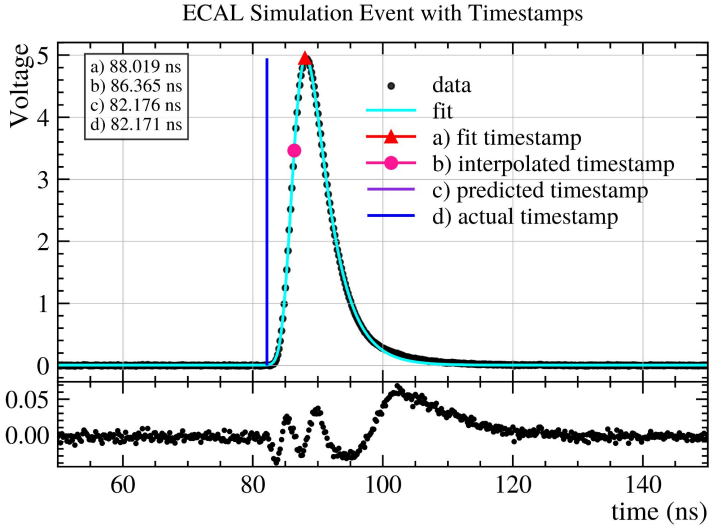


Measuring Time Of Arrival (TOA): Machine Learning

A BDT can be trained to extract a timestamp from a sampled waveform

- Trained on ECAL MC simulation
- Using single photons, Pb spacal config

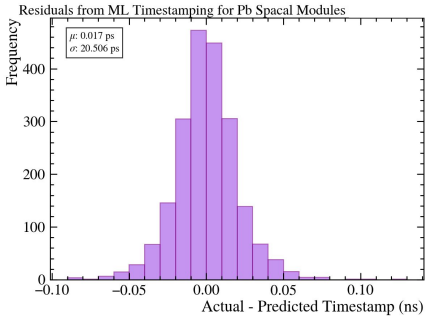


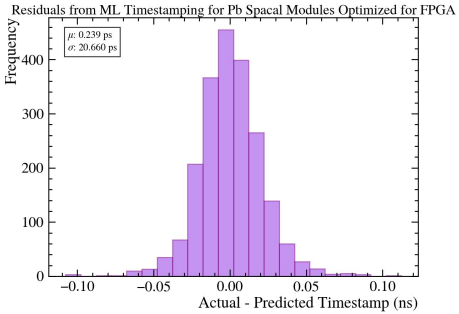


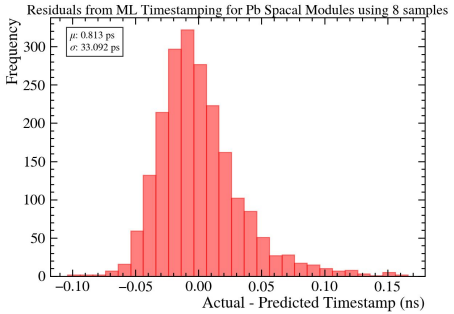
- BDT capability for dealing with pileup TBD

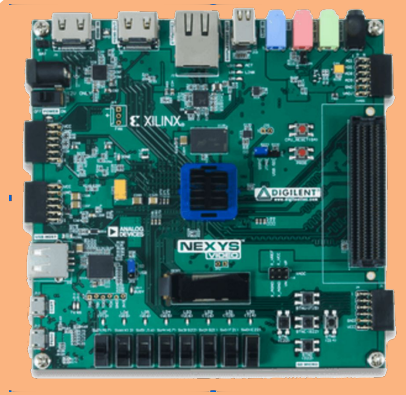
Timestamping on an FPGA

- Feature extraction should be done in real time
- Need to reduce computational requirements while maintaining performance
- ML algorithms should be optimized for FPGA implementation
  - Unoptimized BDT (Left): **200** trees, **22,966** branches, **46,132** leaves
  - Optimized BDT (Middle): **25** trees, **109** branches, **243** leaves
  - Optimized BDT using only 8 sample points along rising edge









Working with a Xilinx Nexys Video Eval Board

Future Prospects

- Apply timestamping methods to test beam data, model AWG produced waveforms using testbeam pulses
- Incorporating in time and out of time pileup into waveforms generated by AWG
- Integrate AARDVARC into LGAD and LAPPD readout
- More in depth study of how time resolution degrades in a real system