3D Integration

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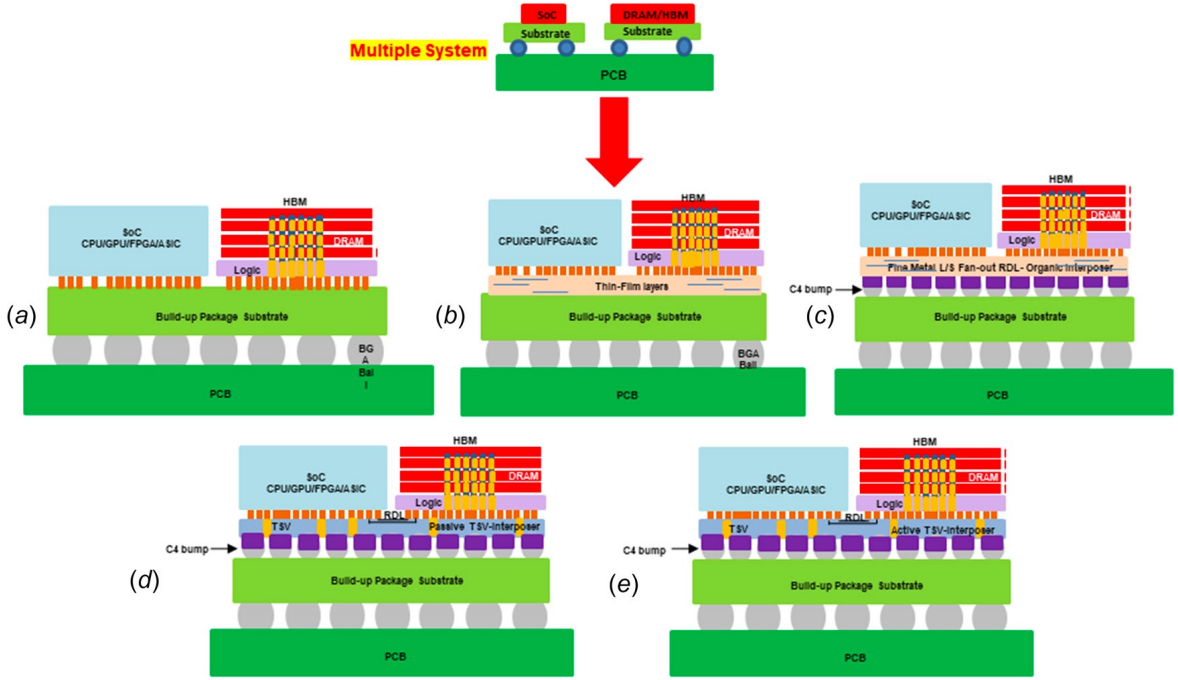
U.S. DEPARTMENT OF ENERGY
Stanford University
SLAC NATIONAL ACCELERATOR LABORATORY

Commercial Semiconductors - SOC

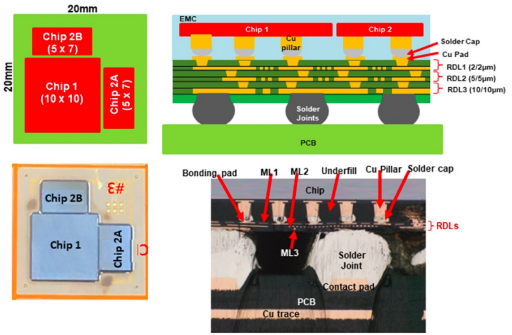
- System-on-chip or ”SoC” dominated scaling approach till mid-2010’s
  - Combines logic blocks, memory, analog, RF etc on a single chip
- Limitations to continued scaling
  - Technology scaling slows down
  - Design costs increasing
  - Need for distinct technologies: heterogeneous integration
  - Increasing complexity -> yield limitation
- 3D integration becomes more attractive
- Technology innovations
  - TSV’s – materials, formation, stress
  - Fine pitch chip-to-chip bonding
  - Handling of thin substrate

Ref: S. Iyer, ”Heterogenous Integration for Performance and Scaling”IEEE Trans. On Components, Packaging and Manufacturing Technology, July 2016

SOC's continued



- Note vertical *and* lateral integration



Ref: John Lau, "Recent Advances and Trends in Chiplet Design and Heterogeneous Integration Packaging" ASME Journal of Electronic Packaging

Commercial Semiconductors: Image Sensors

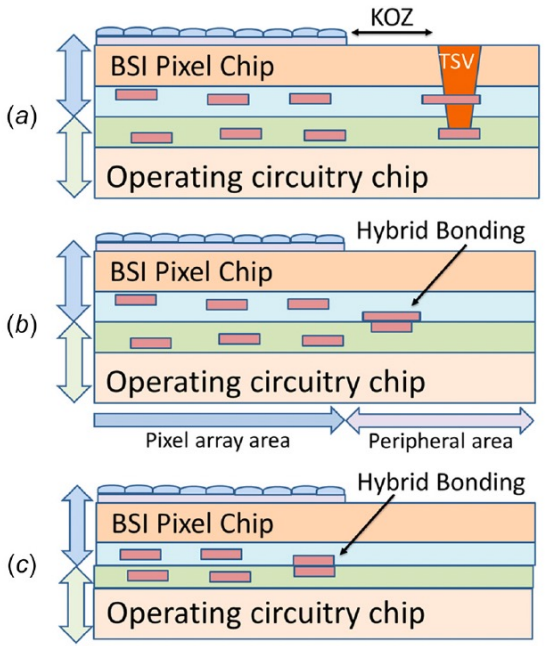
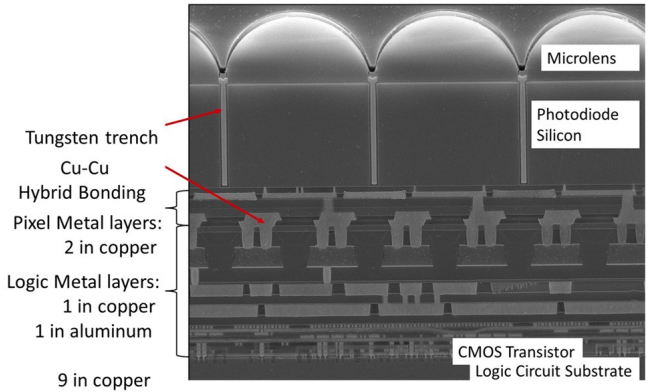


Fig. 8 Chip-to-chip bonding and interconnect methods with (*a*) direct dielectric bonding followed by via-last TSVs for chip-to-chip interconnect, (*b*) hybrid bonding at peripheral area, and (*c*) hybrid bonding under pixel arrays

Image Sensor Die - Cross Section

(Source: Apple IPad Pro LiDAR Module structural, process & cost report, System Plus Consulting, 2020)



- Pixel chip must be exposed for optical sensor
- Position dependent connections
- Mostly 2-chips, 3-chip stacks used for complex processing (Sony rolling shutter)

Ref: M. Lu, "Advancement of Chip Stacking Architectures and Interconnect Technologies for Image Sensors" ASME Journal of Electronic Packaging

3D Integration for HEP Detectors

- Wafer-to-wafer bonding
  - Necessary for <2 layers of chips
  - As bump-bonding replacement for bump-bonding hybrid detectors
    - Potential for finer pitch
    - Potential for lower cost
- TSVs (through silicon vias)
  - Large dimension/pitch in the periphery areas
  - Small diameter in arrays and/or logic
- Availability/continuity of vendors supporting these processes in an issue

3D Integration for HEP Detectors – Demonstration Projects

- LETI/Cern: Demonstration of TSV process on Medipix3 130nm CMOS chips – D. Henry et al 2013
- Fermilab: Demonstration of Copper-to-copper bonding at wafer-to-wafer and wafer-to-chip level and TSVs to create a functional 3-chip stacked detector – G. Deptuch 2015 and R. Lipton 2017
- ATLAS Read-out chips: Demonstration of TSV process, most recently on FE-14, T. Frisch 2022
- SiPMs: Sherbrooke, FBK/INFN 2023, 2-layer

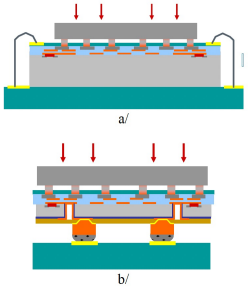


Fig 1: a/ Current assembly of sensor to readout circuit, b/ New assembly of device connected by the solder BGA on the back side of the readout circuit chips using TSV

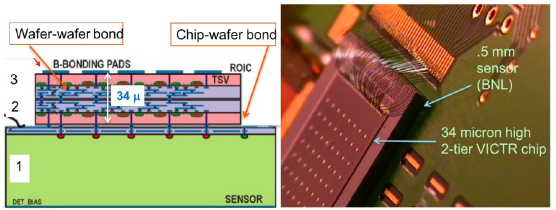


Figure 1: Left - Sketch of the two-tier 3D Stack. Right - Photograph of the VICTR stack mounted on a PC board.

SLAC/Fermilab/LLNL 3D Integrated Sensing Solutions

- Funded under DOE “Accelerate Innovations in Emerging Technologies”
- Develop technologies for 3D integration of detectors with **28nm CMOS read-out chips** and **LGAD sensors** for optimal performance (speed, pixel size, power)
- Develop LGAD technology and build proto-types on 300mm wafers
  - Partnering with Tower Semiconductor
  - Design will include 100μm and 50μm pitch proto-type sensors
  - LGAD process on 12inch wafers, capable of 3D integration with 28nm ASICs
- Develop advanced read-out chips on 28nm CMOS
  - Initial MPW run with linear pixel array to evaluate ASIC design blocks in 28nm CMOS
  - 2nd MPW run with proto-type size array, incorporating learning from 1st MPW run
- At the end of 2nd year, we anticipate first demonstration of 28nm read-out chip bump-bonded to an LGAD array with leading edge timing performance
- For the next phase, we would proceed to wafer-to-wafer bonding of 12inch LGAD and 28nm ASIC wafers, and 3D integration process modules