



## 4D Tracking and Related Developments at Fermilab

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4D Tracking workshop 2024, SLAC

# Overview

Note: 10min presentation – many of the slides are provided as reference

- Current 4D tracking detectors at Fermilab:
  - SMART Pixels (28nm, NN classifier in pixel, CMS pixel upgrade)
  - ETROC (LGAD, CMS ETL)
  - FCFD (LGAD, EIC R&D)
  - ps cryo TDCs (22nm) and cryo timing (SNSPDs)
  - 3D LGADs (SLAC, LLNL, 28nm (ROIC) + 65nm (LGAD)) – Front End
- Not covered in this talk:
  - 3D IC → key to low mass, alternative to MAPS
  - Sensor co-development (e.g. MAPS)
  - Compact per pixel ADCs (e.g. 100KSPS 10b SAR, ~30x30um in 65nm, 40uW)
  - IP block development in 28nm, asynchronous pixel readout, rad-PDK...

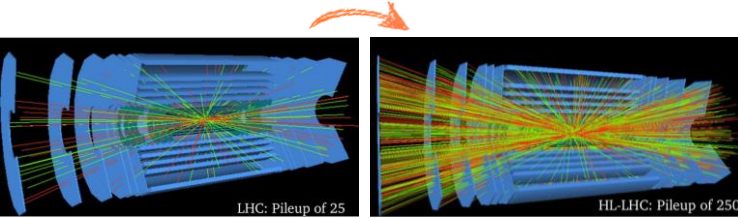
# Smart Pixels: In-pixel AI for on-sensor data filtering

- **AI in pixel**, including digital/analog/beyond CMOS
- Expanding the **Smart Pixel Collaboration** (FNAL, John Hopkins, UIC, UChicago, Northwestern, Purdue, Kansas State Uni, ORNL, Sandia)
- NSF POSE Award to support HLS4ML and make it widely available to the community (Northwestern, UIC and UIUC, Arizona State, Fermilab) *An Open Source Ecosystem for Collaborative Rapid Design of Edge AI Hardware Accelerators for Integrated Data Analysis and Discovery*
- **AI on edge**, including fully reconfigurable on eFPGA: Northwestern+Columbia+Fermilab funding for 3Y to develop design methodology for eFPGAs
- AI chipelets/custom accelerators
- Distributed AI communications across chips: photonics AI

Large collaboration and ecosystem, good candidate for a university-led initiative



# Phase II upgrade HL-LHC CMS



- ❑ More than 90% of this data was produced by one detector subsystem: **silicon pixel detector**
- ❑ Pixel detectors have the highest data rates in high energy physics ... **and getting higher!**
- ❑ In 2018, CMS saw ~40 simultaneous pp collisions
  - The High Luminosity LHC will increase this to ~200
  - **5 times improved luminosity (radiation)**
  - 7 times higher interaction rate (~3Ghit/cm<sup>2</sup>)

Currently being Installed	Beyond 2030: What we are investigating
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Technology	65nm CMOS	28nm CMOS
Pixel ROIC size	50x50 μm <sup>2</sup>	25x25 μm <sup>2</sup>
Pixel Sensor size	100x25	50x12.5 μm <sup>2</sup>
Pixels	394x400 = 157.6k	788x800 = 0.63M
Detection threshold	~1000e-	~500e-
Hit rate	< 3GHz/cm <sup>2</sup>	< 3GHz/cm <sup>2</sup>
Trigger rate	1MHz	40MHz (?)
Digital buffer	12.5 μs	(?)
Readout data rate	1-4 links @ 1.28Gbps	Photonic link @ 30-100 Gbps
Radiation tolerance	500Mrad at -15°C	1Grad at -15°C
Power	1 W /cm <sup>2</sup>	1 W /cm <sup>2</sup>

Credit: Jennet Dickinson

# Pixel detector R&D effort for “Phase III”

## Applications

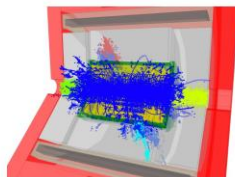
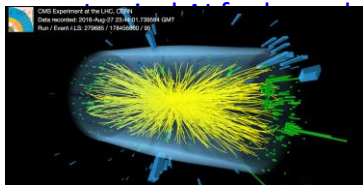
### HL-LHC Phase III upgrade R&D

- 28nm process node
- 4x pixel size reduction
- 2x improve threshold detection
- 40x faster sampling rate
- 1W/cm<sup>2</sup>

### Future colliders

- [Smart pixels with data reduction at source: possible applications for linear e+e- colliders](#)

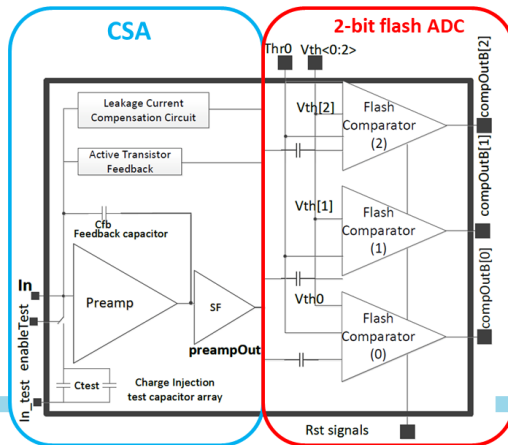
### Xray sources (e.g. Ptychography)



CMS & Future colliders (hh, ee, uu)

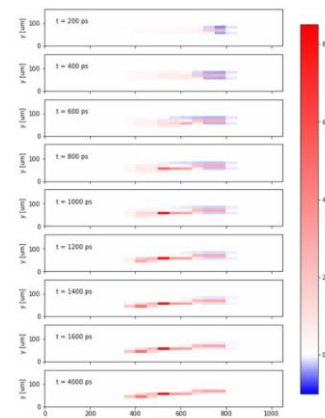
## ROIC Implementation

- Low power, low noise preamplifier with a leakage compensation
- A low power 40MSPS synchronous comparator architecture with auto-zero capability to create an in-pixel ADC
- On chip data reduction capability using AI/ML techniques



## Smart Pixel dataset

- Open Access simulated dataset of silicon pixel clusters produced by charged particles (pions), where the particle kinematics are taken from fitted tracks in CMS Run 2 data.
- Morris Swartz, & Jennet Dickinson. (2024). Smart pixel dataset (Version 3) [Data set]. Zenodo. <https://doi.org/10.5281/zenodo.10783560>

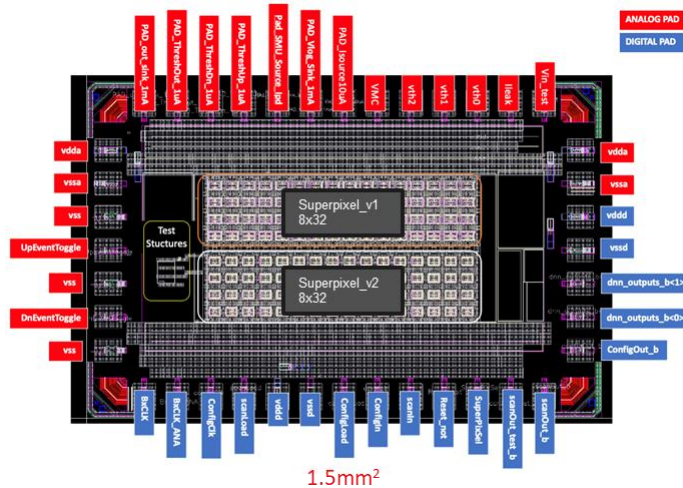




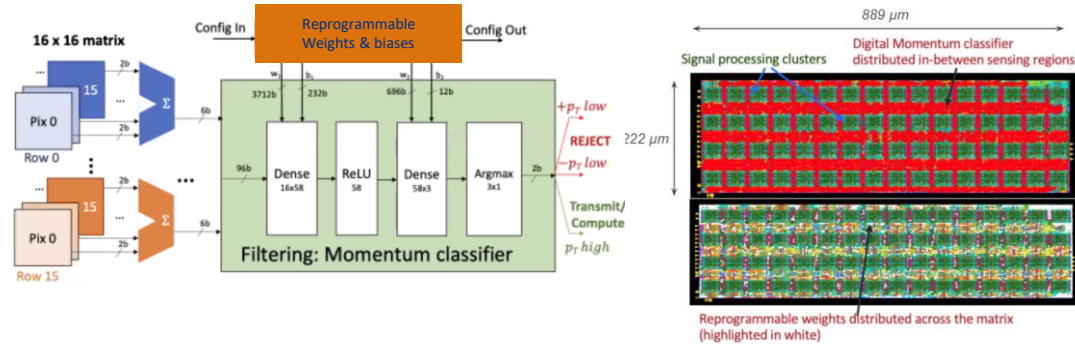
# Ongoing Effort for “Phase III” pixel replacement

## First Prototype Implementation:

- Analog frontend without ML/AI backend
- TSMC HPC+ 28nm
- Two 8x32 pixels matrices called Superpixel
- Pixel size: 25 $\mu$ m x 25 $\mu$ m
- ASIC size: 1.5mm<sup>2</sup>



## Second Prototype Implementation:



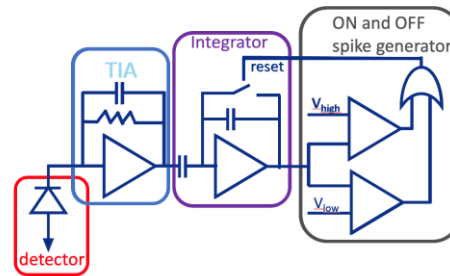
- **Co-Design** development with analog frontend pixels tightly connected to a fully combinatorial digital classifier
- 300uW of power for 256 pixels
- ~1uW/pixel to ensure our goal of 1W/cm<sup>2</sup>
- Classifier allows to reject 75% of the clusters
- Reducing power required for data transfer

# Future R&D

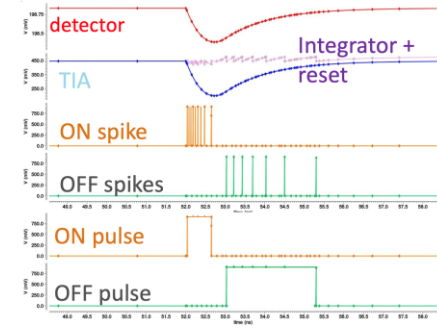
## (1) Neuromorphic Solution

- Event-driven Front-End Architecture
- Spiking Neural Network (SNN) backend

Algorithm -> Digital -> Analog

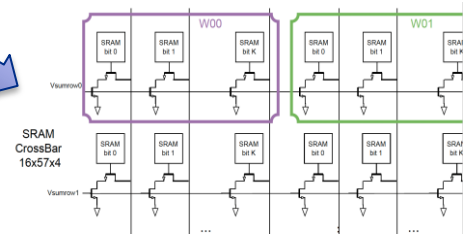
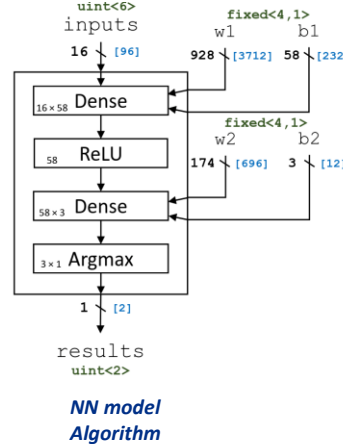


- Pulse shape encoded in spike train
- Ultra-fast signal processing ~ 100ps
- Digital processing – power constraints
- Analog processing – device constraints (speed)

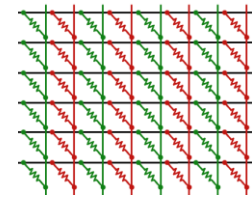


## (2) Analog AI Back-End:

- Implement analog classifier counterpart for a cluster of pixels
- Develop ROIC prototypes:
  - SRAM based solution
  - Floating Gate based solution
  - Beyond CMOS ReRAM based solution



Analog NN model with SRAM

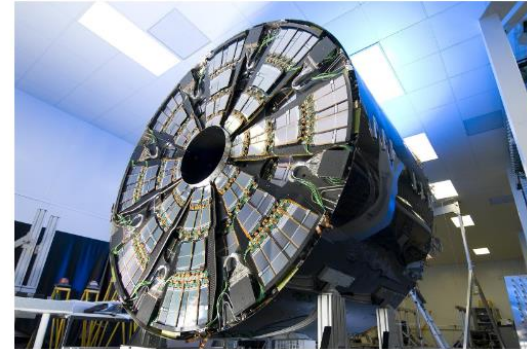
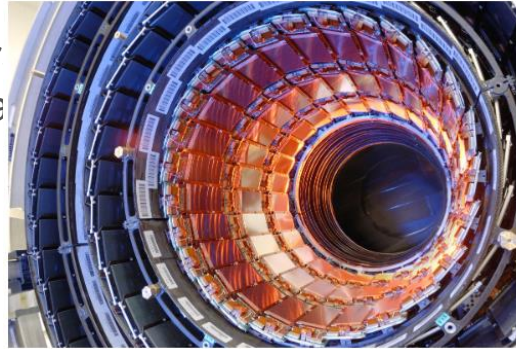


Analog NN model with ReRAM

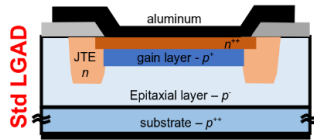
# LGAD Tracking Detectors

- Future colliders need tracking detector with 5-25 ps timing and 5-30  $\mu\text{m}$  spatial resolution [11]:

- FCC-hh
- Electron-Ion Collider (EIC)
- Muon Collider...



- LGADs are a leading sensor candidate with 20-30ps timing resolution, but how to read them out?



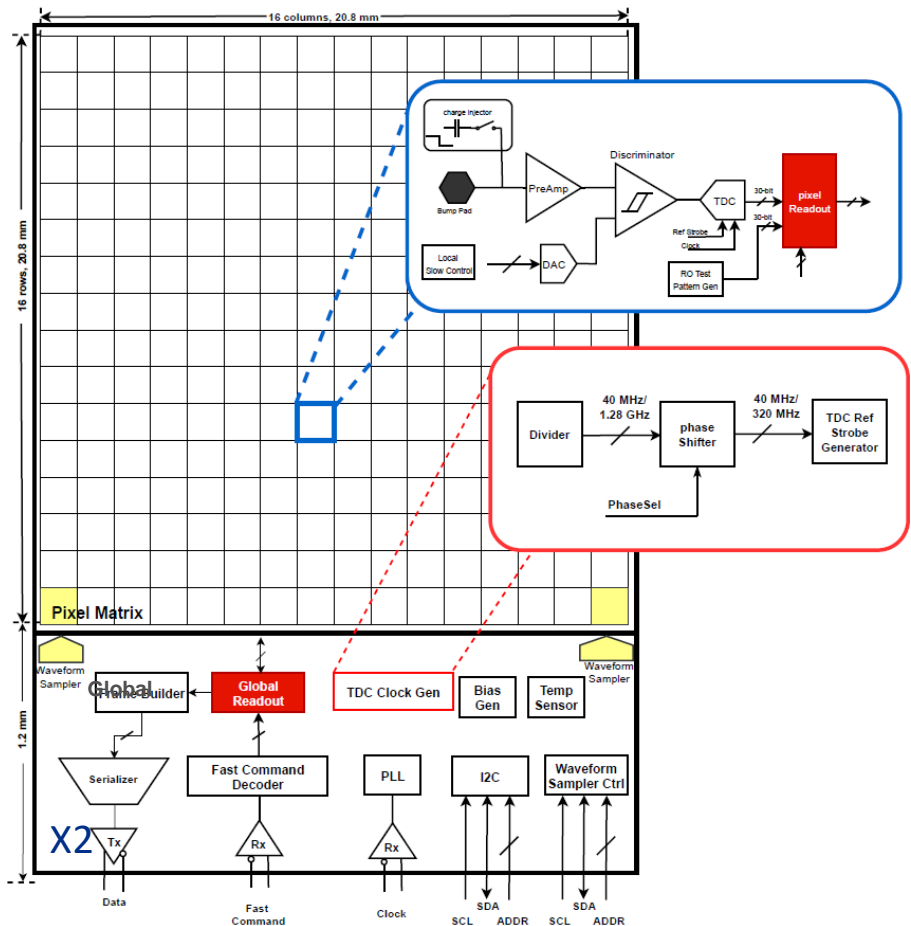
Single LGAD pixel

HEP Application	Pitch Range	Time Resolution	Power	Noise - ASIC	Frame Rate	Gain
e+ e- collider	~ 1 mm	< 10 ps	~1 W/cm <sup>2</sup>	n.a.	Circular ~50MHz Linear 120Hz-300MHz	~10
Proton or muon collider	< 25 $\mu\text{m}$	< 10 ps	~1 W/cm <sup>2</sup>	n.a.	40 MHz	~10
BES Application	Pitch Range	Time Resolution	Full Well	Noise - ASIC	Frame Rate	Gain
Soft x-ray imaging	100 $\mu\text{m}$	n.a.	> 100 keV	< 1 keV	< 1 MHz	> 5
Mossbauer Spectroscopy	100 $\mu\text{m}$	< 5 ns	> 1 MeV	< 4 keV	< 1 MHz	> 5
X-ray Spectroscopy	> 100 $\mu\text{m}$	n.a.	< 20 keV	< 100 eV	< MHz	20
Momentum Microscope	100 $\mu\text{m}$	< 100 ps	> 30 keV	< 1 keV	1 MHz	20
FES						
LCLS Pulse Train	100 $\mu\text{m}$	< 350 ps	> 3 MeV	< 2 keV	>3 GHz burst	3-5
NIF	< 100 $\mu\text{m}$	< 20 ps	> 10 MeV	< 3 keV	>50 GHz burst	~10



# ETROC Overview

- 16x16 pixel matrix: 1.3 x 1.3 mm<sup>2</sup>
- Measuring arrival time of LGAD signal
  - Front-end: PA + Discriminator + TDC
- L1 trigger-driven readout with zero suppression
- Flexible trigger path
- Fast waveform sampling for two pixels
- Interface of ETROC
  - 40 MHz reference clock
  - I2C-based slow control
  - 320 Mbps fast control
  - Two serial links: each up to 1.28 Gbps
- Time resolution contribution: ~ 40 ps
- TSMC 65 nm technology, 1p9m, 1 W/chip@1.2 V
- 100 MRad TID tolerance, SEE protection for controls



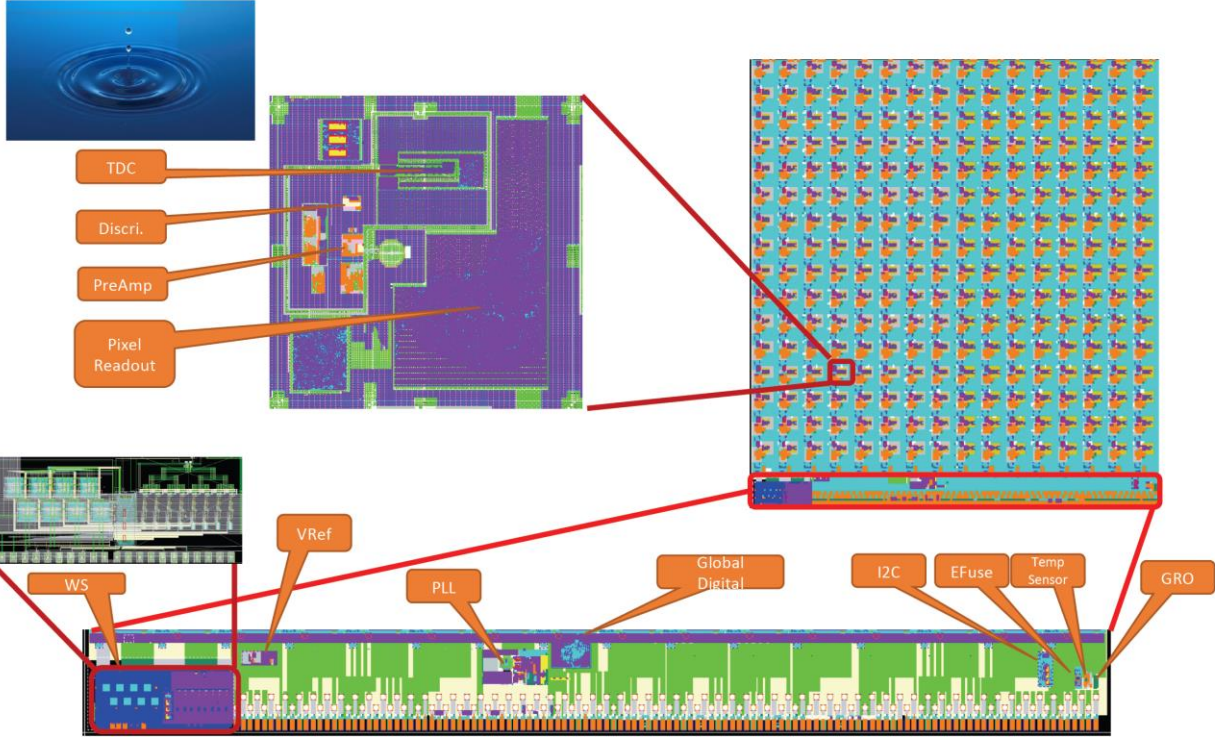
# ETROC2 architecture and testing

From Ted Liu's presentations:

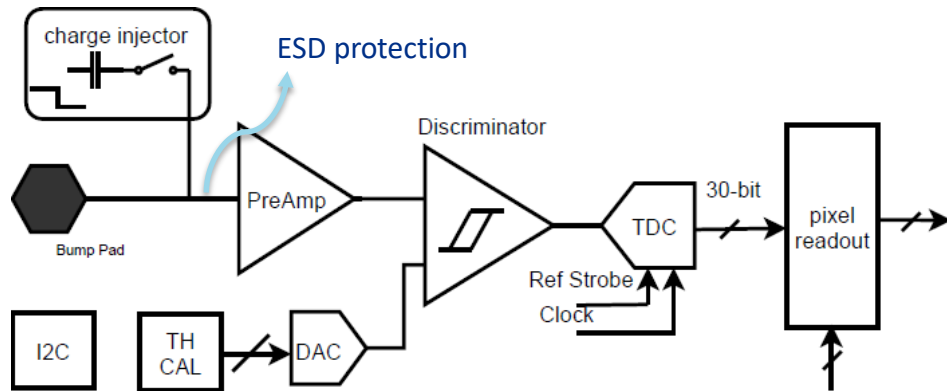
<https://indico.bnl.gov/event/20473/contributions/85273/attachments/51866/88691/ANL-workshop-ETROC.pdf>



*ETROC2 layout (submitted on Oct 21, 2022)*

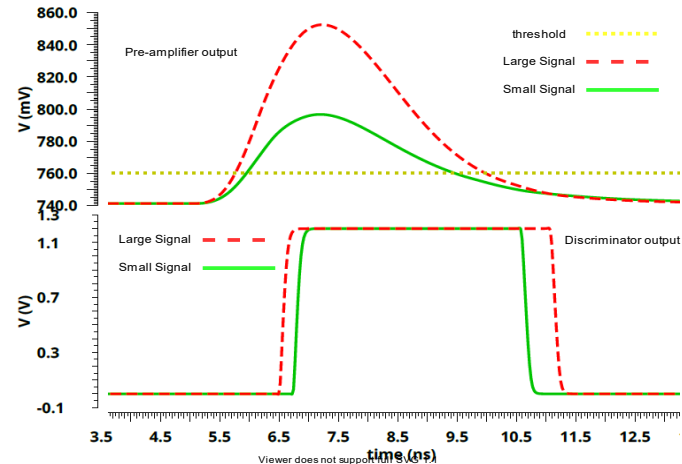


# ETROC Front-end



simplified diagram of ETROC pixel

- The front-end (**PA + Discrim. + TDC**) serves to measure the TOA and TOT of the input signal [1][2]
  - ESD protection at PA input
  - Time walk is corrected with TOT
- A **charge injector** helps test the chip
- A **10-bit voltage DAC** provides threshold voltage to the discriminator
  - threshold can be automatically calibrated in-pixel [3]



Waveform example of PA and Discrimi

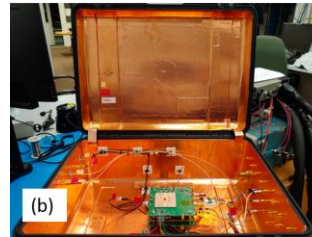
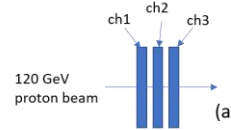
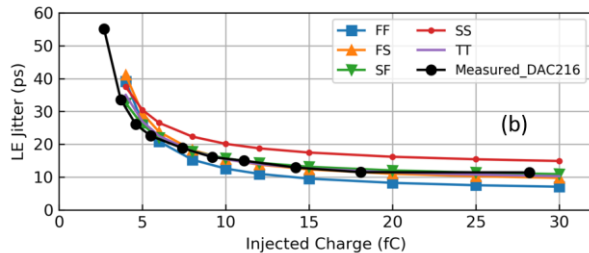
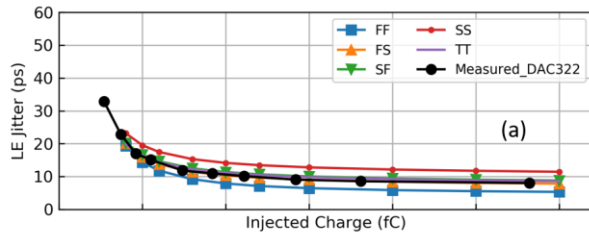
- [1] Characterization of the CMS Endcap Timing Layer readout chip prototype with charge injection
- [2] A Low-Power Time-to-Digital Converter for the CMS Endcap Timing Layer (ETL) Upgrade
- [3] In-pixel automatic threshold calibration for the CMS Endcap Timing Layer readout chip

Blue: prototyped and tested

# ETROC Analog Front-end Performance

The analog front-end (PA+Discriminator) taped-out in ETROC0 and tested extensively

- Measured jitter consistent with expectation
- DAC DNL  $< \pm 0.2$  LSB  $\rightarrow$  meet design goal
- Irradiated to 100 Mrad TID  $\rightarrow$  no performance degradation found
- Got  $\sim 33$  ps time resolution from PA waveform in test beam
- Run sensor HV at beyond breakage voltage for a long period. no performance degradation found



# Bump bonded ETROC2 performance with charge injection

ETL spec is < 50 ps per hit:

LGAD contribution: ~30ps

ASIC contribution:

30ps line →

15ps line →

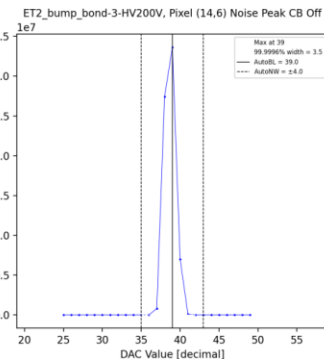
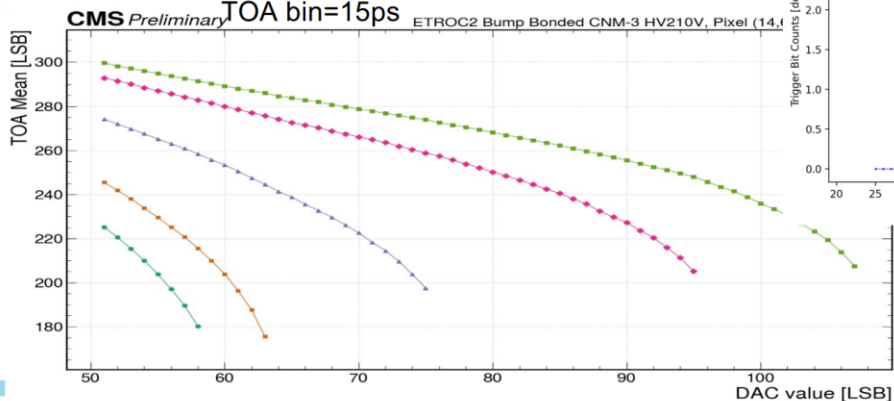
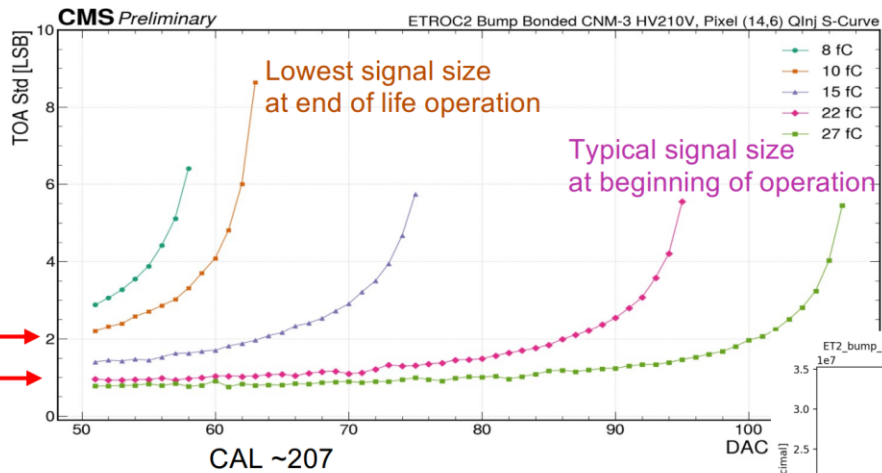


From charge injection results, the expected performance with sensor (roughly):

LGAD+ preamp/discriminator + TDC	34 / 42 ps
Time-walk correction residual	< 10 ps
Internal clock distribution	< 10 ps
System clock distribution	< 15 ps
Per hit total time resolution	39 / 47 ps
Per track (2 hits) total time resolution	28 / 33 ps

Initial operation: ~39 ps per hit

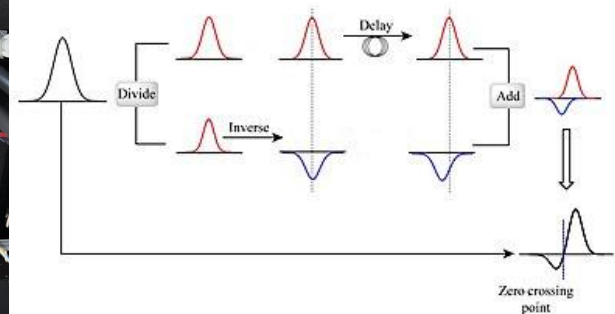
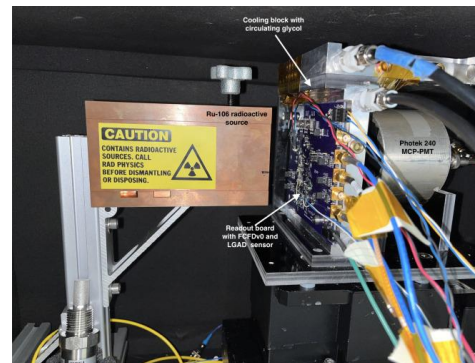
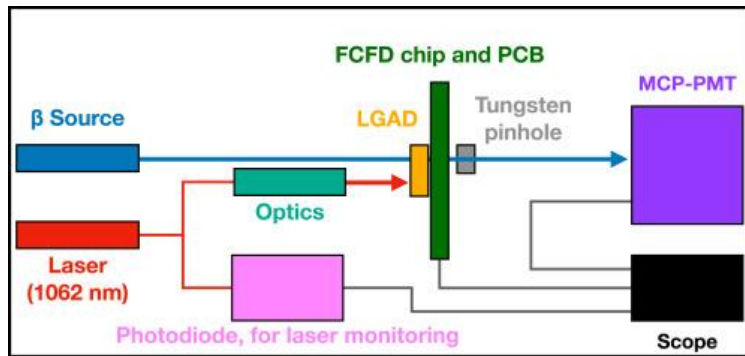
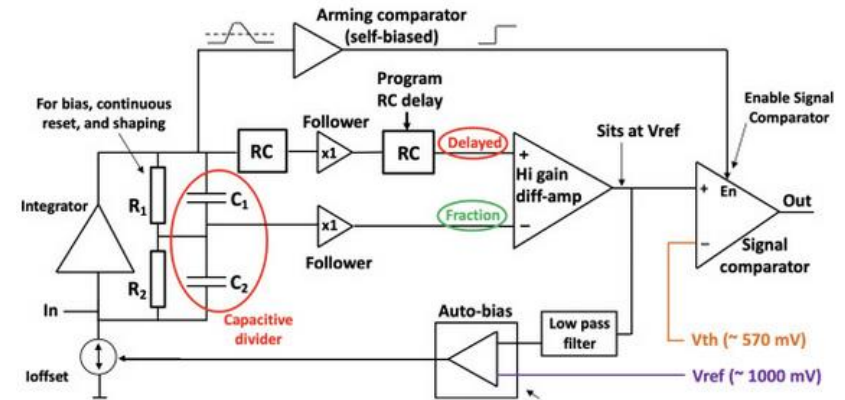
End of life operation: ~47ps per hit





# The Fermilab Constant-Fraction Discriminator (FCFD)

- FCFDv0 is a front-end readout chip for LGADs which uses CFD to locally compensate for input signal time walk.
- The FCFD includes pulse injection (5~26 fC) which mimics LGAD signals for easy characterization.
- 65nm strip LGAD readout now being translated to 28nm for 50um pixels

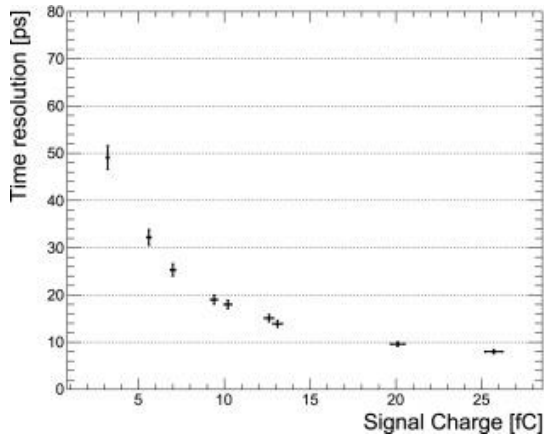


Images from [11]

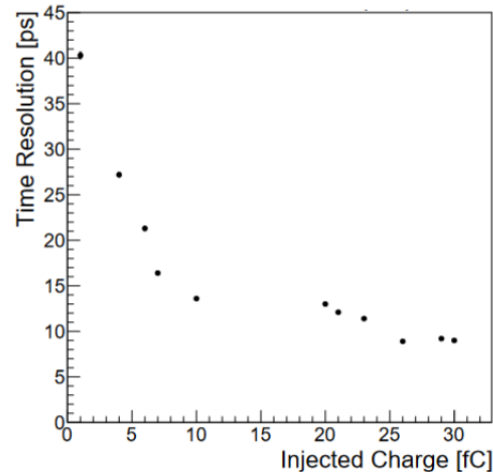
# Readout Results with FCFD

- CryoTDC v1 achieves sensor-limited readout fidelity with FCFDv0.
- Intrinsic readout RMS noise  $O(5\text{ps})$ .

Time Resolution vs Injected Charge Measured with an Oscilloscope (reference) [11]



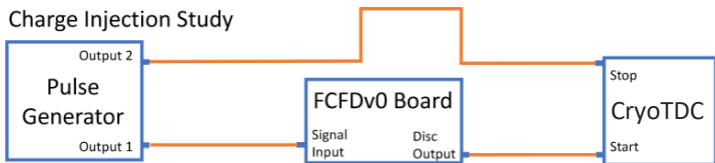
Time Resolution vs Injected Charge Digitized with CryoTDC v1



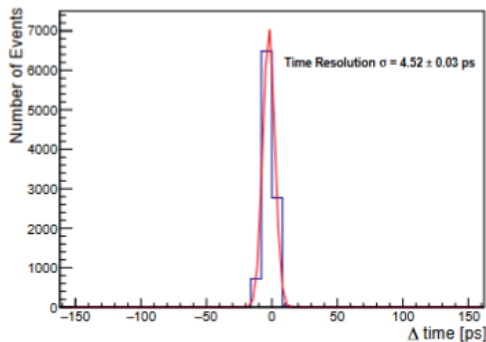
Pulse Generator Study



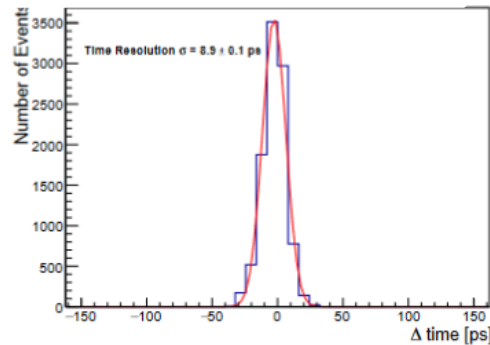
Charge Injection Study



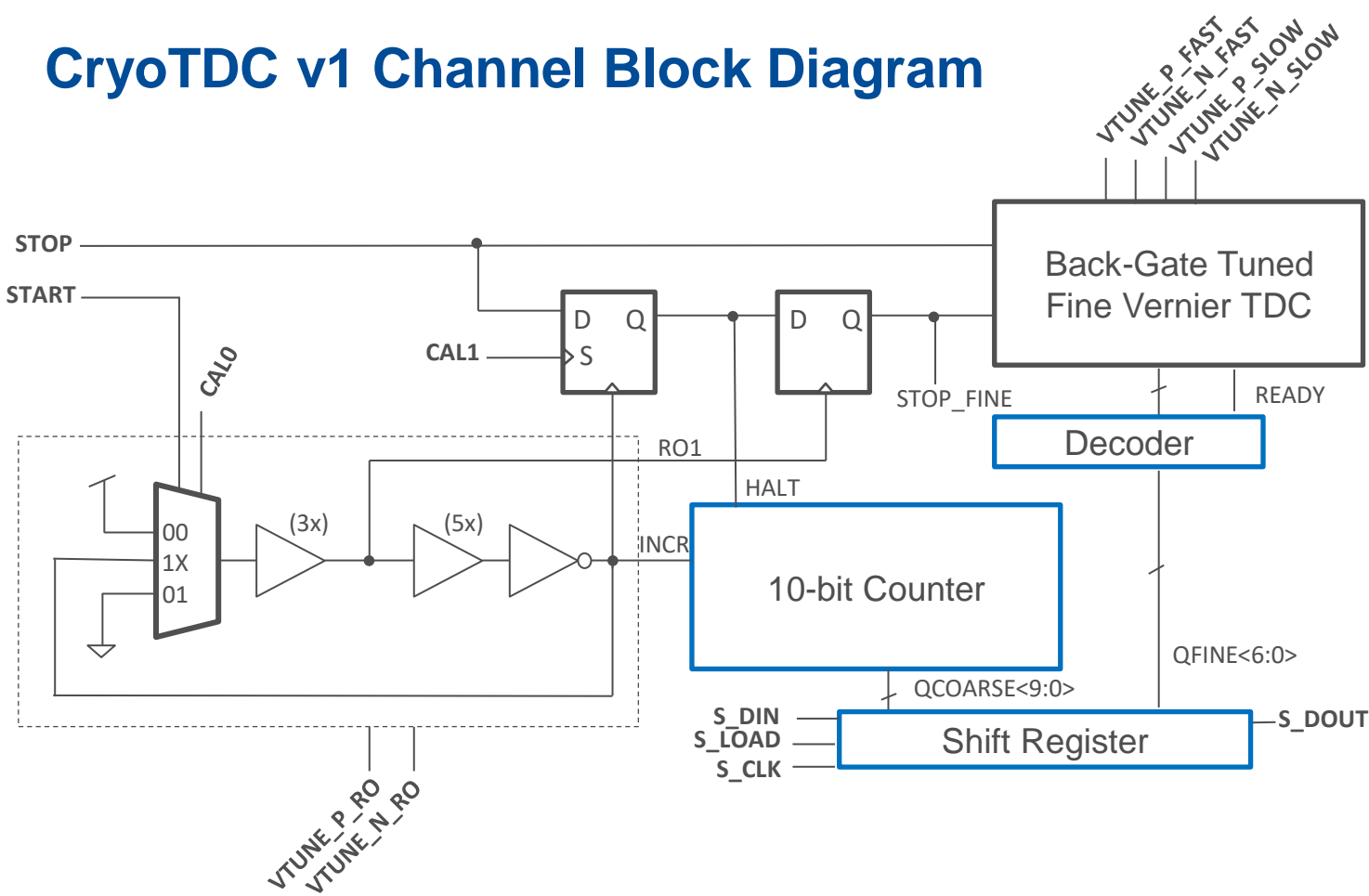
RMS Noise (Pulse Generator → CryoTDC v1)



RMS Noise (FCFD (26 fC) → CryoTDC v1)



# CryoTDC v1 Channel Block Diagram

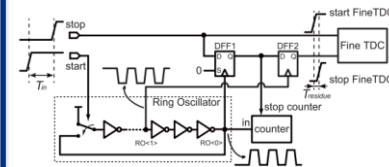


Total Pins: 22

- 6 analog inputs
- 7 digital inputs
- 3 digital outputs
- 6 power pins

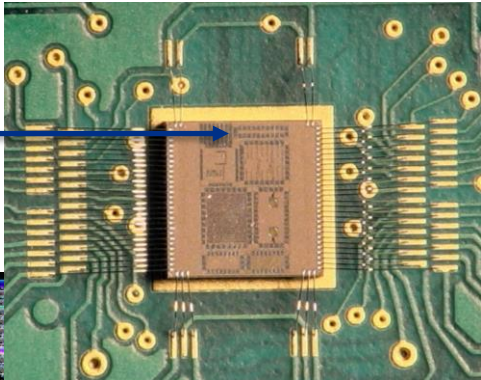
*Not Shown:*

- \* RO1, HALT, INCR, and STOP\_FINE are mux'd to **two** digital outputs with the select done by 4 shift register bits.
- \* RESET pin

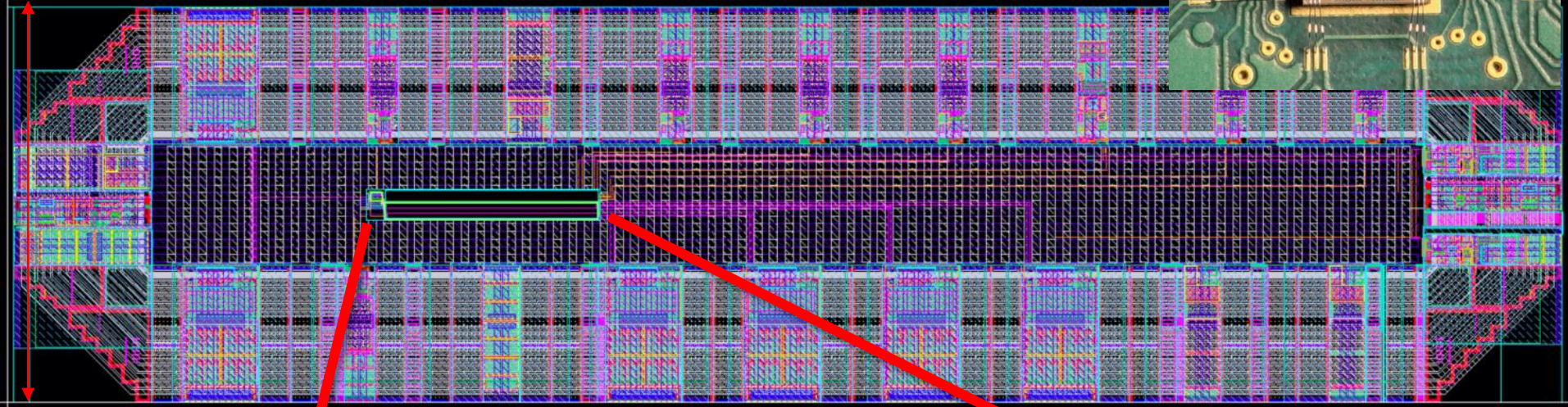


Enomoto et al. [2]

# CryoTDC v1 Test Chip 11/2021

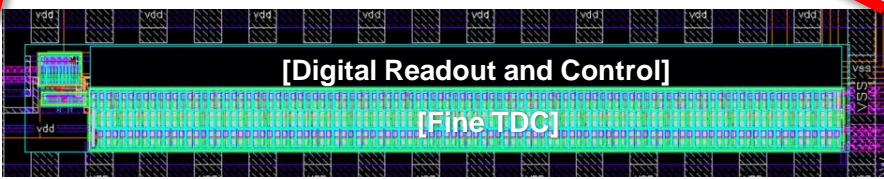


≈ 250 μm



≈ 1000 μm

≈ 20 μm



≈ 150 μm

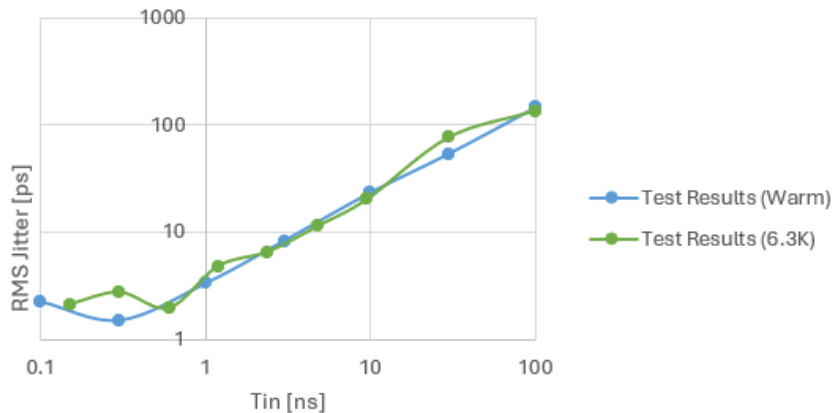


# CryoTDC v1 Jitter vs $T_{in}$

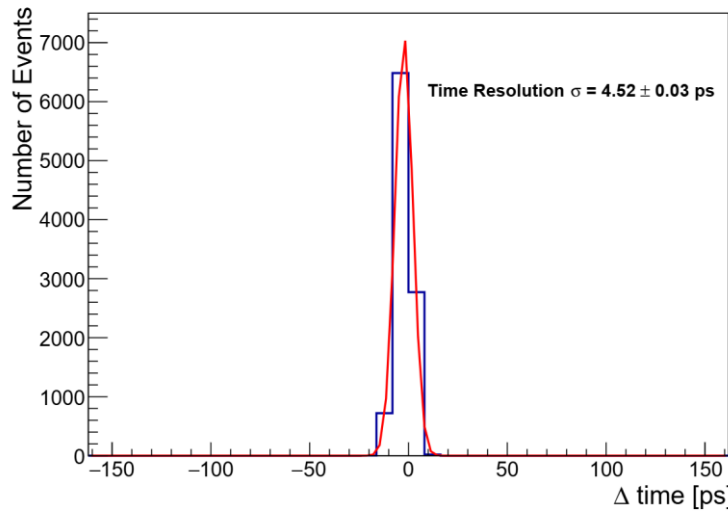
Figure of Merit	295 K	8.5 K
Quiescent Power ( $P_{Quiescent}$ , $\mu\text{W}$ )	109	46.6
Energy per fine ADC conversion ( $E_{fine}$ , $\mu\text{J}$ )	3.30	3.03
Ring oscillator power ( $P_{RO}$ , $\mu\text{W}$ )	193	142
Estimated channel power when operating at 100 Msps [ $\mu\text{W}$ ]	632	492

- At low  $T_{in}$ , test instrument jitter dominates the measurement.
- At high  $T_{in}$ , jitter accumulation in the ring oscillator results in a linear correlation.
- Flicker noise dominates thermal noise, so cryogenic results resemble warm.

## Test Results Summary

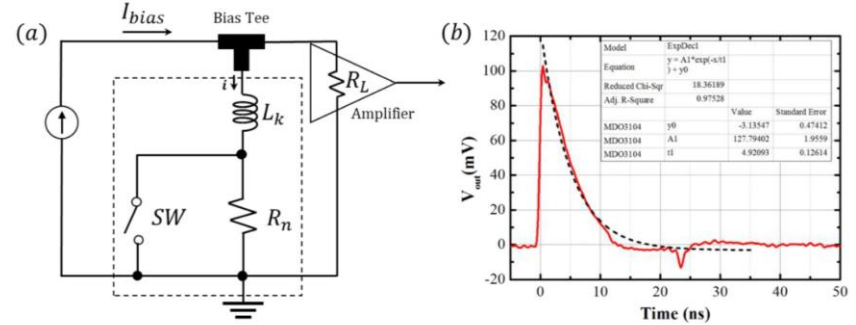
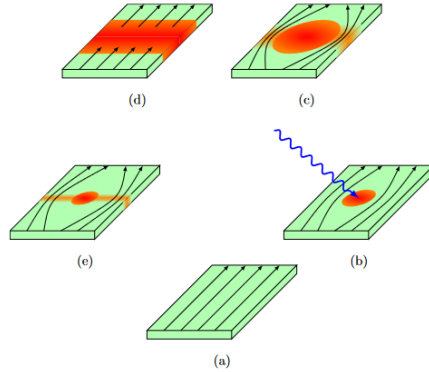
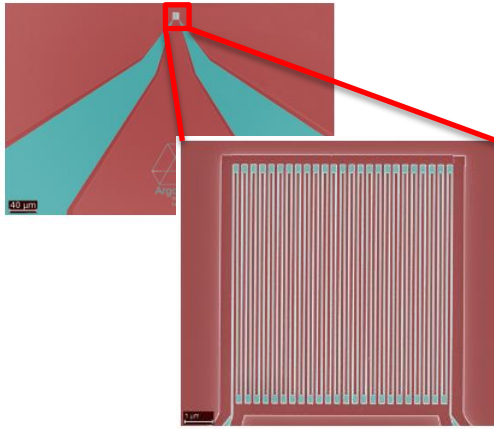


## Pulse Generator Test Using DILVERT readout





# Superconducting Nanowire Single-Particle Detectors (SNSPDs)



- Ideal inductors when superconducting
- Resistive when heated by a photon/particle

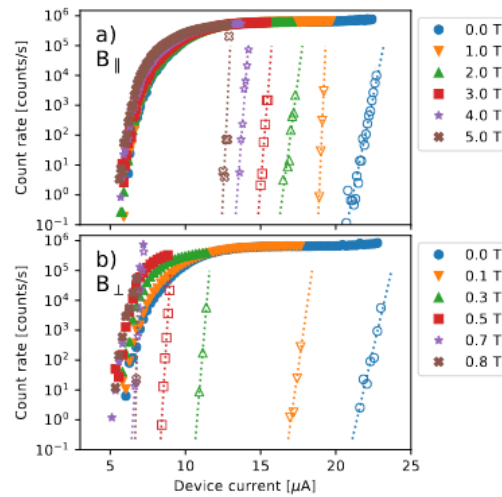
- Risetime  $\sim L_k / (R_n + R_L) \sim 100$ 's ps
- FallTime  $\sim L_k / R_L \sim 10$ 's ns

## Motivation:

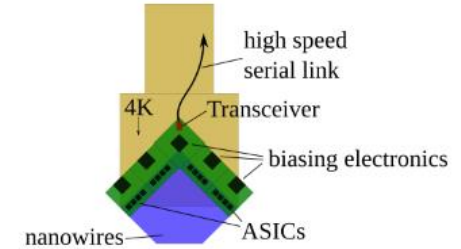
- SNSPDs are fast, and fast-timing ASICs are needed to preserve that resolution.
- **Cryogenic readout** designs are key to reduce heat load.

# SNSPDs at the EIC

- Electron-Ion Collider: Novel accelerator under development at BNL to probe proton mass, other challenges.
- SNSPD operation at cryo + high magnetic fields can help increase acceptance by instrumenting difficult regions of the machine.
- Radiation hardness under investigation.

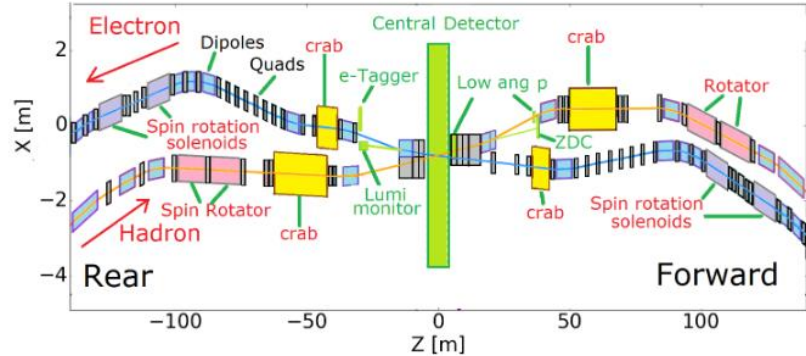


SNSPD operation at high B-field;  
zero dark counts.



Integration concept with SNSPDs, ASICs, and high-speed readout links.

## Electron-Ion Collider Diagram



# SUNROCK ASIC for SNSPD readout, biasing, and time tagging

- 22nm FDSOI for 4K operation
- 32x channels, a shared clock and readout architecture, and DC biasing for SNSPDs.
- Taped out last October. Test is currently underway, with results to be presented at CPAD.

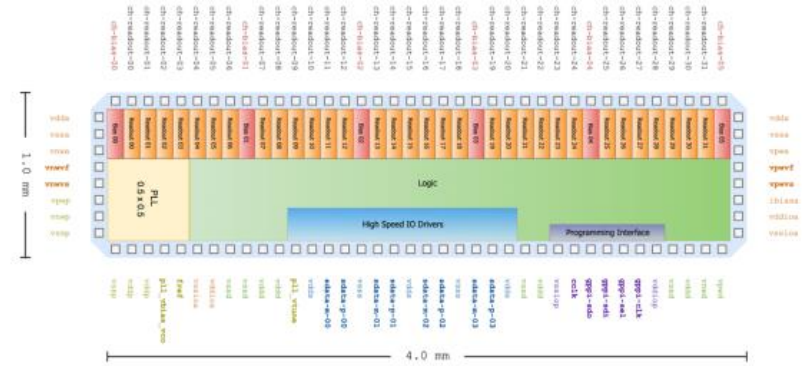
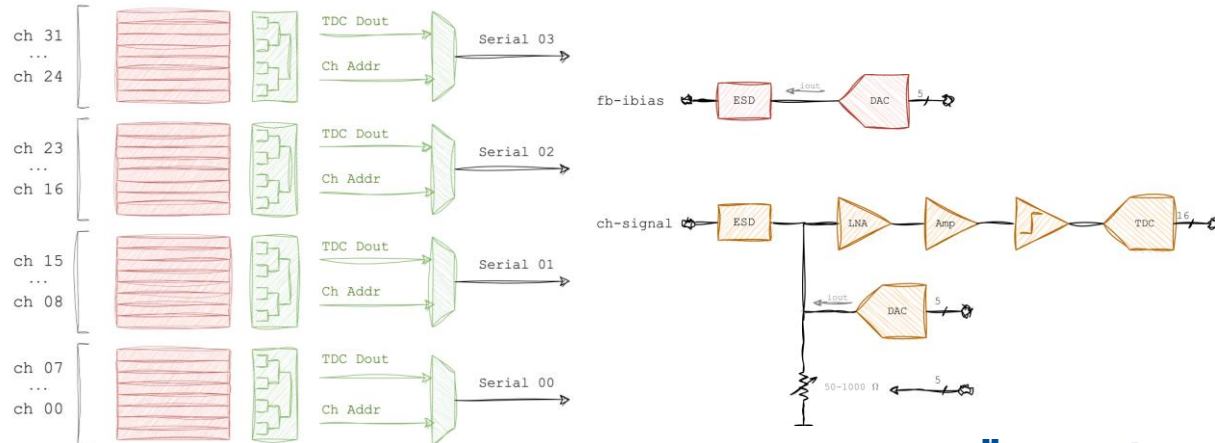


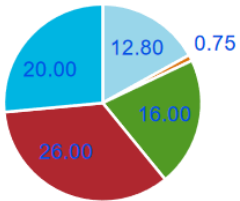
Figure 1. High-Level Floorplan of SUNROCK ASIC



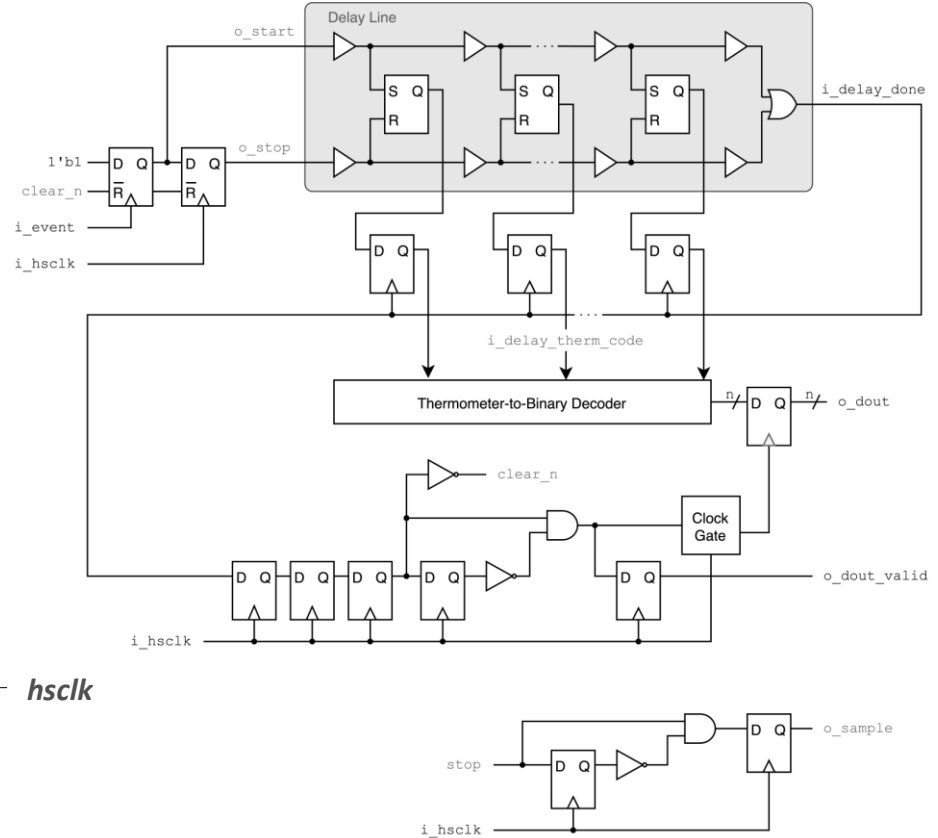
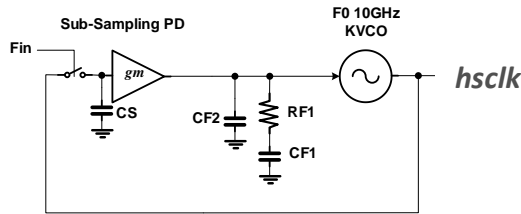
# SUNROCK TDC Architecture

- Fine TDC design essentially identical to CryoTDC v1.
- Coarse counter is clocked by *hsclock*
- *hsclock* (10.0 GHz) is produced on-chip by a novel cryogenic sampling PLL with ~10fs rms jitter.

Power [mW]

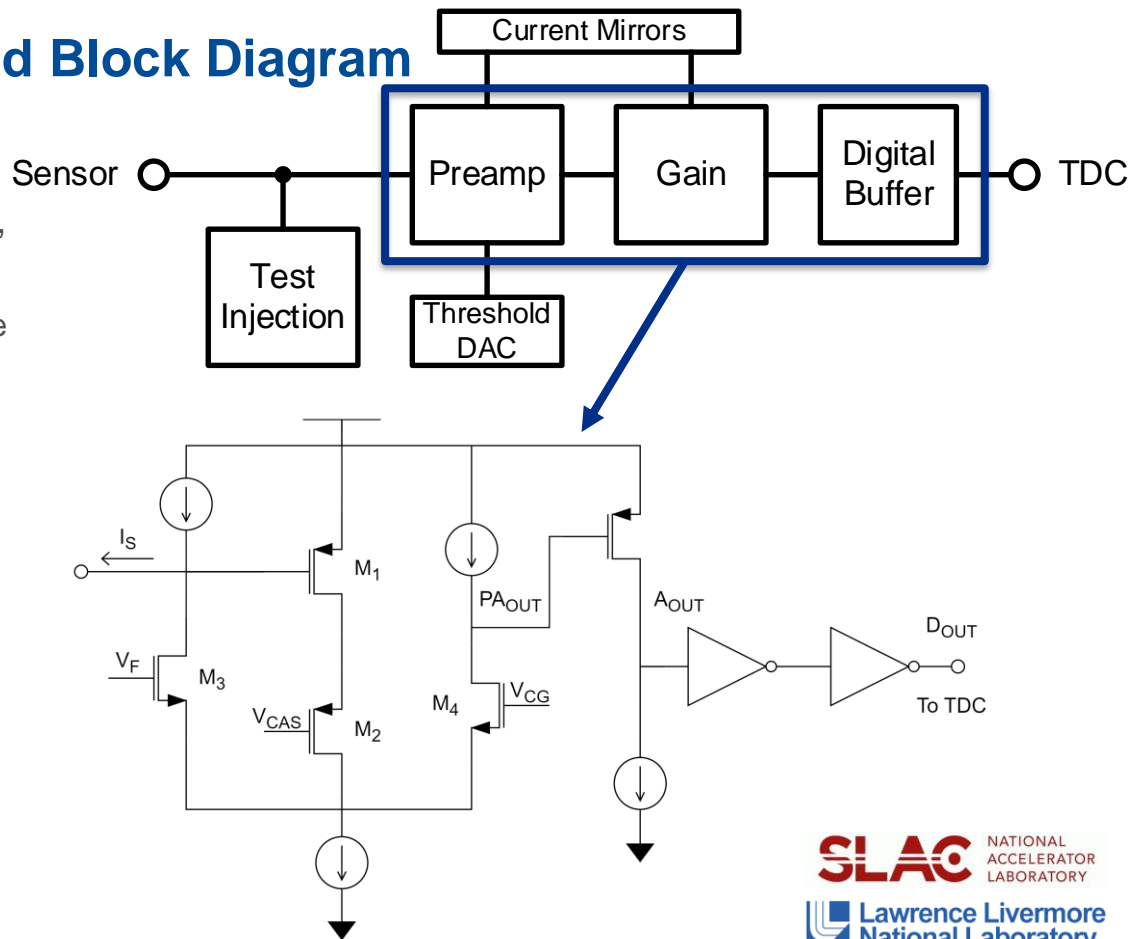


- Readout Channels
- Digital Power
- PLL Power
- Bias Channels
- SerDes Lane



# Accelerate 3D LGAD, Frontend Block Diagram

- There are 6 pieces to the front end
- The signal path consists of a preamplifier, additional gain, and a digital buffer
  - The signal path uses abundant gain in place of a specialized comparator
- Support circuitry includes current mirrors, a DAC for setting the threshold, and charge injection for testing
- The circuit is based on 'A transimpedance amplifier using a novel current mode feedback loop'<sup>1</sup>
- Operating in geiger mode, feedback transistor turned off on hit
- Time over threshold used to access amplitude information





# Accelerate 3D LGAD, Pixel Floorplan

Decoupling Caps

- The front end uses about 40 % of the 50  $\mu\text{m}$  pixel
- Top and bottom will abut with other front ends
- Inside a deep n well with n well contacts all around
- Substrate contacts on east and west sides
- Adjacent front ends will share deep n well

Input Mirror

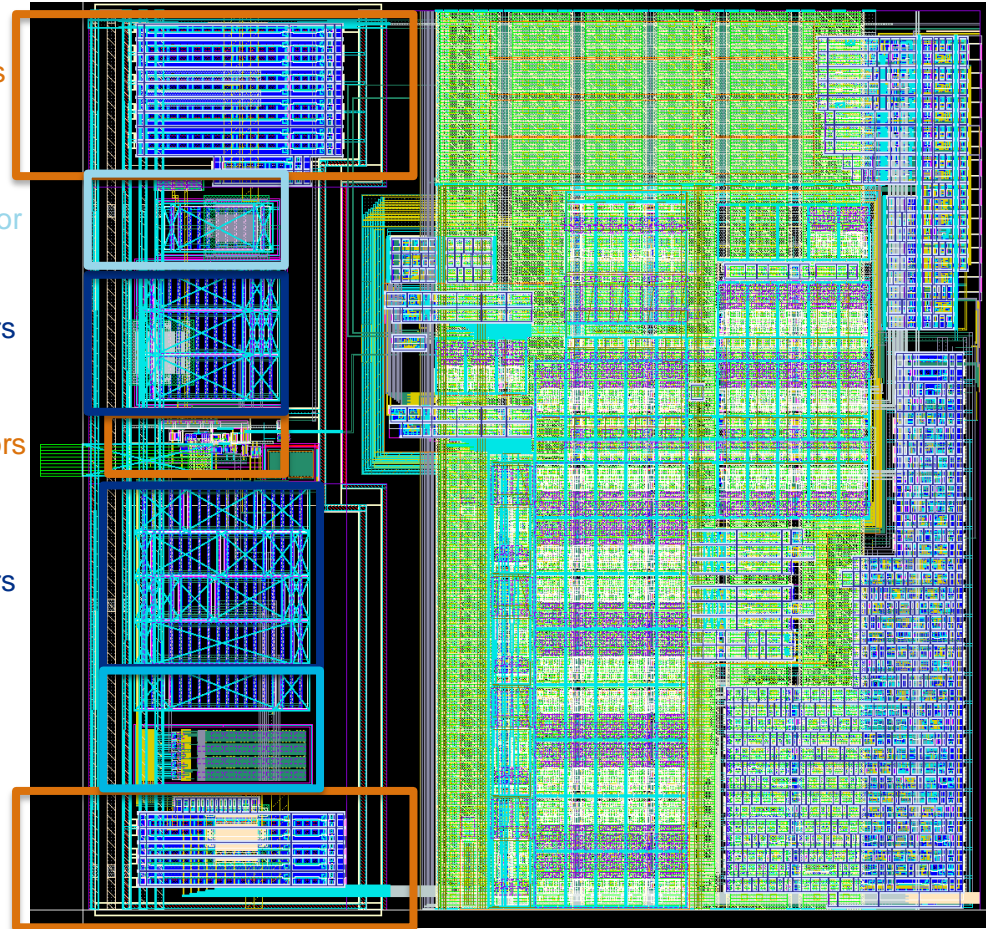
Mirror Resistors

Transistors

Mirror Resistors

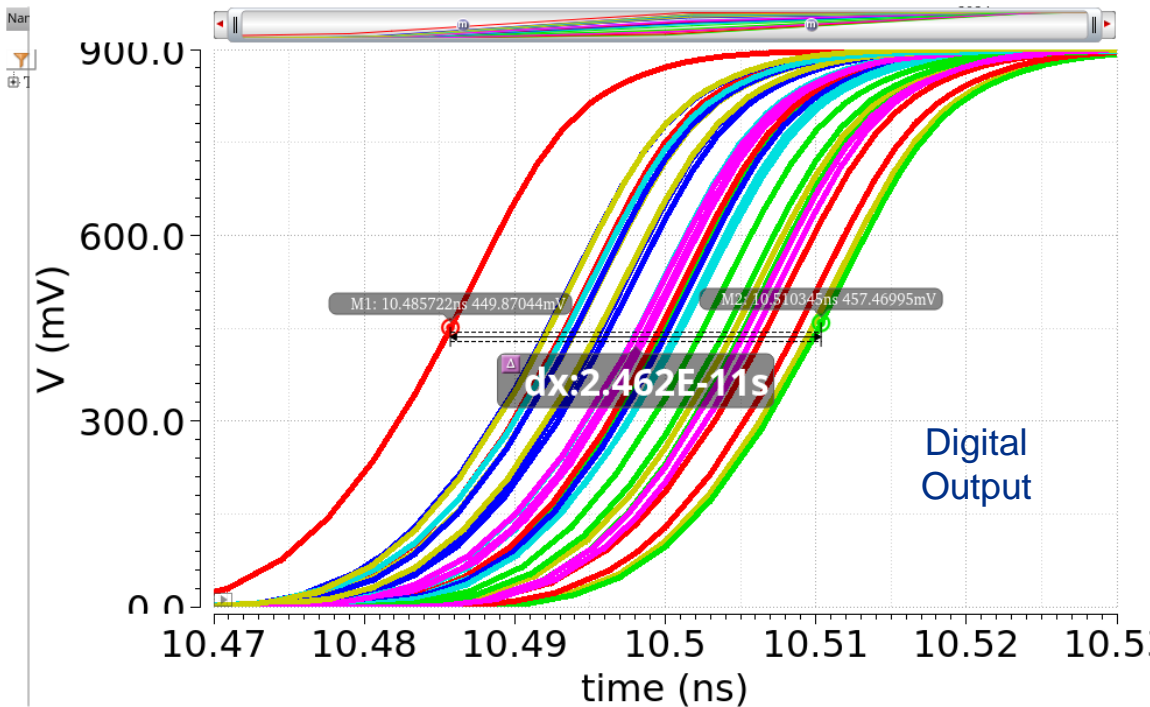
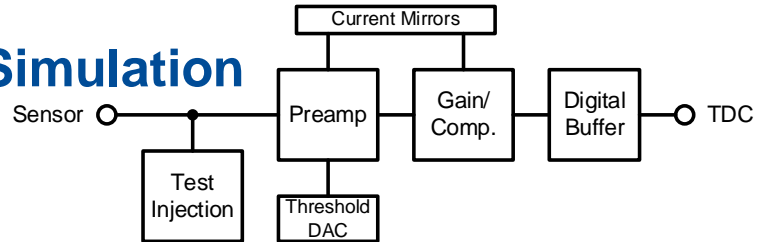
DAC

Decoupling Caps

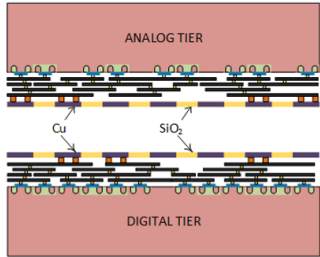


# Accelerate 3D LGAD, Time of Arrival Jitter Simulation

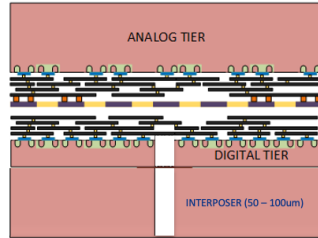
- Filled RCC PEX
- Nominal PVT
- Minimum input charge, 1.3 fC
- Conservative accuracy
- Noise to 30 GHz, 30 runs
- No noise from LGAD
- Standard deviation of the times the output crosses 0.45 V is 5.7 ps
- Specification is 10 ps



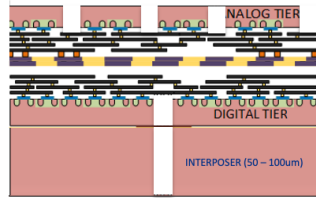
# Establishing Chicago 3D Chips Codesign Community C 3D C<sup>3</sup>



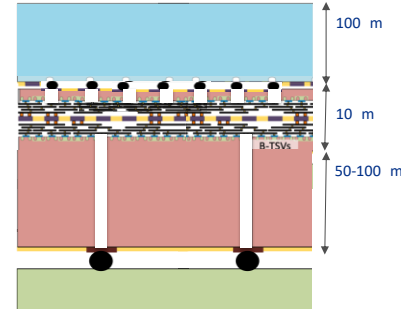
a. Face-2-Face wafer bonding



b. B-TSV insertion and bond to TSV interposer wafer



c. Thinned down top side and B-TSV insertion



3D sensor system

Fermilab,  
Oak Ridge,  
UMN,  
ASU,  
Northwestern,  
U.Chicago,  
UIC,  
UIUC,  
Purdue,  
Cornell Tech,  
DESY,  
SLAC

- CREATING A COMMUNITY and RELEVANT PARTNERSHIPS
- Create open source ADK (Assembly Design Kits) and distribute to consortium members. Membership agreement is almost ready
- Fermilab assembles MPW work with (IMEC, MUSE and others)
- Currently have a multi party NDA with more than 80 institutions for HEP chips (IMEC-TSMC-CERN-Fermilab-others)
- 1<sup>st</sup> run: Low cost – same as the cost of silicon; 65 nm; several national labs and university groups have expressed interest and actively working on designs

