4D Tracking workshop 2024

November 7th, 2024

4D Tracking Electronics Developments @ SLAC

Bojan Markovic – TID ID Integrated Circuits, SLAC National Accelerator Laboratory (*markovic@slac.stanford.edu*)
on behalf of SLAC's TID and FPD

SLAC NATIONAL ACCELERATOR LABORATORY | TID TECHNOLOGY INNOVATION DIRECTORATE

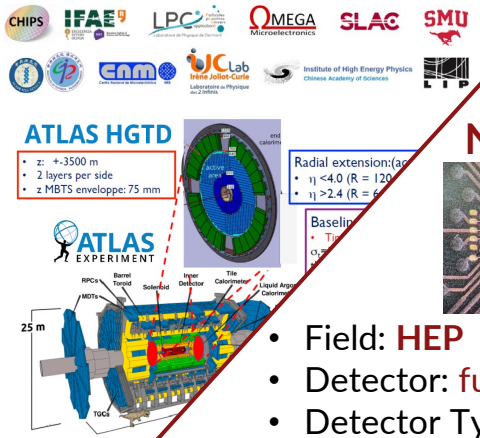
Stanford University | U.S. DEPARTMENT OF ENERGY

Timing ASICs @ SLAC

4D Tracking workshop 2024

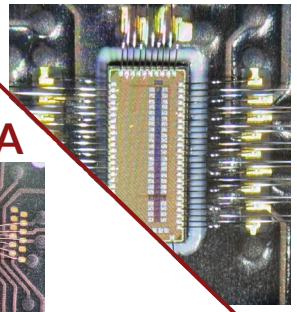
Altiroc

- Field: **HEP**
- Detector: HGTD (Atlas)
- Detector Type: Hybrid
- Sensor: LGAD
- ASIC Technology: 0.13µm
- Time Resolution: **20ps**
- Pixel size: 1.3x1.3 mm²
- Phase: pre-production

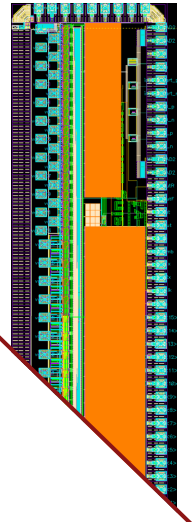


28nm 4D Tracking ASICs

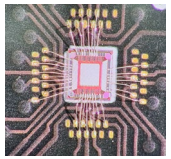
- Field: **HEP**
- Detector: future 4D tracking
- Detector Type: Hybrid
- Sensor: LGAD
- ASIC Technology: 28nm
- Time Resolution: **6.25ps**
- Pixel size: 50x50 & 100x100 µm²
- Phase: R&D



Fermilab



NAPA



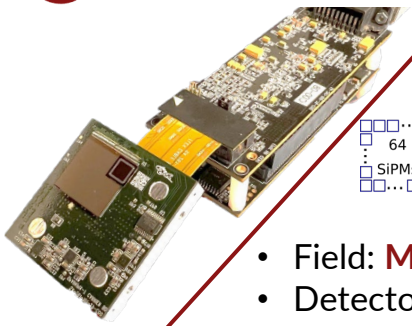
- Field: **HEP**
- Detector: future e+e- Tracker/Cal.
- Detector Type: Monolithic
- Sensor: MAPS
- ASIC Technology: 65nm imaging
- Time Resolution: ~1ns / **20ps**
- Pixel size: 25×25 µm²
- Phase: R&D

HEP

SparkPix-T

- Field: **Photon Science**
- Det.: Tixel (TMO @ LCLS-II)
- Detector Type: Hybrid
- Sensor: Thin Si PAD / LGAD
- ASIC Technology: 0.13µm
- Time Resolution: **100ps**
- Pixel size: 100x100 µm²
- Phase: Final R&D → construc.

LCLS Linac Coherent Light Source

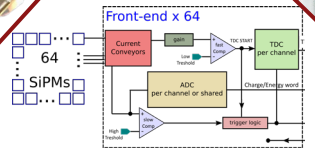


ToF LiDAR (CRADA)

- Field: **Automotive**
- Detector: digital LiDAR
- Detector Type: Monolithic
- Sensor: SPAD
- ASIC Technology: 0.13µm HV
- Time Resolution: **500ps**
- Pixel size: 400x400 µm²
- Phase: products sold by Ouster

OUSTER

SiPM FE



- Field: **Medicine**
- Detector: ToF PET
- Detector Type: Hybrid
- Sensor: SiPM
- ASIC Technology: 0.13µm
- Time Resolution: **10ps**
- Channel size: 1200x250µm²
- Phase: R&D

Politecnico di Bari

Stanford MEDICINE

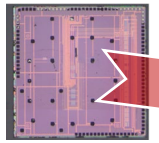
Other Fields

ATLAS HGTD: ALTIROC ASIC (130nm)

4D Tracking workshop 2024

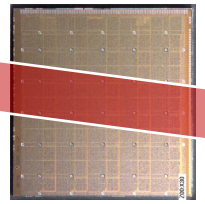
ALTIROC timeline:

Altiroc0 (2016)

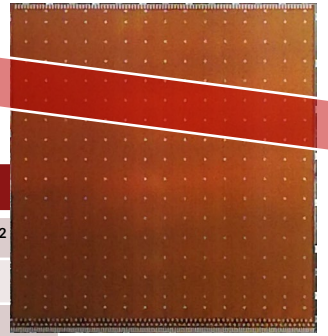


*ASICs not in scale

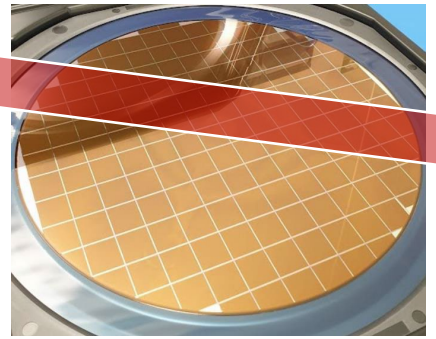
Altiroc1 (2018)



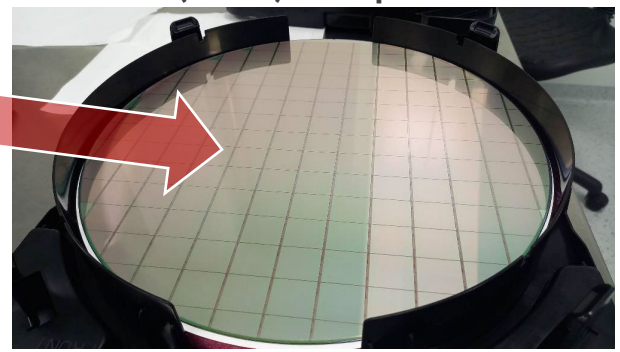
Altiroc2 (2021)



Altiroc3 (2023)



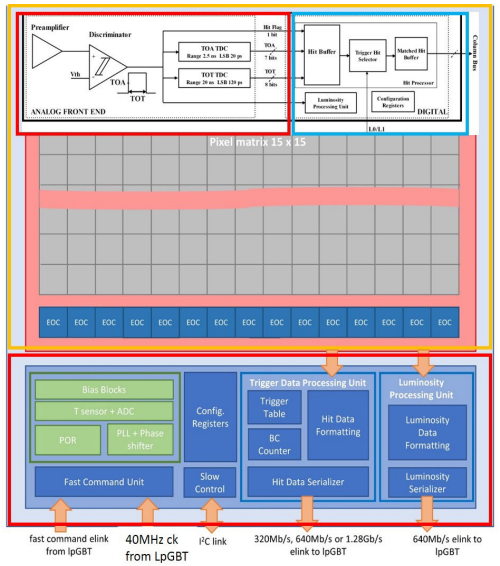
Altiroc-A (2024): Pre-production



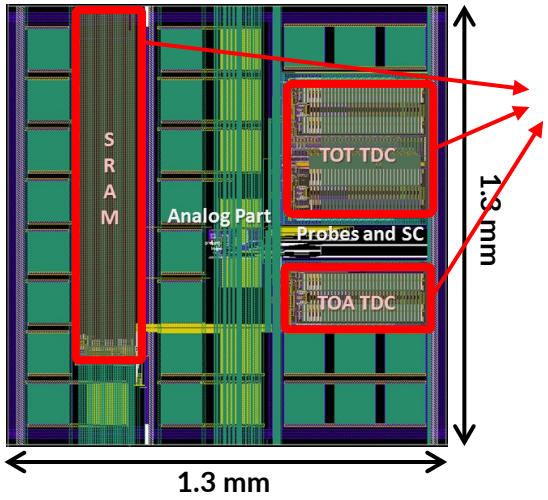
ALTIROC Requirements		
Number of pixels / pixel size:		225 / 1.3x1.3 mm^2
Minimum charge		2 fC
Charge dynamic		up to 100 fC
Noise		< 0.5 fC or 3 ke–
Crosstalk		< 2 %
Power consumption		< 1.2 W (4.5 mW / ch)
Timing precision per hit	10fC (start of lifetime)	35 ps
	4fC (end of operation)	70 ps
TOA TDC*	Resolution	20 ps
	Measurement Range	2.5 ns (7 bit)
TOT TDC*	Resolution	40 ps
	Measurement Range	20 ns (9 bit)
Radiation tolerance	TID	2 MGy
	NIEL	2.5 10^{15} n_{eq}/cm^2
	SEE	10^{15} n_{eq}/cm^2
	SEU rate	< 5 % per hour

*SLAC design

ALTIROC Architecture:



ALTIROC1 Pixel Layout:



SLAC contribution:

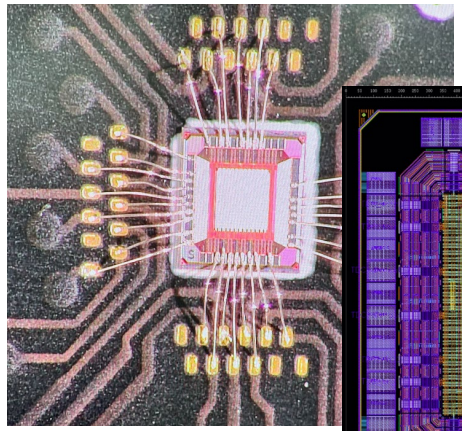
- TOA TDC
- TOT TDC
- Hit buffer (SRAM)

TJ 65nm imaging process work

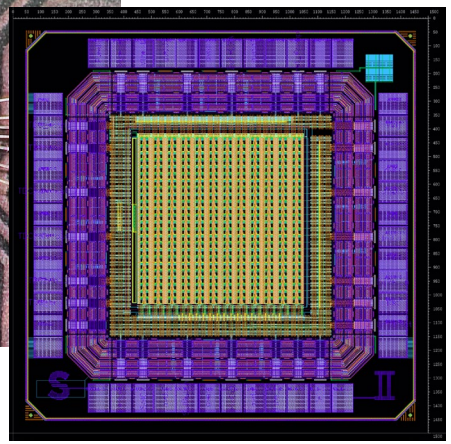
NAPA: **NA**nosecond **P**ixel for large **A**rea sensors:

- Goal: achieve low-power, large-area, ultra-low-mass detector with ~ns timing
- Long term application: Trackers/ Calorimeters in future e+e- colliders
- Designed in Tower Semiconductor 65 nm imaging technology, capitalizing on the CERN WP1.2 efforts over a decade of sensor optimization

NAPA_p1

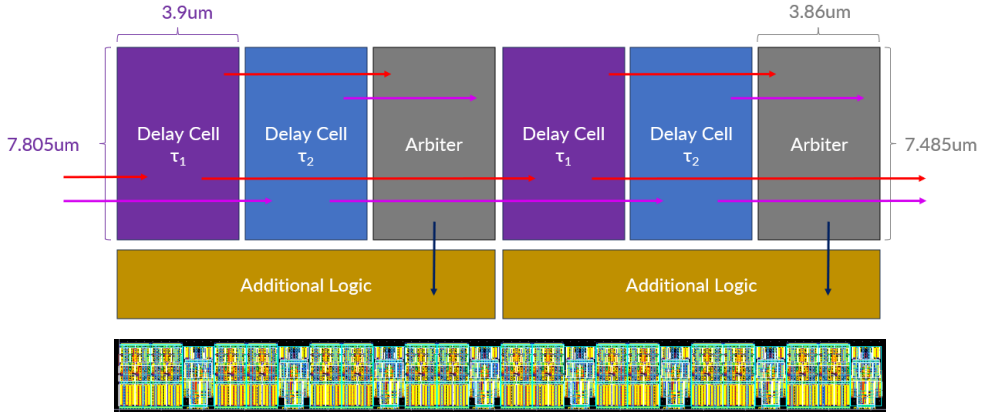


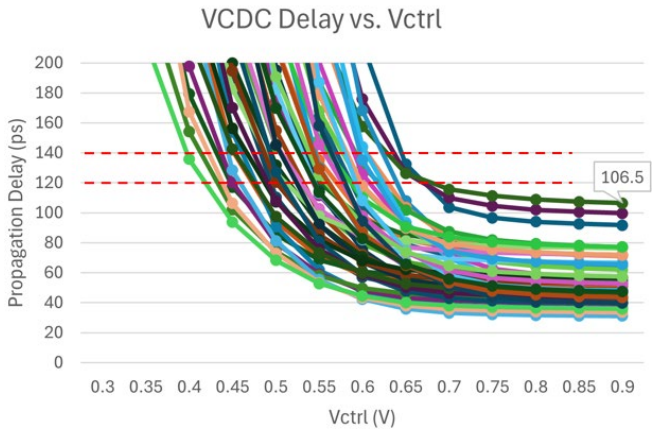
Layout of NAPA_p2

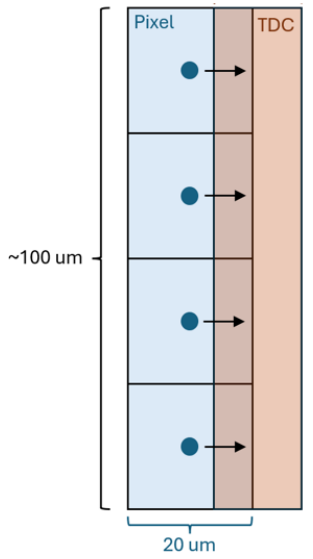


Exploring the possibility of incorporating a 20ps TDC:

- Work by Megan Zeng, Sanford University PhD. student (HEPIC summer internship)
- Design of the TDC core complete
- Oscillator test structure included in the NAPA_p2 submission



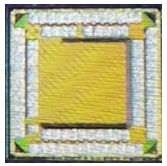


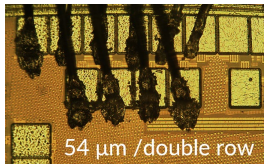


Designs in **28nm**

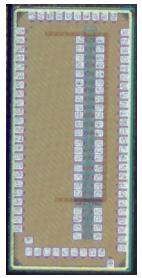
DOE HEP Detector R&D program

v1 (submitted Jan. 2023) - **wire-bounding issues**

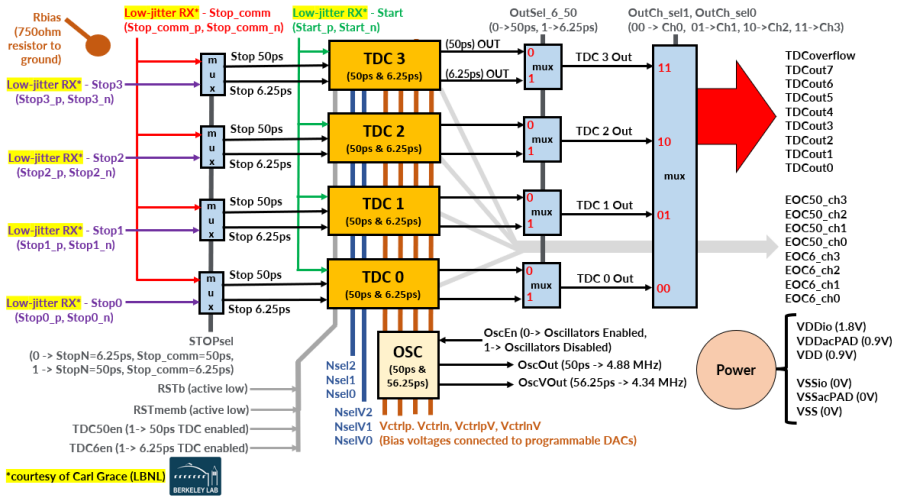




v2 (submitted Jan. 2024, received Jun. 2024) – **testbench characterized**



28nm TDC ASIC: 4 channels, each with 50ps and 6.25ps sections



Further efforts (Victor Turbiner, Stanford U. PhD. student):

- delay line devices for CFD implementation
- clustering algorithms

DOE Accelerate Innovations in Emerging Technologies

3D Integrated Sensing Solutions – SLAC, FNAL, LLNL

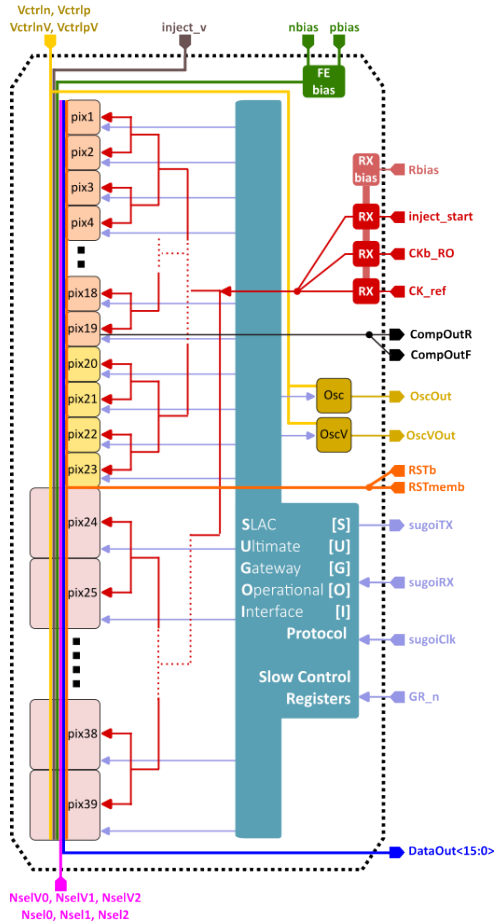
SLAC Fermilab Lawrence Livermore National Laboratory

Parallel effort to the development and fabrication of LGADs on 12” wafers in partnership with Tower Semiconductor

The first LGAD readout prototype (1x3mm^2) submitted in Aug., testing to start in Dec. 2024.

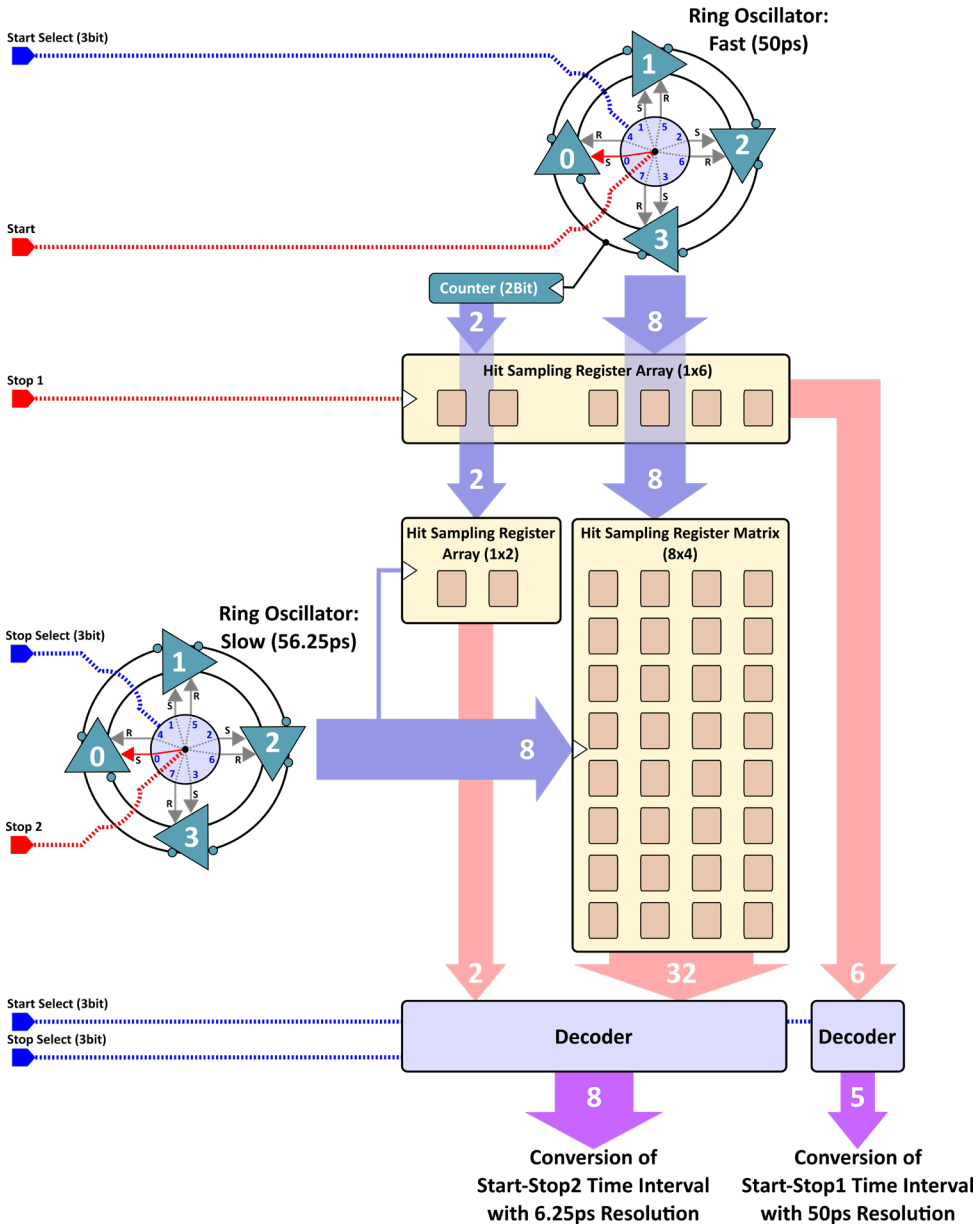
- Linear pixel array (39 pixels); 2 variants of 50µm and 1 variant of 100µm size pixels;
- Pixels include analog frontend and TDC for TOA and TOT;
- Sparsified readout scheme.

Next summer, we will tape-out a MPW run (5x6mm^2) with 50x50 100µm and/or 100x100 50µm pixel array.



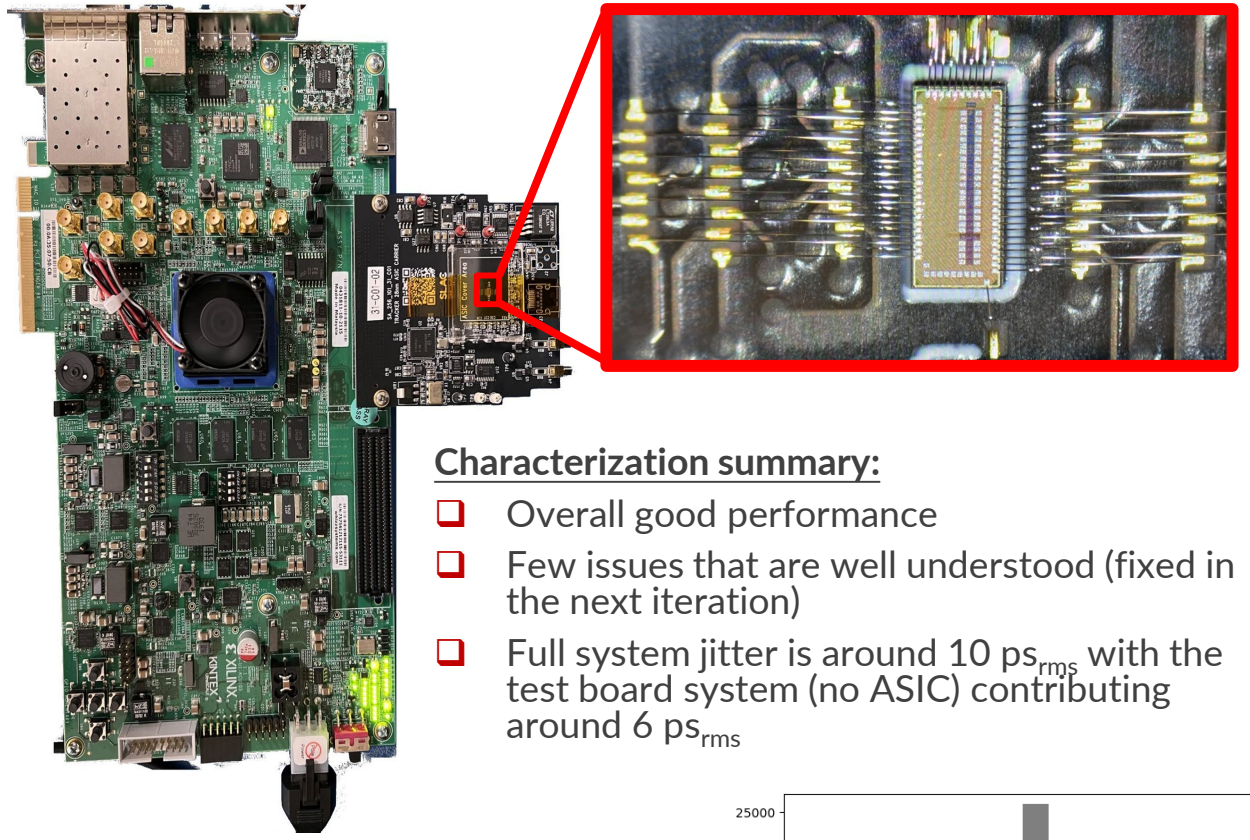
28nm TDC: Architecture

- **2D Vernier Architecture:**
  - Fast Ring Oscillator with 50ps propagation delay cells;
  - Slow Ring Oscillator with 56.25ps propagation delay cells;
- START + two STOP signal for simultaneous time-of-arrival (TOA) and time-over-threshold (TOT) measurements;
- Start-Stop1 - Coarse time resolution (TOT): 50ps;
- Start-Stop2 - Fine time resolution (TOA): 56.25ps - 50ps = 6.25ps;
- **Sliding scale technique for improvement of conversion linearity:**
  - Both ring oscillators have programable starting conditions via delay cell set/reset function;
  - Starting conditions randomly selected each measurement cycle and corresponding values subtracted from the conversion result;
  - Same time intervals converted with different parts/bins of the TDC conversion characteristics;
  - Sliding scale transforms the non-linearities into stochastic variable thus effectively improving the conversion linearity at the expense of worsening single-shoot precision.



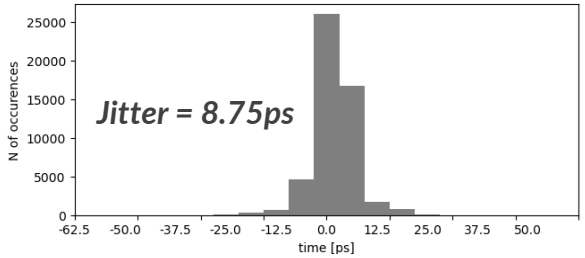
28nm TDC: Characterization

TDC prototype ASIC test setup:

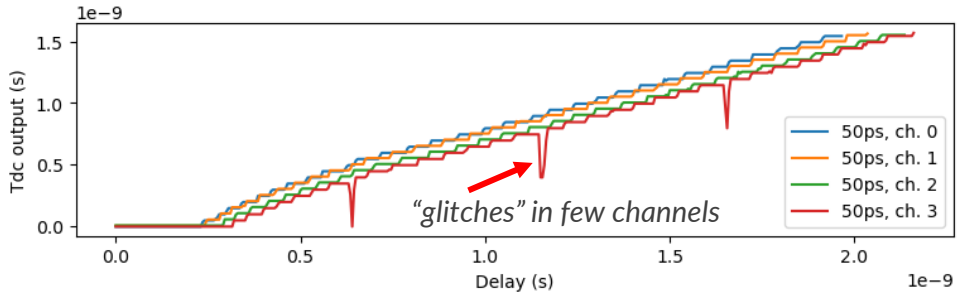


Characterization summary:

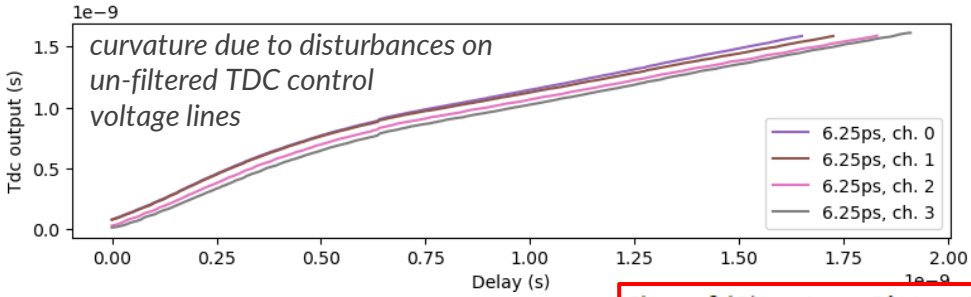
- Overall good performance
- Few issues that are well understood (fixed in the next iteration)
- Full system jitter is around 10 ps_{rms} with the test board system (no ASIC) contributing around 6 ps_{rms}



50ps (TOT) TDC Output VS programmable delay:

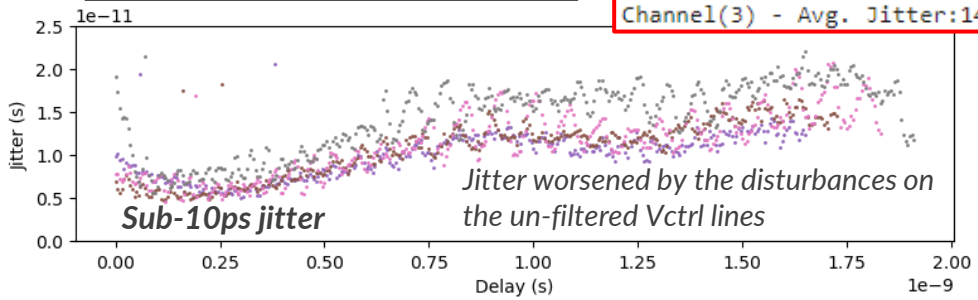


6.25ps (TOA) TDC Output VS programmable delay:




```
Channel(0) - Avg. Jitter:10.18ps
Channel(1) - Avg. Jitter:10.75ps
Channel(2) - Avg. Jitter:11.68ps
Channel(3) - Avg. Jitter:14.47ps
```

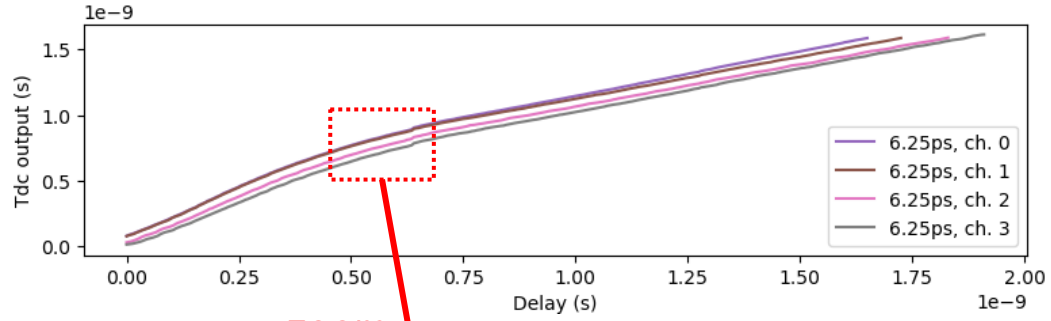
Jitter VS programmable delay:



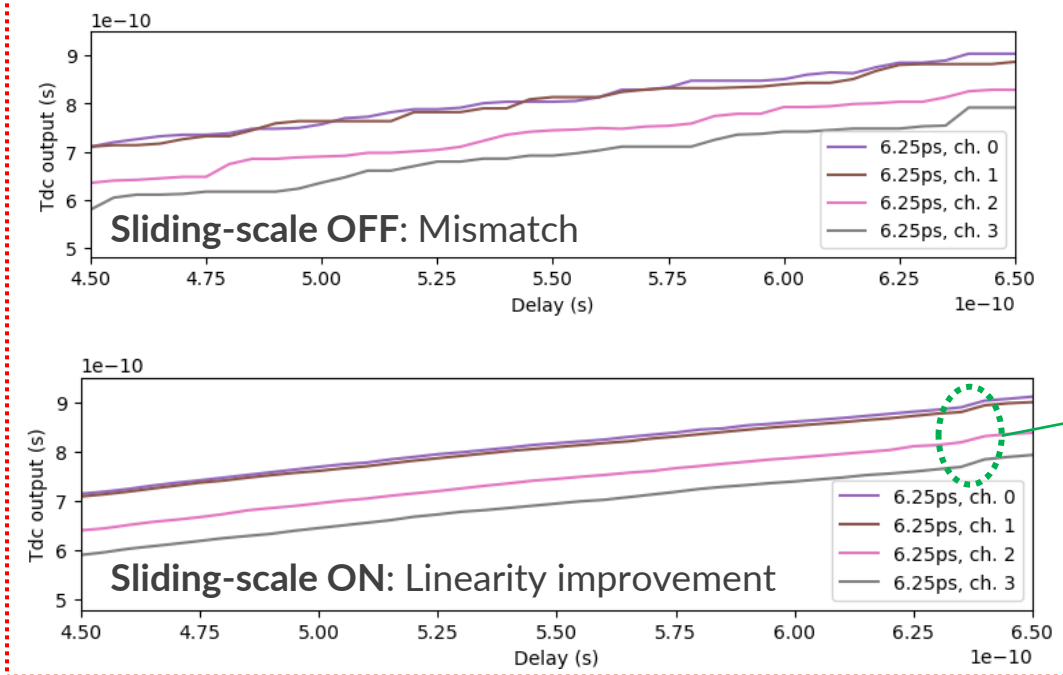
28nm TDC: Sliding-Scale Linearity Improvement

4D Tracking workshop 2024

6.25ps (TOA) TDC Output VS programmable delay:

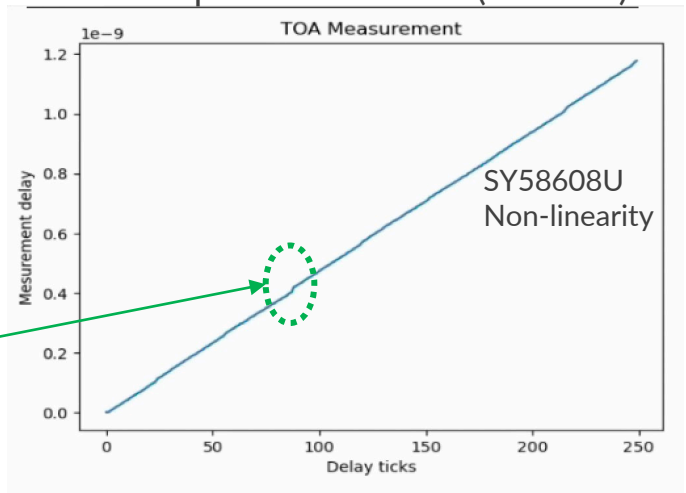


zoom



- Achieving sub-10ps resolution in all PVT conditions requires Vernier architecture (LSB given by the difference of propagation delays) that suffers heavily from mismatch (especially true for implementations that target small pixel sizes) resulting in significant non-linearities of the TDC characteristics.
- The developed TDC implement the sliding-scale technique [1,2] for linearity improvement to mitigate the weakness of the Vernier approach.

Oscilloscope measurement (no ASIC):



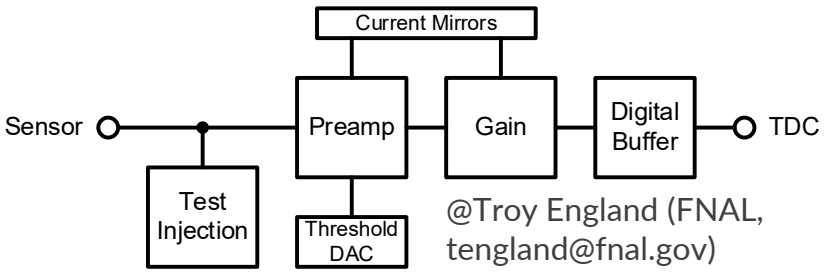
[1] C. Cottini, **E. Gatti**, and V. Svelto, "A new method for analog to digital conversion," Nucl. Instr. Meth., vol. 24, p. 241, Aug. 1963.
[2] **E. Gatti**, P. F. Manfredi, and D. Marino, "Analysis and characterization of cyclic-scale compensated analog-to-digital converters," Nucl. Instrum. Methods, vol. 165, no. 2, pp. 225–230, Oct. 1979.

3D Integrated Sensing Solutions: FE ASIC

4D Tracking workshop 2024

Frontend Specification	Value
Total Power Density	$1\,W/cm^2$
Power 50x50 µm^2	$25\,\mu W$
Time of Arrival (ToA) Jitter (ASIC)	$\mathbf{10\,ps_{rms}}$
Min Signal for ToA Jitter	$1.3\,fC$
Max Signal	$13\,fC$
Dynamic Range	$10-20$
Repetition Rate at each Pixel	$100\,kHz$
LGAD Input Cap. Approx.	$11.52\,aF/\mu m^2$

Analog Front-End:

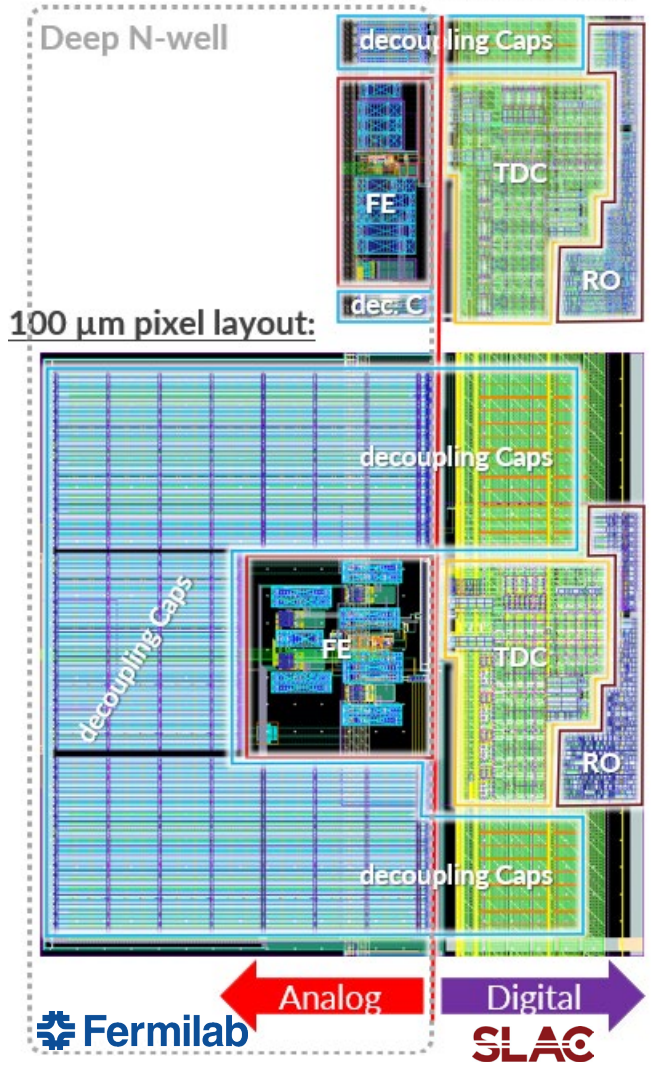


@Troy England (FNAL, tengland@fnal.gov)

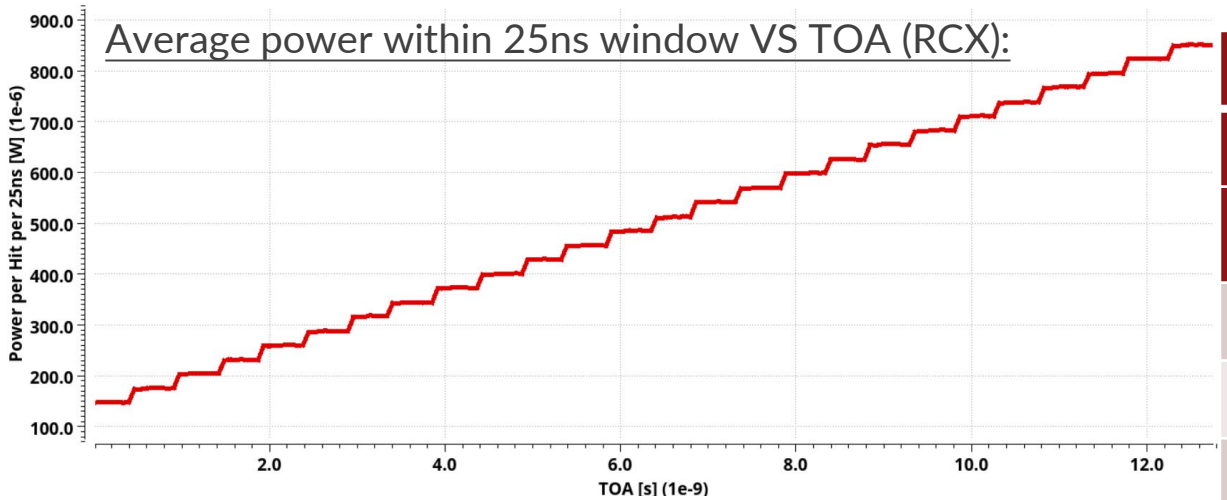
1st prototype submitted Aug. 2024, characterization to start Dec. 2024

	TDC metrics
Technology	**28nm**
Timing resolution	**6.25ps (TOA) / 50ps (TOT)**
Time depth	~~1.6ns (8bit / 5bit)~~ **12.8ns (11bit / 8bit)** easily extendable by simple addition of bits to the counter
TDC area	**26µm x 40.5µm** (1.7µm x 13.3µm per additional bit)
Power consumption	(average, 25ns conversion cycle / bunch crossing)
10% occupancy	~~16µW~~ **51.1µW**
1% occupancy	~~2.5µW~~ **6.2µW**

50 µm pixel layout:



3D Integrated Sensing Solutions: FE ASIC Power



- TDC idle consumption (due to leakage): ~1.2µW
- TDC power consumption depends on time-interval being measured
  - For uniformly distributed time-intervals Ti the average power consumption per Hit in a 25ns measurement window is:

$$P_{\frac{av}{hit}/T_{CK}} = 500\mu W$$

- **Average power consumption:**

$$P_{av} = 1.2\mu W \cdot (1 - Occupancy) + P_{\frac{av}{hit}/T_{CK}} \cdot Occupancy$$

  - **For 10% occupancy: ~ 51.1µW**
  - **For 1% occupancy: ~ 6.2µW**

	Power Consumption (average, 40MHz clock) [µW]							
	50 µm x 50 µm pixel				100 µm x 100 µm pixel			
Occupancy	FE	TDC	*Clk three	Tot.	FE	TDC	*Clk three	Tot.
0%	11.6	1.2	1.2	14	81	1.2	2.4	84.6
1%	11.6	6.2	1.2	19	81	6.2	2.4	89.6
2%	11.6	11.2	1.2	24	81	11.2	2.4	94.6
4%	11.6	21.2	1.2	34	81	21.2	2.4	104.6
6%	11.6	31.1	1.2	43.9	81	31.1	2.4	114.5
8%	11.6	41.1	1.2	53.9	81	41.1	2.4	124.5
10%	11.6	51.1	1.2	63.9	81	51.1	2.4	134.5

*Clock distribution contribution is derived assuming hierarchical tree on a matrix of 256x256 50µm pixels and 128x128 100µm pixels (parasitic extracted sim.)