FCC-ee electronics challenges and requirements

FCC-ee accelerator program

Parameter	Z	WW	H (ZH)	ttbar
beam energy [GeV]	45	80	120	182.5
beam current [mA]	1280	135	26.7	5.0
number bunches/beam	10000	880	248	36
bunch intensity [10^{11}]	2.43	2.91	2.04	2.64
SR energy loss / turn [GeV]	0.0391	0.37	1.869	10.0
total RF voltage 400/800 MHz [GV]	0.120/0	1.0/0	2.08/0	4.0/7.25
long. damping time [turns]	1170	216	64.5	18.5
horizontal beta* [m]	0.1	0.2	0.3	1
vertical beta* [mm]	0.8	1	1	1.6
horizontal geometric emittance [nm]	0.71	2.17	0.64	1.49
vertical geom. emittance [pm]	1.42	4.34	1.29	2.98
horizontal rms IP spot size [μm]	8	21	14	39
vertical rms IP spot size [nm]	34	66	36	69
luminosity per IP [10^{34} $cm^{-2}s^{-1}$]	182	19.4	7.3	1.33
total integrated luminosity / year [ab^{-1}/yr] 4 IPs	87	9.3	3.5	0.65
beam lifetime (rad Bhabha + BS+lattice)	8	18	6	10
	4 years	2 years	3 years	5 years

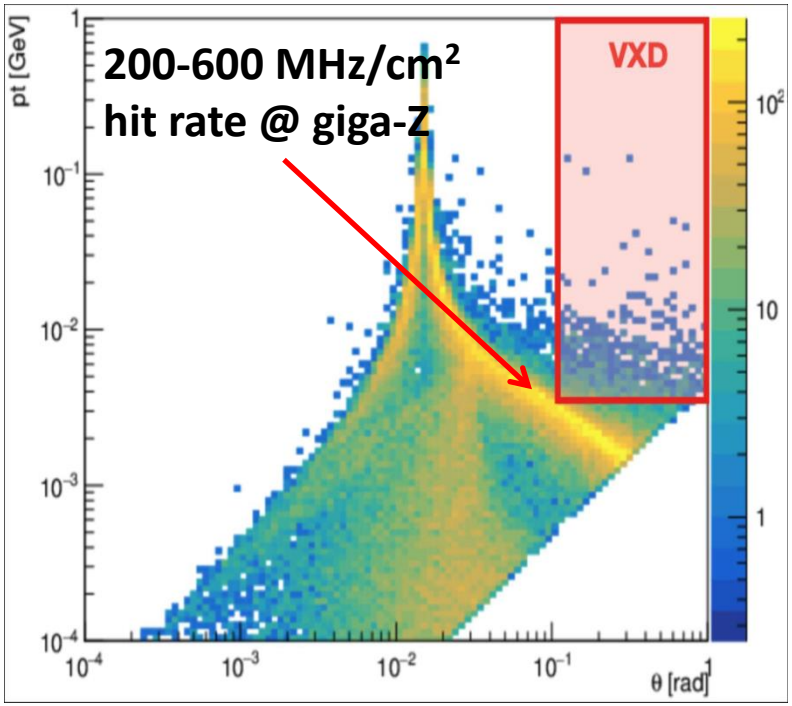
Lumi is the highest during the giga-Z program. However, not every BC contains a Z-boson

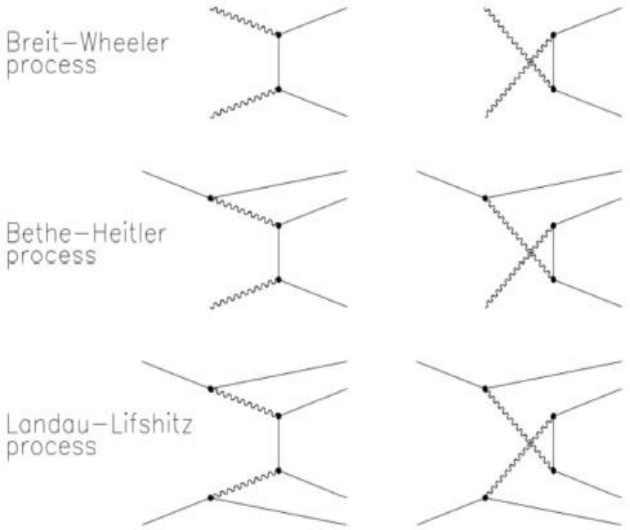
Hard scatter and background rates

- At the Z pole, expected total ee collision/event rate is ~200 kHz. The bunch crossing rate is 50 MHz.
- Incoherent pair production is the main source of beam backgrounds.

Physics process	Rate (kHz)
Z decays	100
$\gamma\gamma \to$ hadrons	30
Bhabha	50
Beam background	20
Total	$\sim$ 200

https://arxiv.org/pdf/2111.04168v1.pdf





See https://indico.cern.ch/event/1307378/contributions/5727164/attachments/2791569/4869322/Bedeschi_Annecy_2024.pdf and
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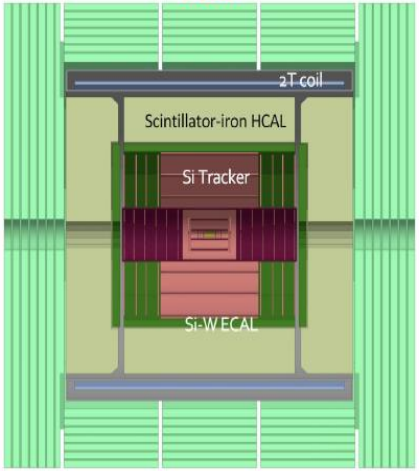
https://indico.cern.ch/event/1298458/contributions/5987291/attachments/2875496/5035607/Silicon%20tracker%20optimisation_Armin%20llg.pdf

Detector concepts

- All the detectors are instrumented with an innermost Si trackers. These are challenging to readout and may require fixed-latency triggerring.
- The innermost layer is subject to the incoherent pair production.

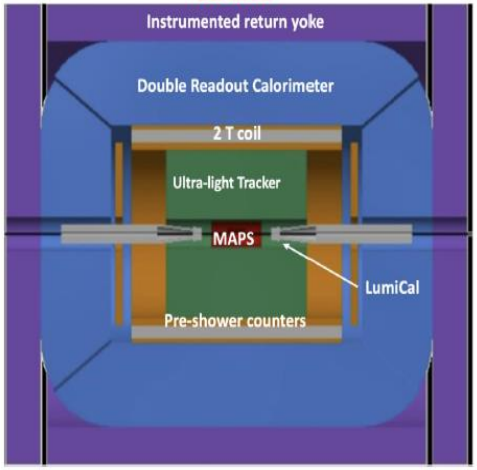
Detector benchmarks

CLD



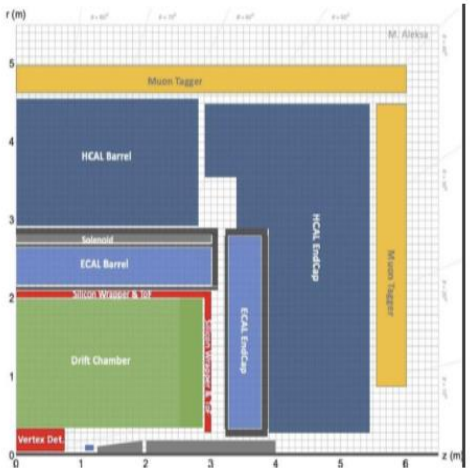
- Full silicon vertex + strip tracker
- CALICE-like 3D-imaging high-granular calorimetry with Si-W for ECAL and Sci-iron for HCAL
- Muon system with RPCs
- Coil outside of calorimeters

IDEA



- Silicon vertex + ultra-light tracker
- Monolithic dual readout calorimeter with Cu-fibers (possibly augmented by dual-readout crystal ECAL)
- Muon system with μ-RWELL
- Coil inside calorimeters

ALLEGRO



- Silicon vertex + ultra-light tracker
- High granularity noble liquid ECAL (LAr or LKr with Pb or W absorbers)
- CALICE-like or TileCal-like HCAL
- Muon system
- Coil outside of ECAL

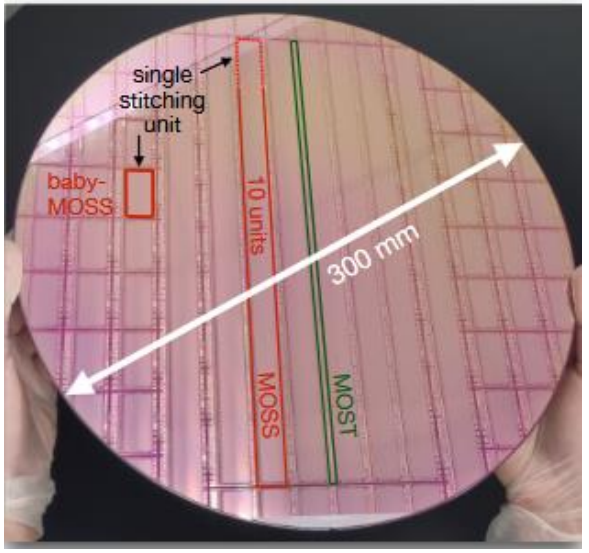
From: https://indico.cern.ch/event/1298458/contributions/5975666/attachments/2874286/5033190/DetectorRequirements_Zhu.pdf

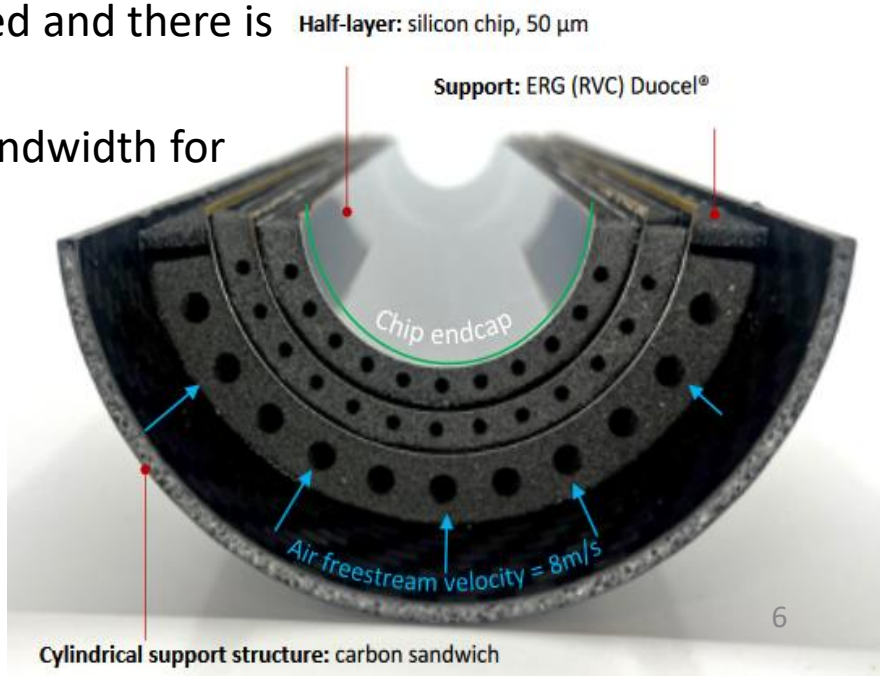
Required tracking performance

- The tracker is required to have micron accuracy of single point resolution.
  - → Small pixels and minimal inert material.
  - → Air-cooled MAPs
- The particle ID can greatly benefit physics capabilities of the detectors (e.g. improve charm jet tagging)
- ToF measurements can be used for the PID.
- Tentatively, the vertex detectors are not capable of accurate timing measurements.
  - Can these be useful for physics or background rejection?
- The low material budget caps the power dissipation due to the need for air-cooling (~200 mW/cm2) for the Si detectors
- An outermost timing layer is not restricted by the power cap.
- The 20 ns bunch crossing rate during the giga-Z does not allow power pulsing/gating.

MAPS for FCCee trackers

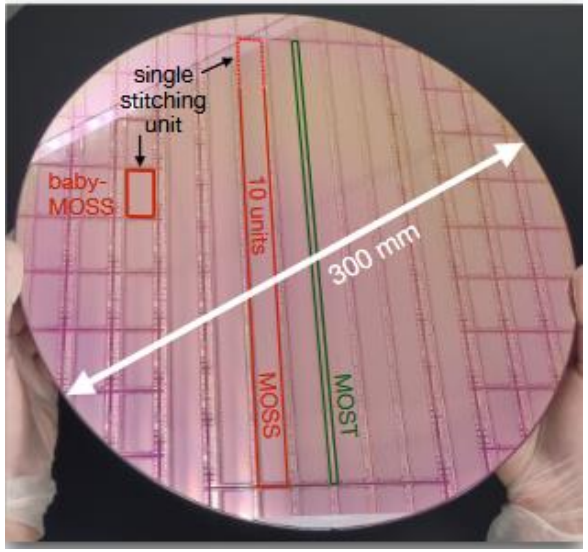
- See https://indico.cern.ch/event/1417976/timetable/
- These sensors are flexible and self-supporting.
- They can be as large as a wafer.
- MOSAIX ASIC uses 65nm CMOS and the fill factor is 93%.
- The power consumption is almost maxed out
- There are long data transmission lines from the pixel matrix to the end-caps periphery.
- The readout of the pixel matrix is optimized and there is no on-chip data processing.
- The chip does not have enough output bandwidth for data taking at FCCee.





Large MAPS challenges

1. Can we have triggerless readout?
   - Frees space on-chip (no buffering)
   - Requires fast data link from the chip to DAQ (e.g. Si-pho fiber to chip)
   - Requires enough power to serialize the data
2. Long and large clock distribution circuit. Is the clock jitter reasonable?
3. Power distribution (IR drops, noise).
4. Will there be enough power budget for timing measurements (TDCs, clock, data movement, etc)?
5. Will we need more on-chip bandwidth to move data to the periphery?
6. Will there be enough off-chip link bandwidth to transmit the extra timing data?
7. Do we need smaller CMOS feature size for FCCee MAPS?
8. Can we use on-chip data processing to reduce the power and on-chip and off-chip bandwidth?



Outlook

- People have started looking at the impact of track timing on the physics capabilities of the experiments.
  - PID for Charm jet tagging.
  - Are there more applications?
- Would we benefit from accurate detector simulations for all the detector concepts?
- Do the vertex detectors benefit from the 4D tracking?
- Is it technically feasible to do 4D tracking with the expected technologies (CMOS/MAPS, fiber-optical data links, etc) ?
  - Clock distribution to-chip and on-chip
  - Power delivery on-chip and to-chip