IC Design Tutorial

HEPIC Summer Week

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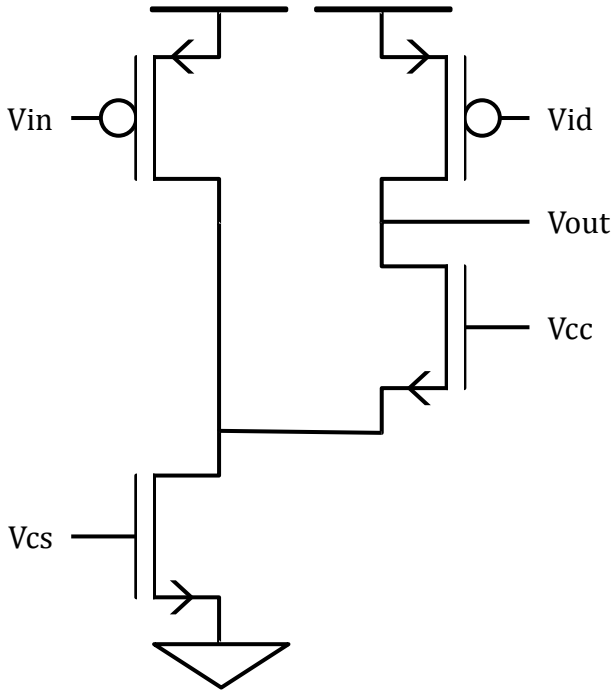
2024

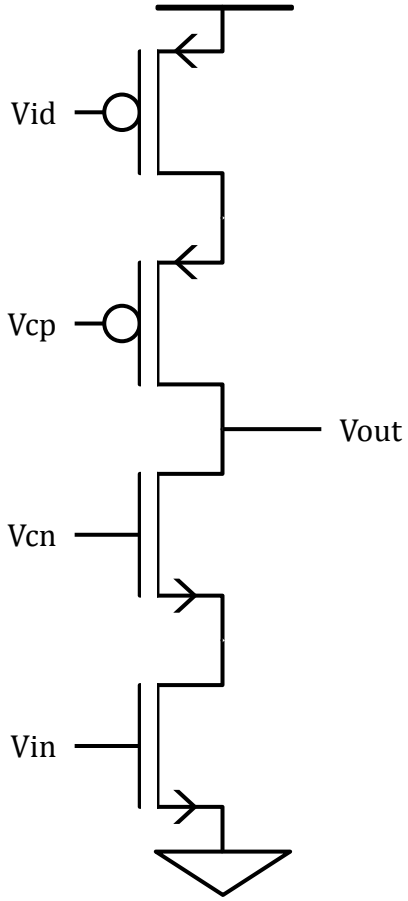
SLAC NATIONAL ACCELERATOR LABORATORY

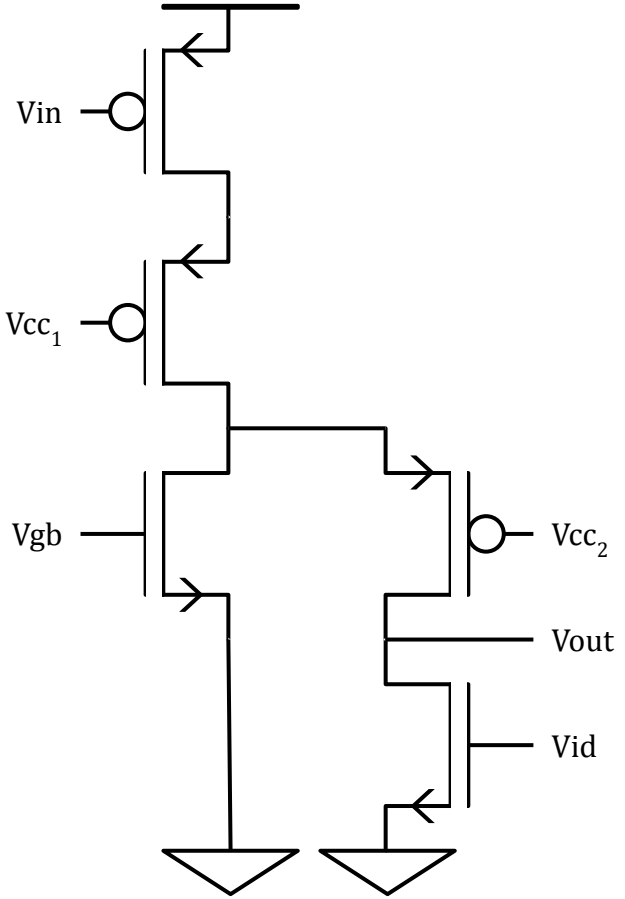
Stanford University | U.S. DEPARTMENT OF ENERGY

The End Goal

Look at these circuits and intuitively understand what they do

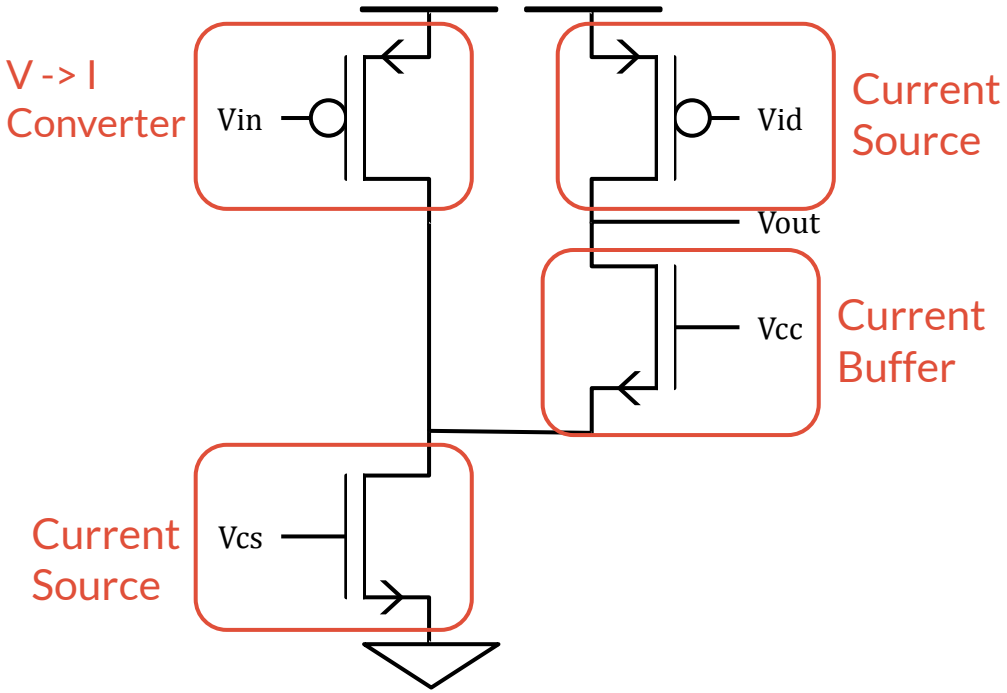


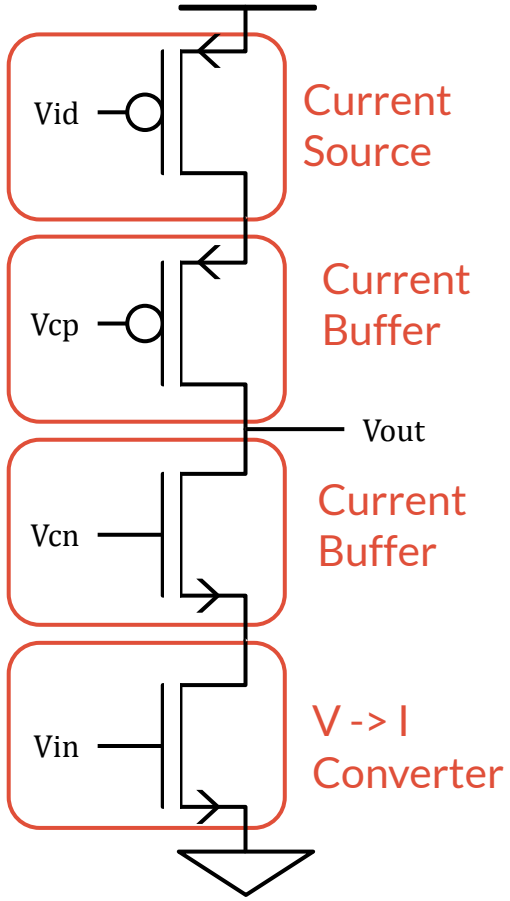


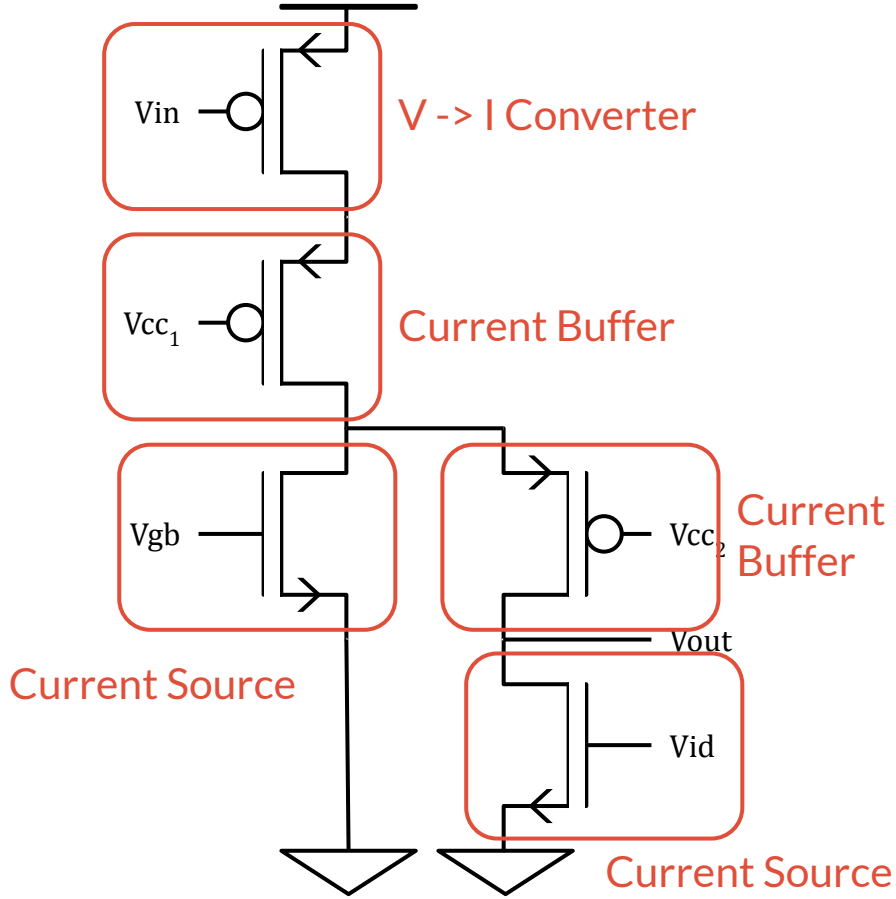


The Approach

Break circuits down into modular blocks







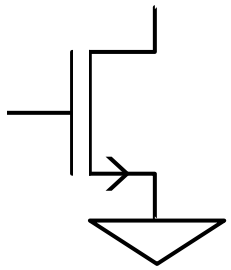
The Steps

1. Small Signal DC Analysis
   a. The three types of building blocks
      i. I → V and V → Converters
      ii. Impedance Transformers
   b. How to quickly solve any circuit with no feedback loops
   c. Designing circuits with building blocks
2. DC Biasing And Sizing Transistors
   a. Device equations and gm/Id
   b. How to size transistors to get a desired gm
   c. Current sources
3. AC Analysis And Feedback
   a. Charge-sensitive amplifiers and diode readouts
   b. The open-loop intrinsic gain stage
   c. Adding capacitive feedback
   d. Working with multi-stage amplifiers

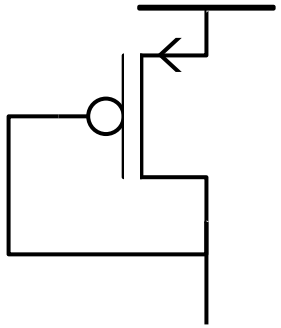
Small Signal DC Analysis

Three types of building blocks

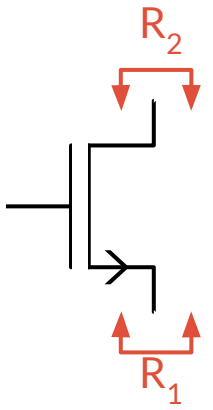
The Three Types of Building Blocks



V → I
Converters

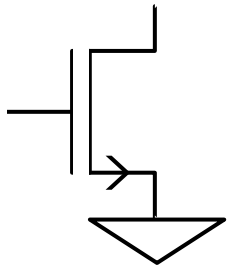


I → V
Converters

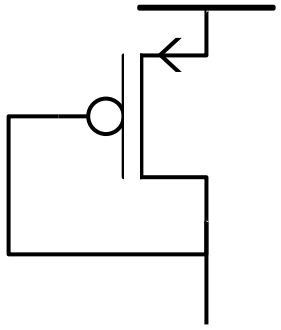


Impedance
Transformers

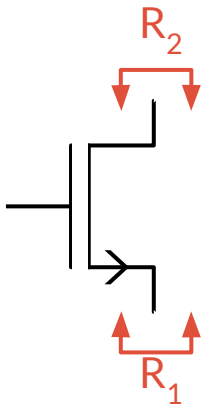
First step: V → I and I → V



V → I
Converters

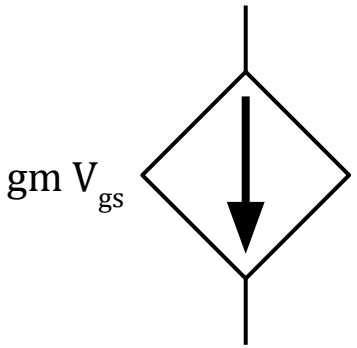


I → V
Converters

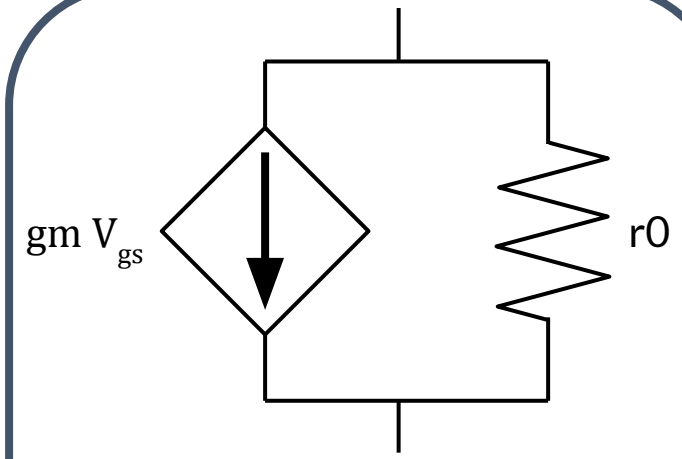


Impedance
Transformers

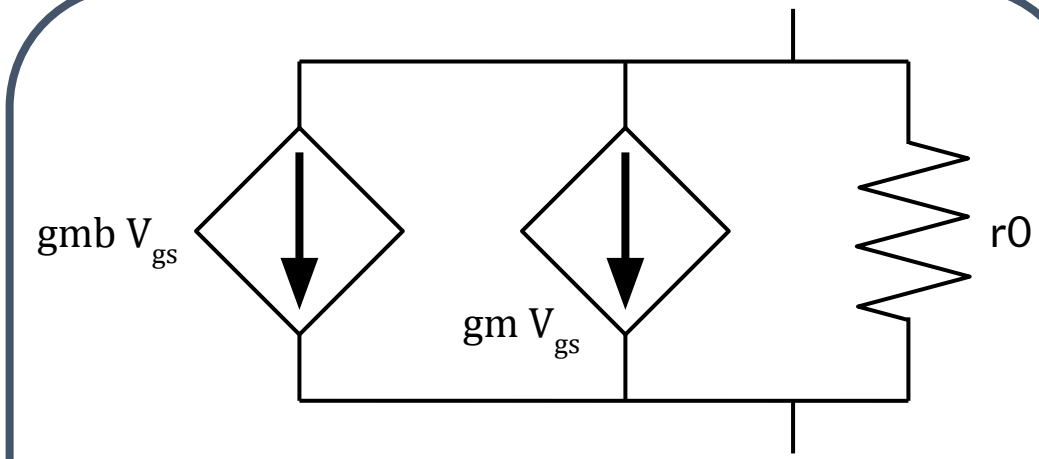
MOSFET Small Signal Models



Ideal Transconductor

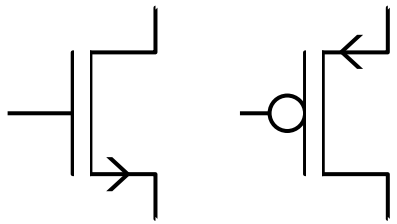


Output Impedance



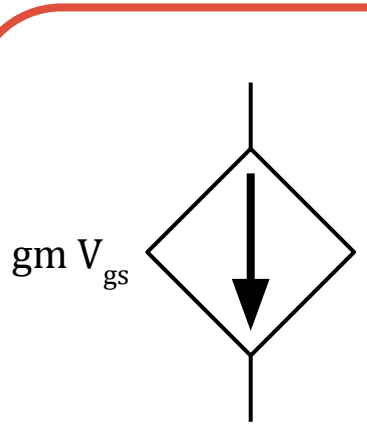
Body Effect

Same model for both:

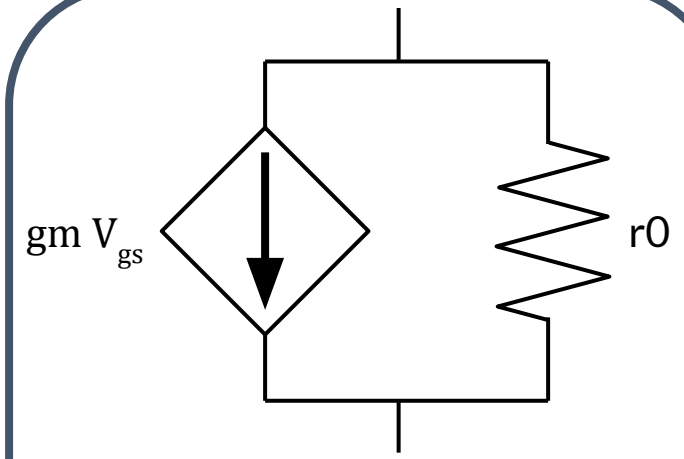


MOSFET Small Signal Models

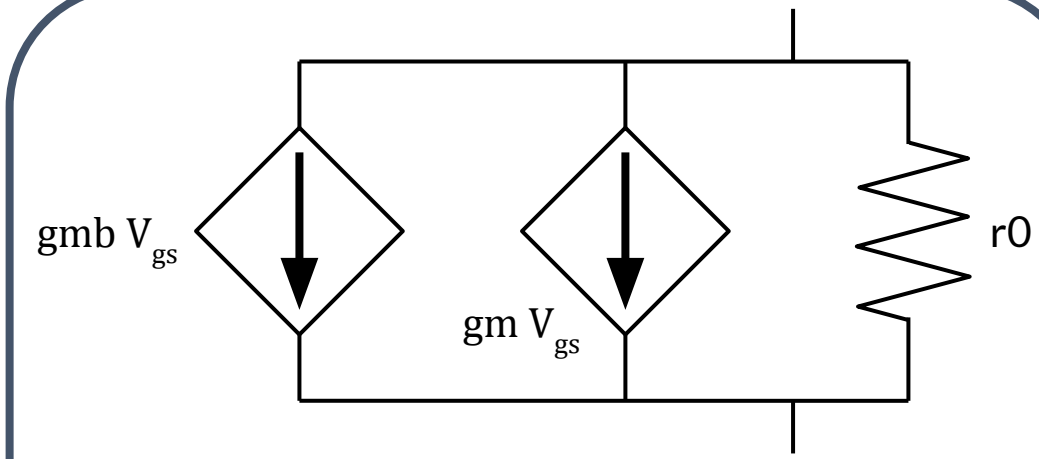
We'll start with ideal transconductor



Ideal Transconductor



Output Impedance



Body Effect

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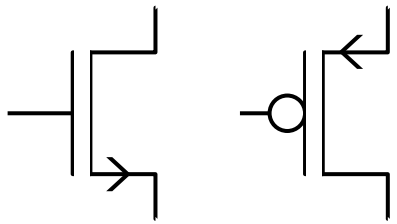
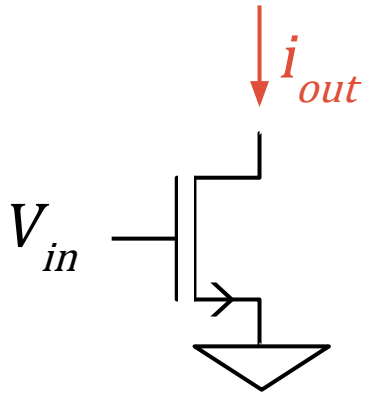
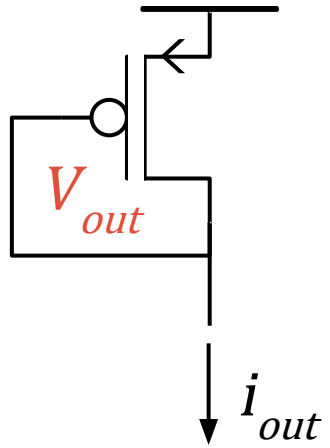


Converting between current and voltage



$$V_s = 0$$

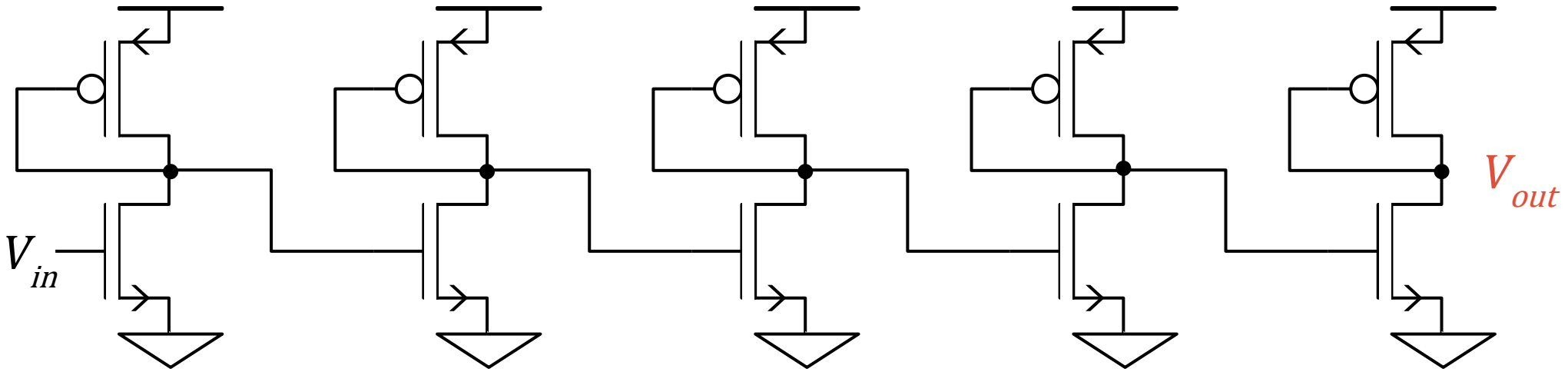
$$i_D = g_m V_{gs} = g_m (V_g - V_s) = g_m V_g$$



$$i_{out} = g_m V_{in}$$

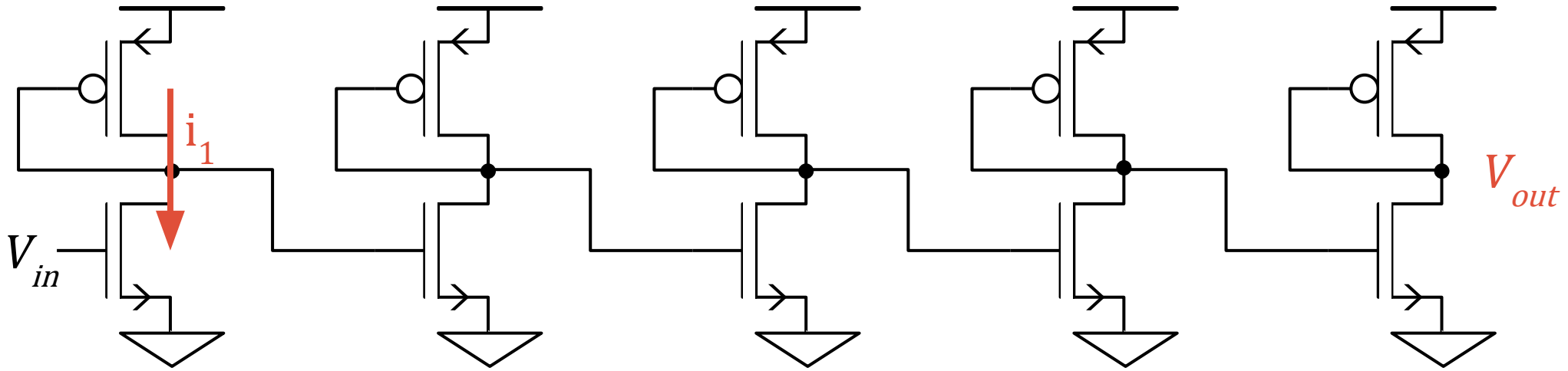
$$V_{out} = i_{in} / g_m$$

Chaining stages together



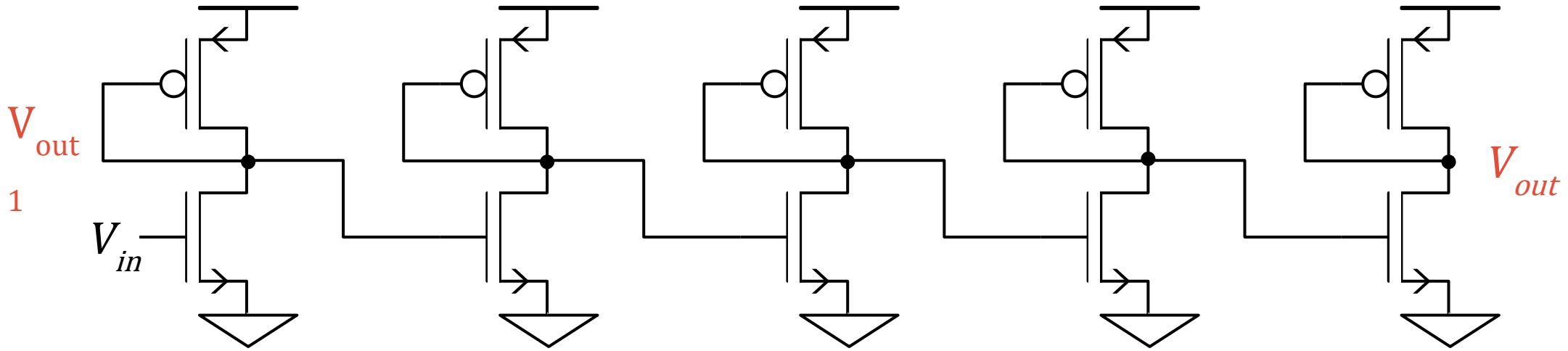
Chaining stages together

$$i_1 = g_{mn1} V_{in}$$



Chaining stages together

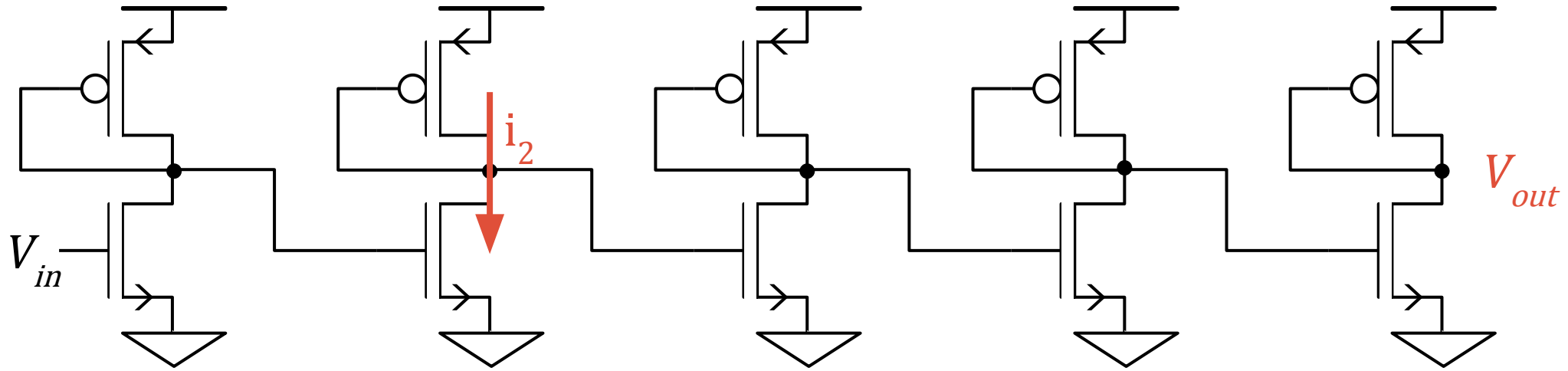
$$i_1 = g_{mn1} V_{in}$$



$$V_{out1} = i_1 / g_{mp1} = \frac{g_{mn1}}{g_{mp1}} V_{in}$$

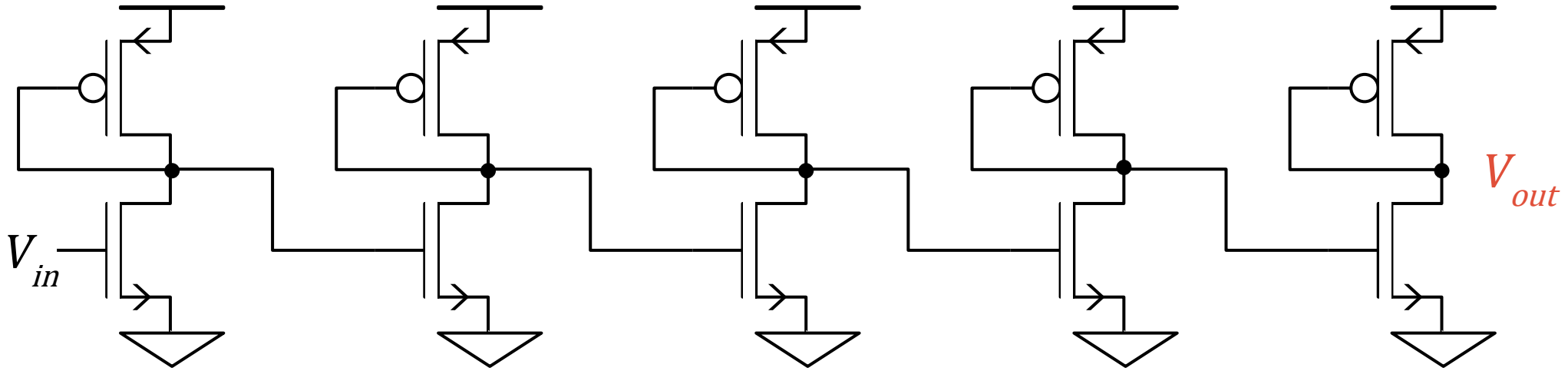
Chaining stages together

$$i_1 = g_{mn1} V_{in} \quad i_2 = g_{mp2} V_{out2} = g_{mp2} \frac{g_{mn1}}{g_{mp1}} V_{in}$$



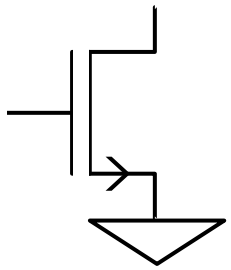
$$V_{out1} = i_1 / g_{mp1} = \frac{g_{mn1}}{g_{mp1}} V_{in}$$

Chaining stages together

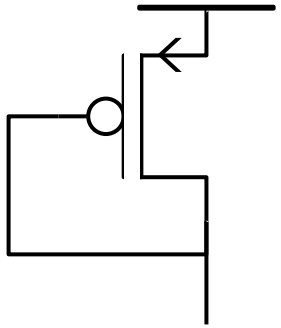


$$V_{out} = \frac{\prod_{i=1}^{N} g_{mn,i}}{\prod_{i=1}^{N} g_{mp,i}} V_{in}$$

Understanding Impedance Transformers



V → I
Converters



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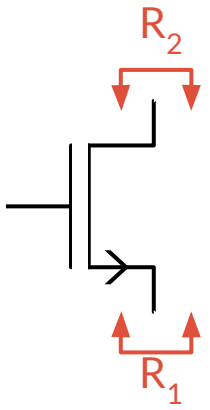
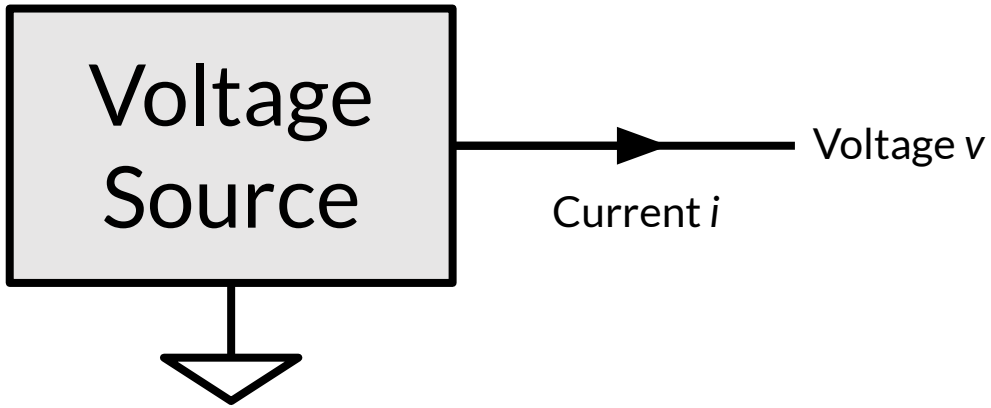


Impedance
Transformers

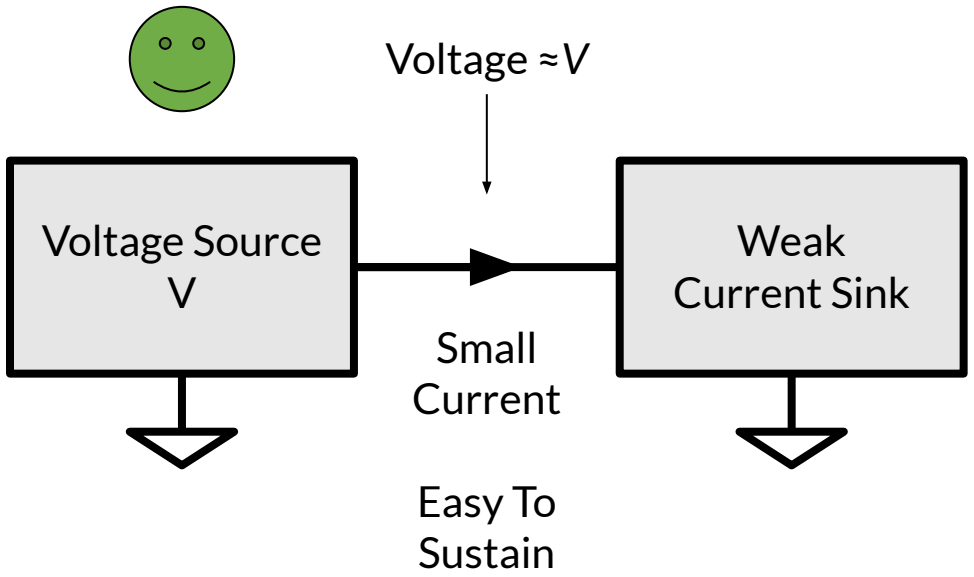
Consider a generic source of voltage

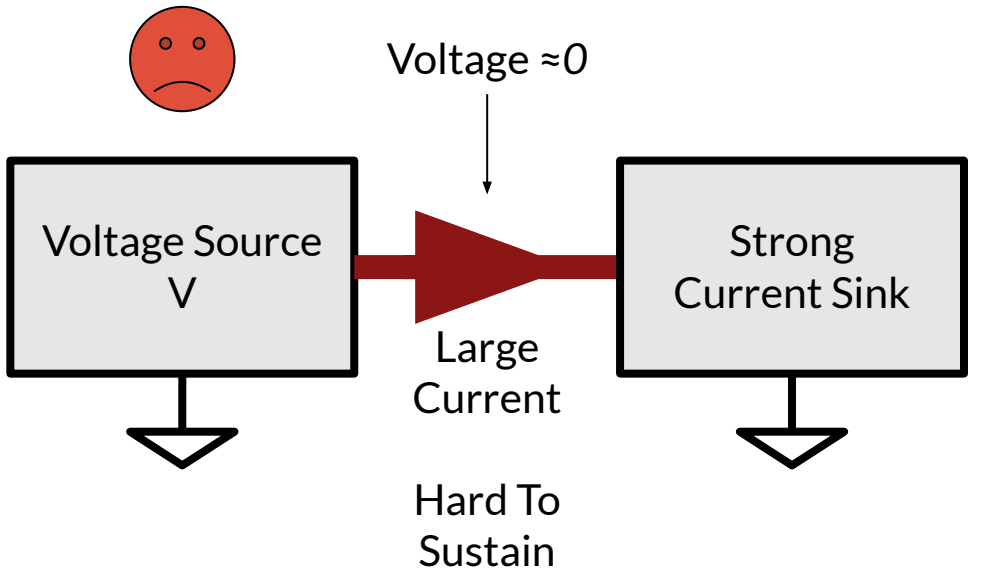


$$v = v(i) \approx v_0 + \frac{\partial v}{\partial i}(v - v_0) + \ldots = \alpha + \beta i$$

It takes “effort” to emit a current

The more current is taken from the voltage source, the more it struggles to maintain its voltage





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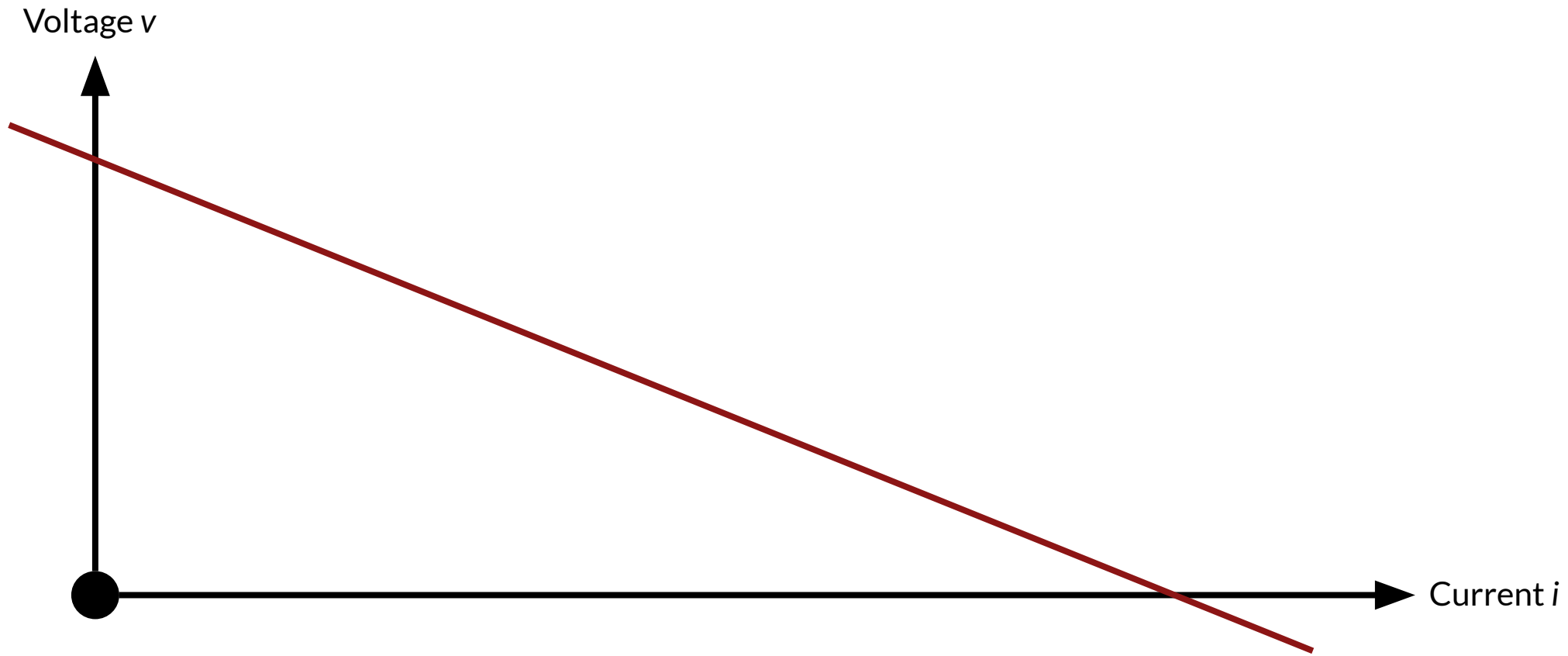
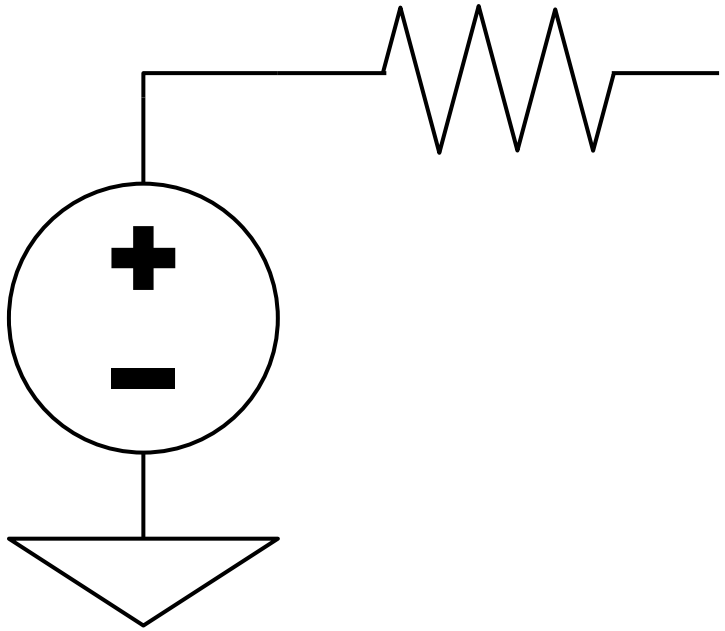


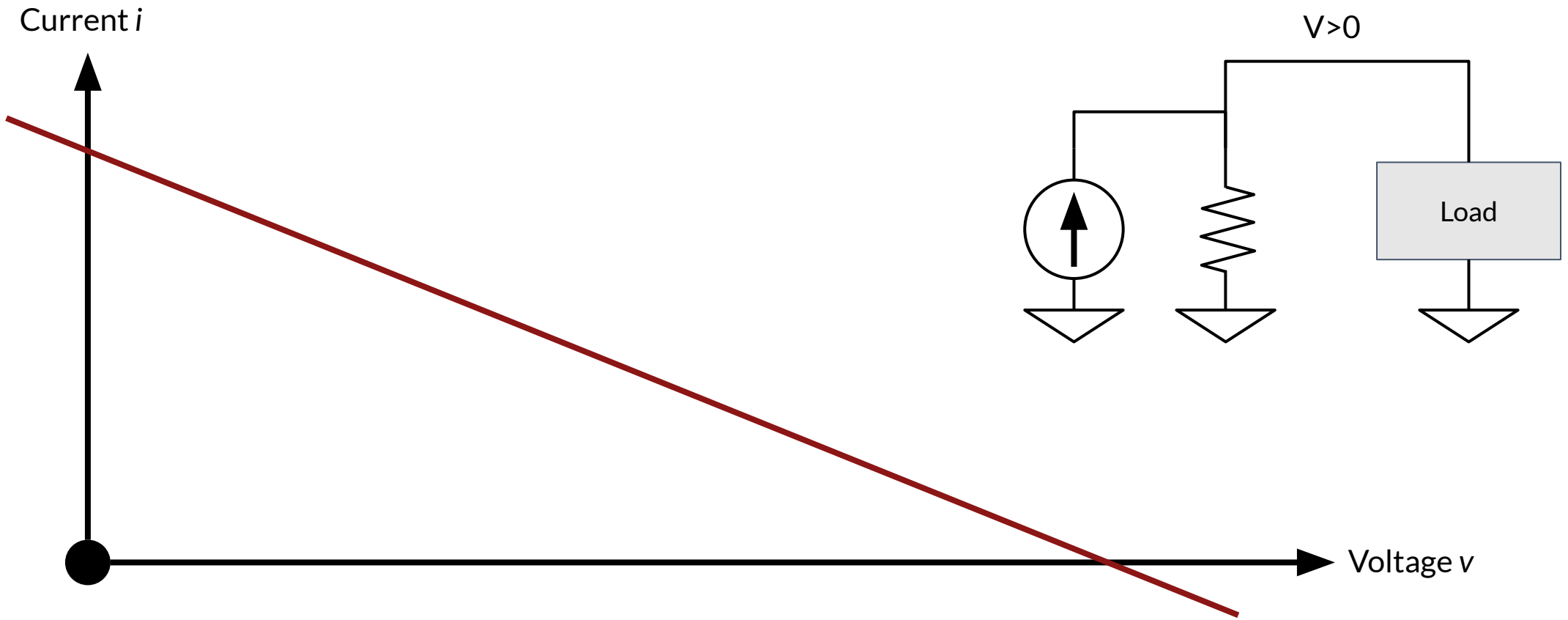
So a voltage source has some impedance

Once too much current is drawn from the voltage source, the resistor cancels it out



Similarly, it takes “effort” to maintain a voltage

The more voltage is needed, the more the source struggles to maintain it. Once too much voltage is applied, the current is controlled by the resistor, not the current source.

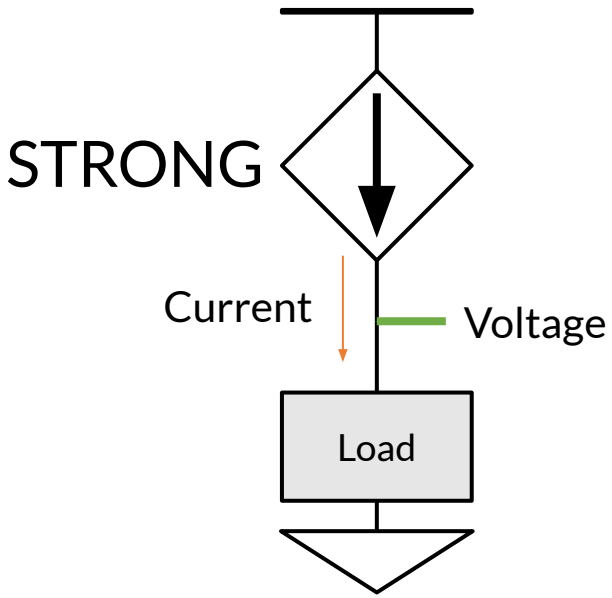


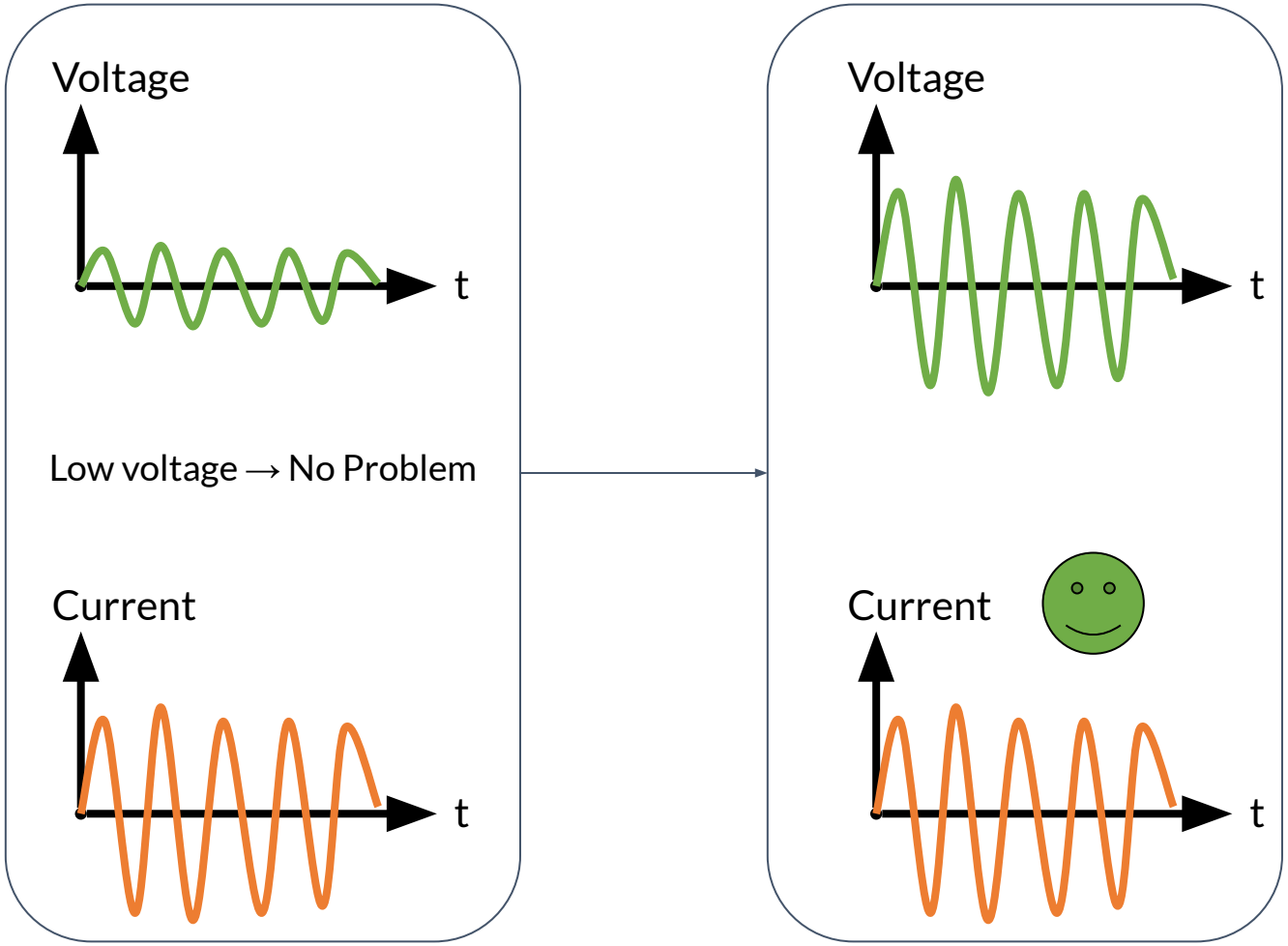
Sources of voltage and current are never ideal

Can we improve the “strength” of a current source?

What is a “strong” source of current?

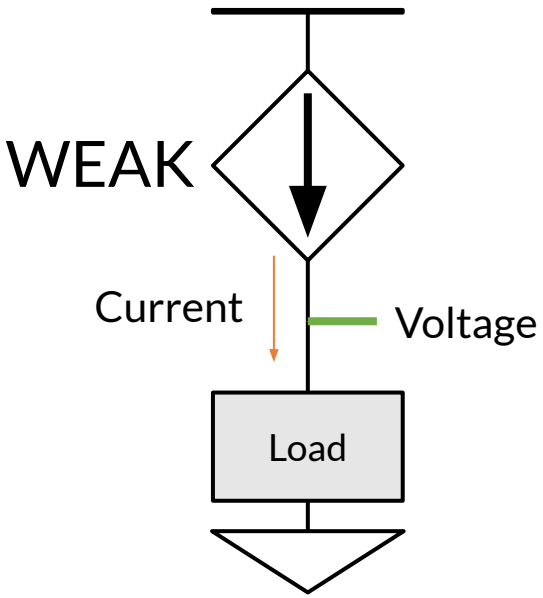
A strong source maintains a constant current at any voltage

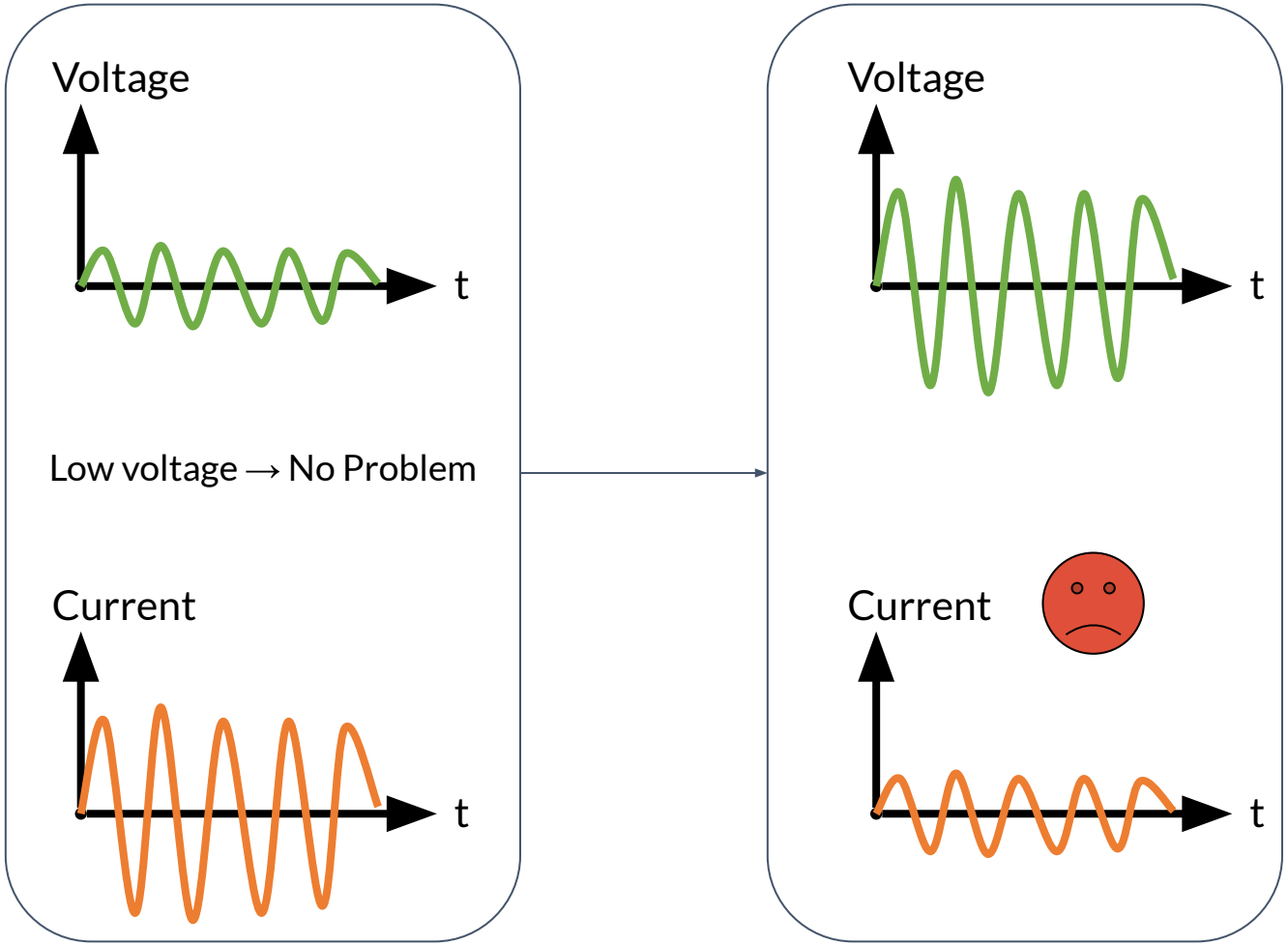




What is a “strong” source of current?

A weak source is unable to maintain its current at high voltages

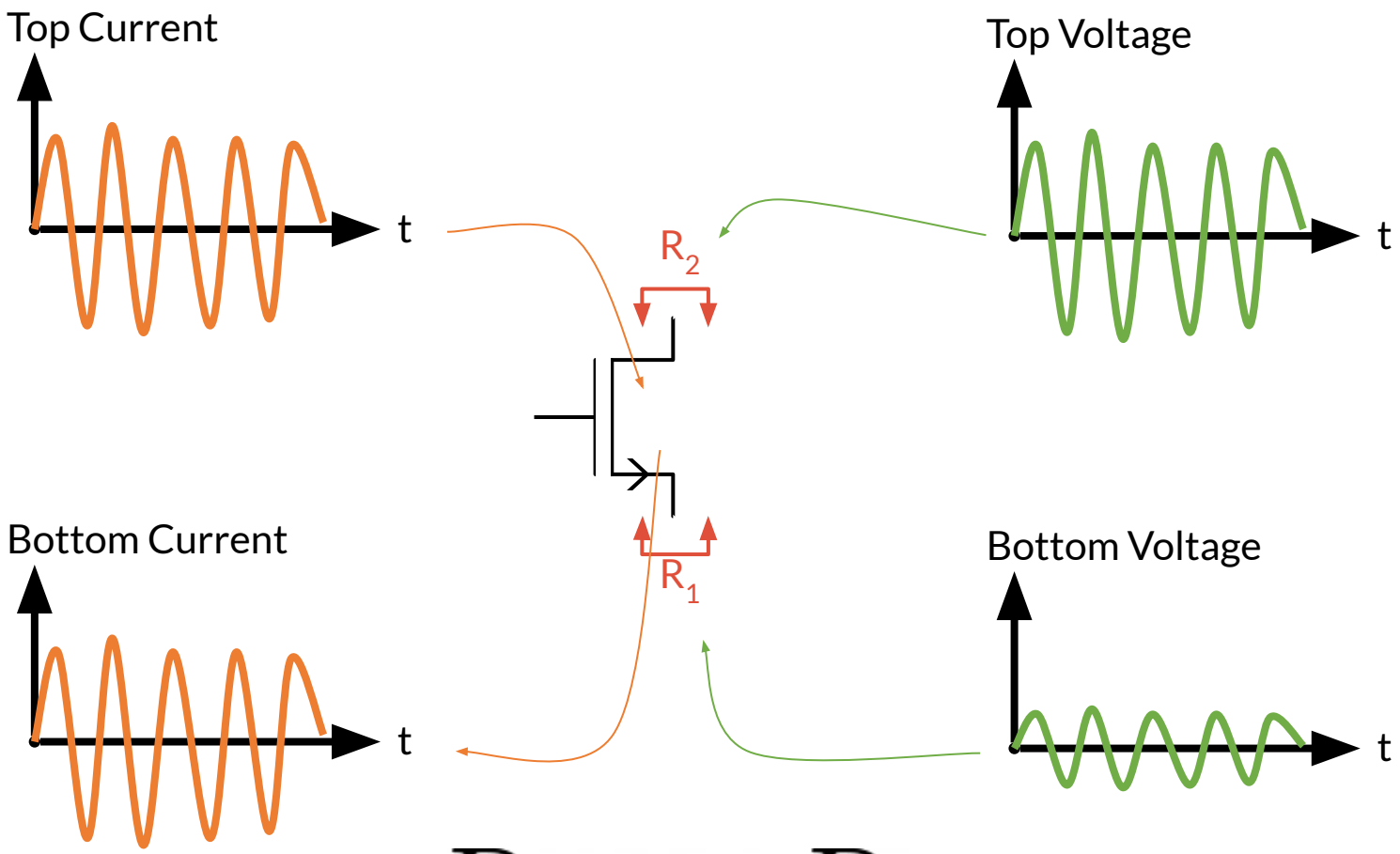




The common gate stage provides “isolation”

The drain of the transistor can freely “wiggle” while the source remains at a fixed voltage.

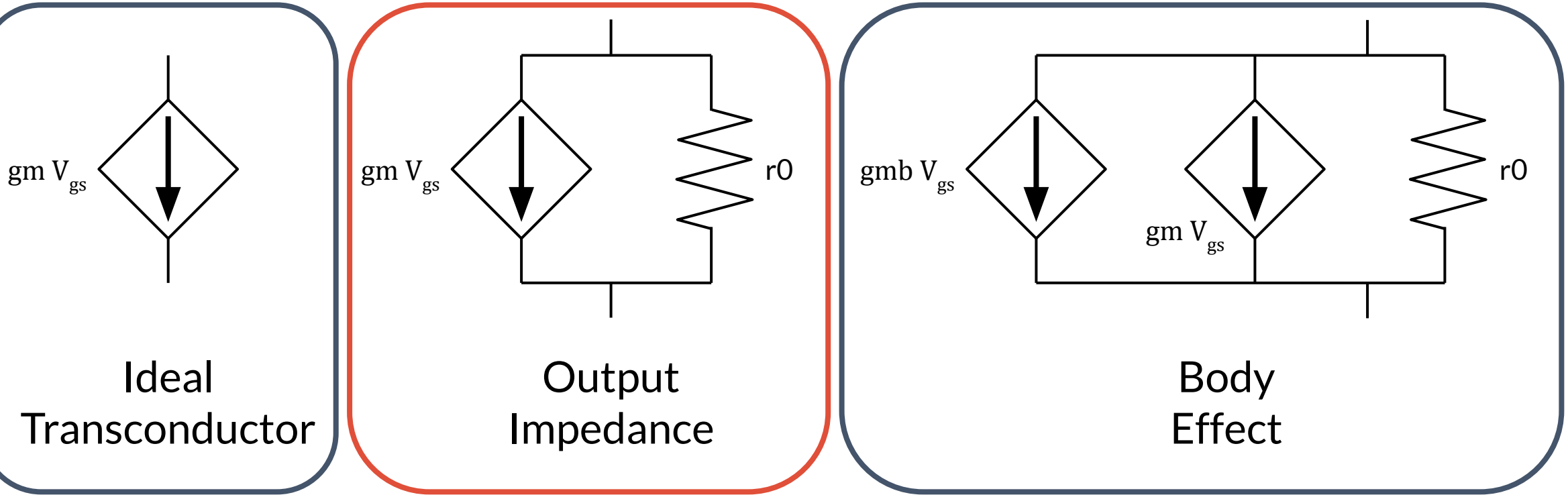
The current across the common gate stage is constant.



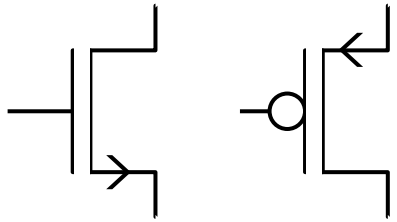
$$R_2 \gg R_1$$

MOSFET Small Signal Models

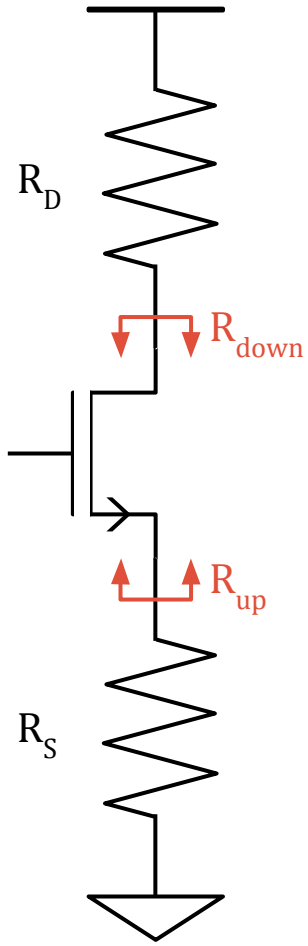
We'll use this model for the rest of the tutorial



Same model for both:



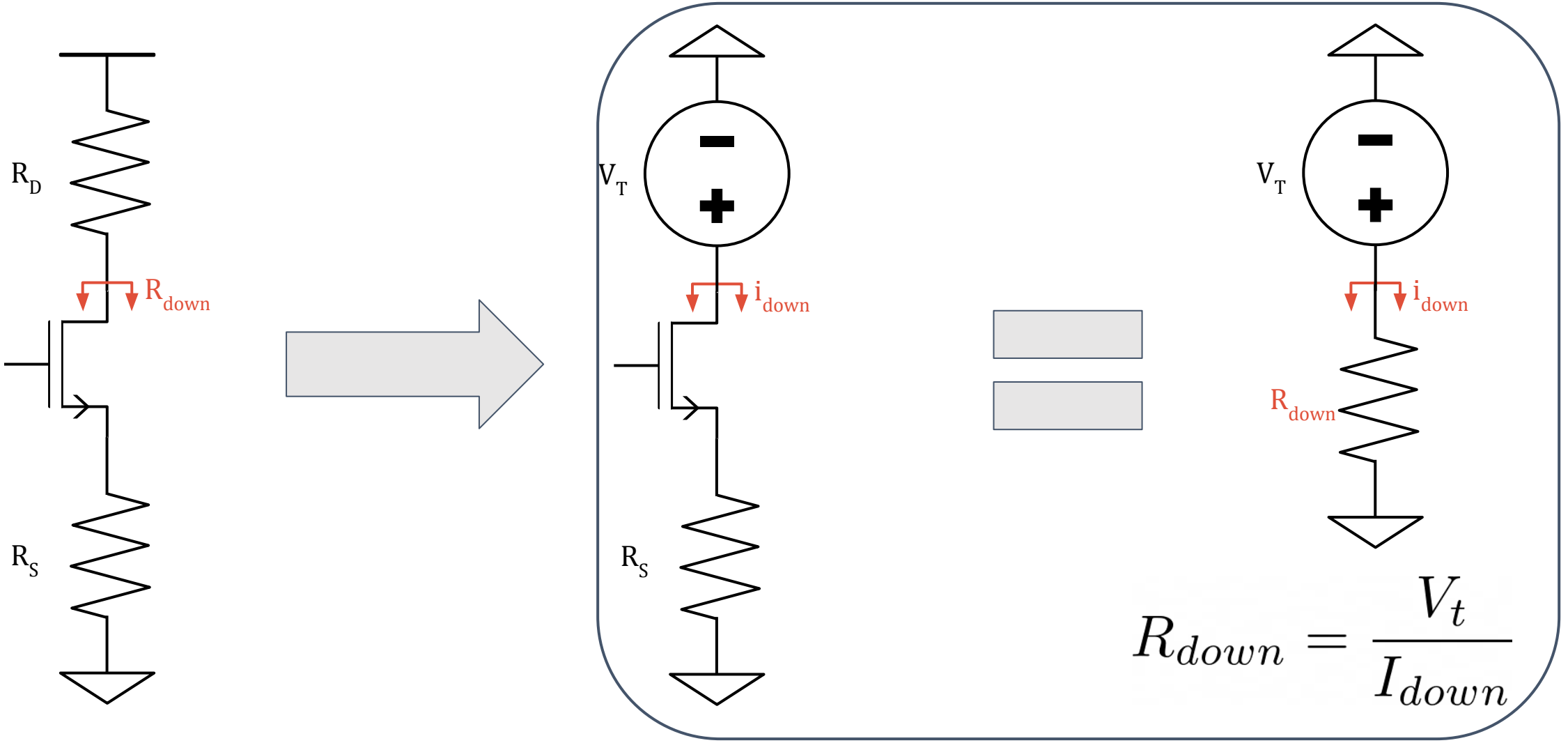
The current buffer



$$R_{down} = R_S + r_0 + g_m R_S r_0$$

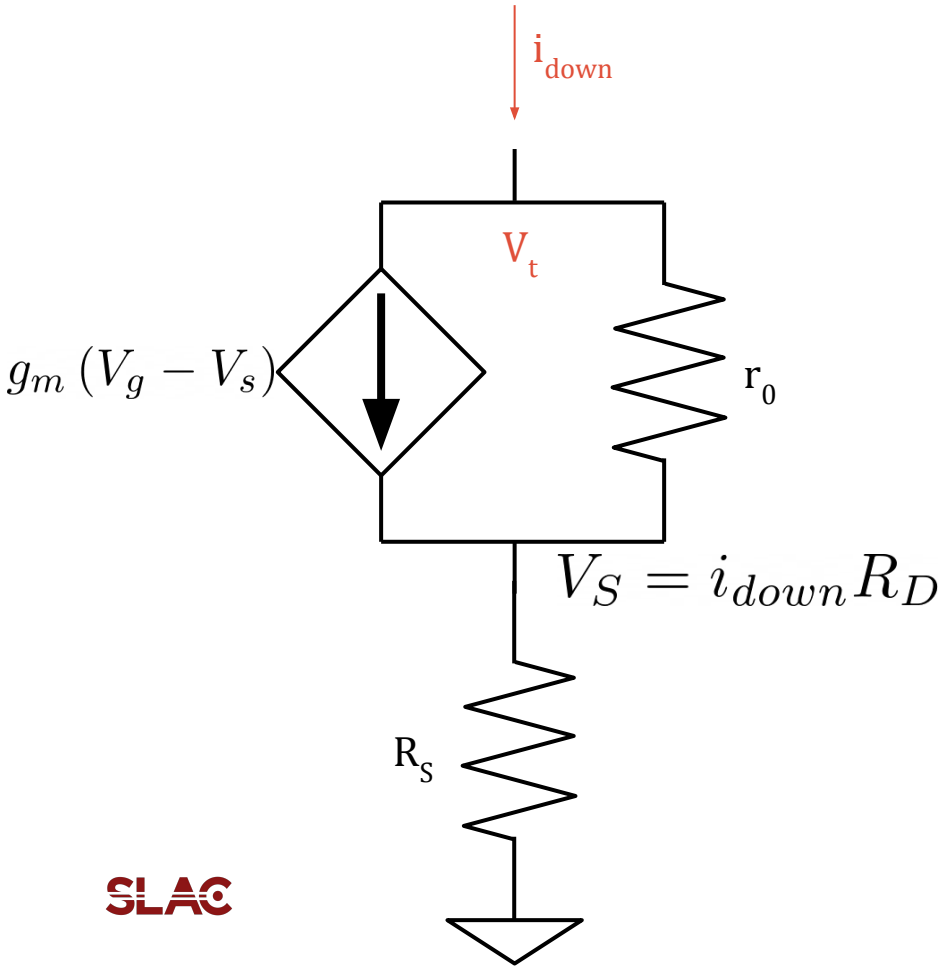
$$R_{up} = \frac{r_0 + R_D}{1 + g_m r_0}$$

Deriving the downwards impedance



$$R_{down} = \frac{V_t}{I_{down}}$$

Deriving the downwards impedance

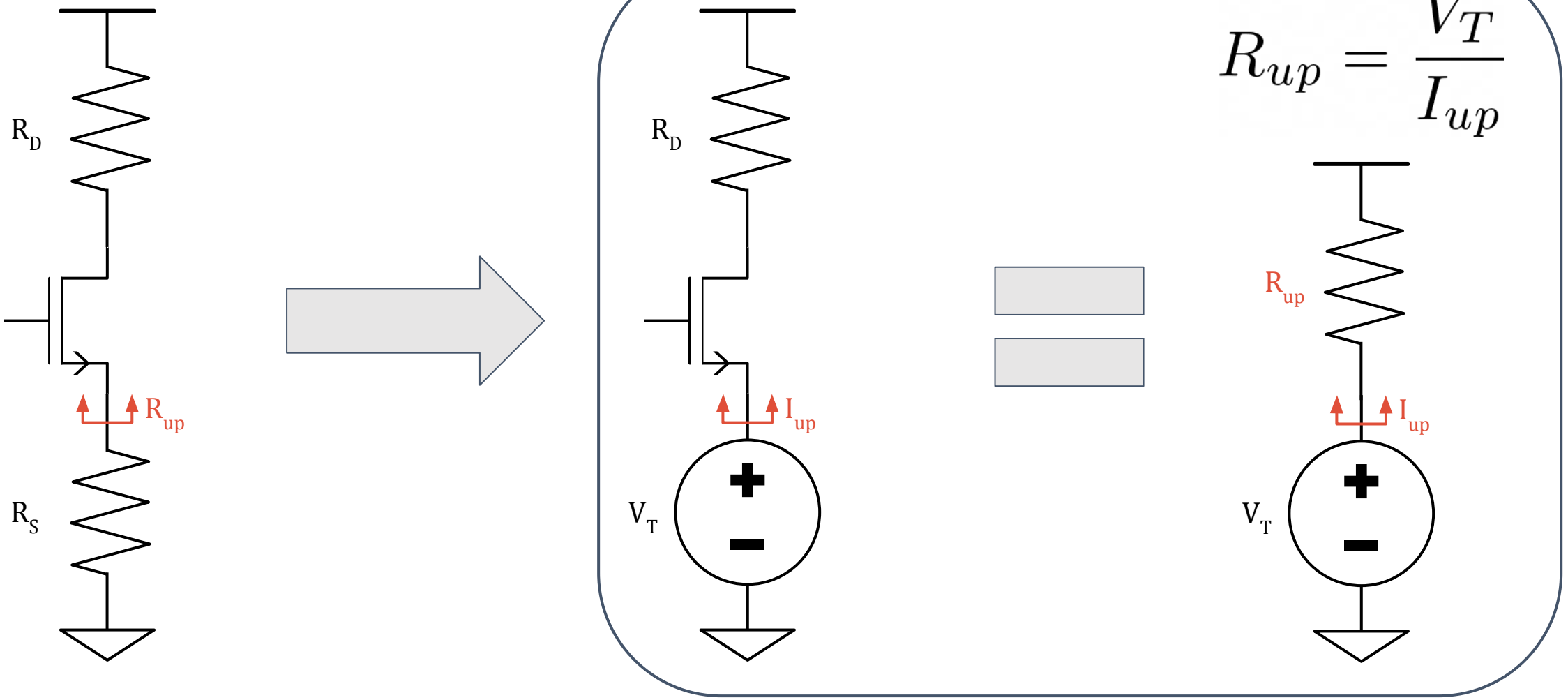


$$i_{down} = \frac{V_t - V_s}{r_0} + g_m(-V_s)$$

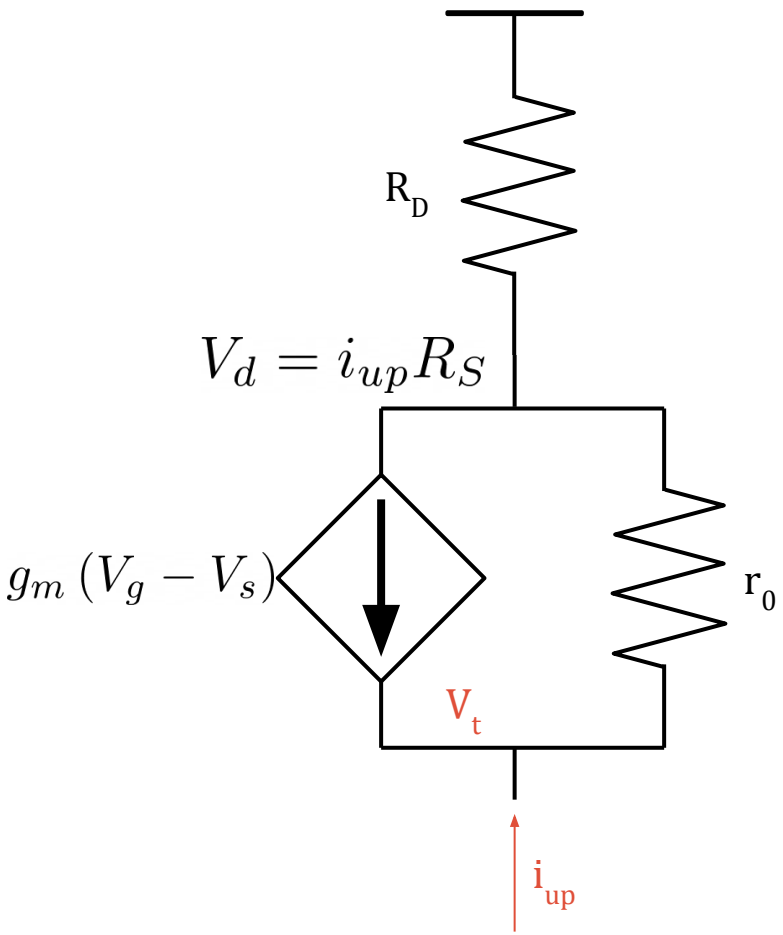
$$i_{down} = \frac{V_t - R_D i_{down}}{r_0} - g_m R_D i_{down}$$

$$R_{down} = \frac{V_t}{i_{down}} = R_S + r_0 + g_m r_0 R_S$$

Deriving the upwards impedance



Deriving the upwards impedance

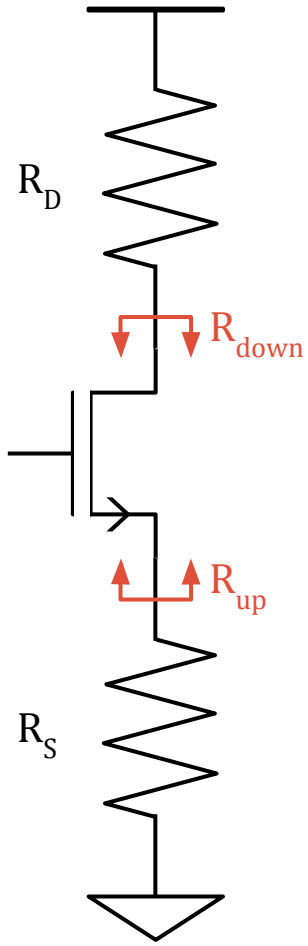


$$i_{up} = \frac{V_t - V_d}{r_0} - g_m(-V_t)$$

$$i_{up} = \frac{V_t - i_{up} R_D}{r_0} - g_m(-V_t)$$

$$R_{up} = \frac{V_t}{i_{up}} = \frac{r_0 + R_D}{1 + g_m r_0}$$

Intuition: The transistor arrow is the low-impedance port



$$R_{down} \approx (g_m r_0) R_S \gg R_S$$

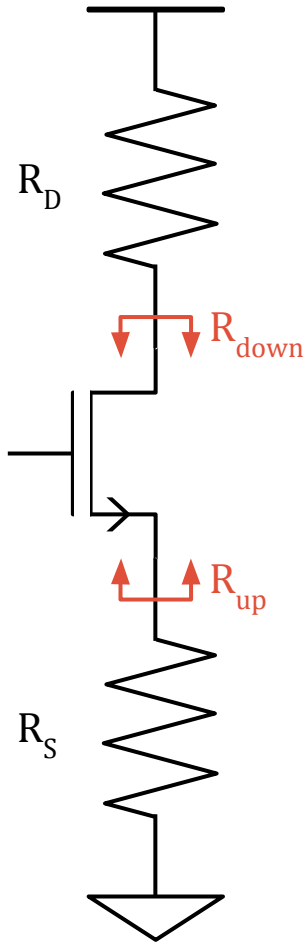
The source draws-in current with its low impedance.
The drain re-emits it with high impedance.

$$R_{up} \approx \frac{1}{g_m} \ll R_D$$

Small Signal DC Analysis

How to quickly solve any circuit with no feedback loops

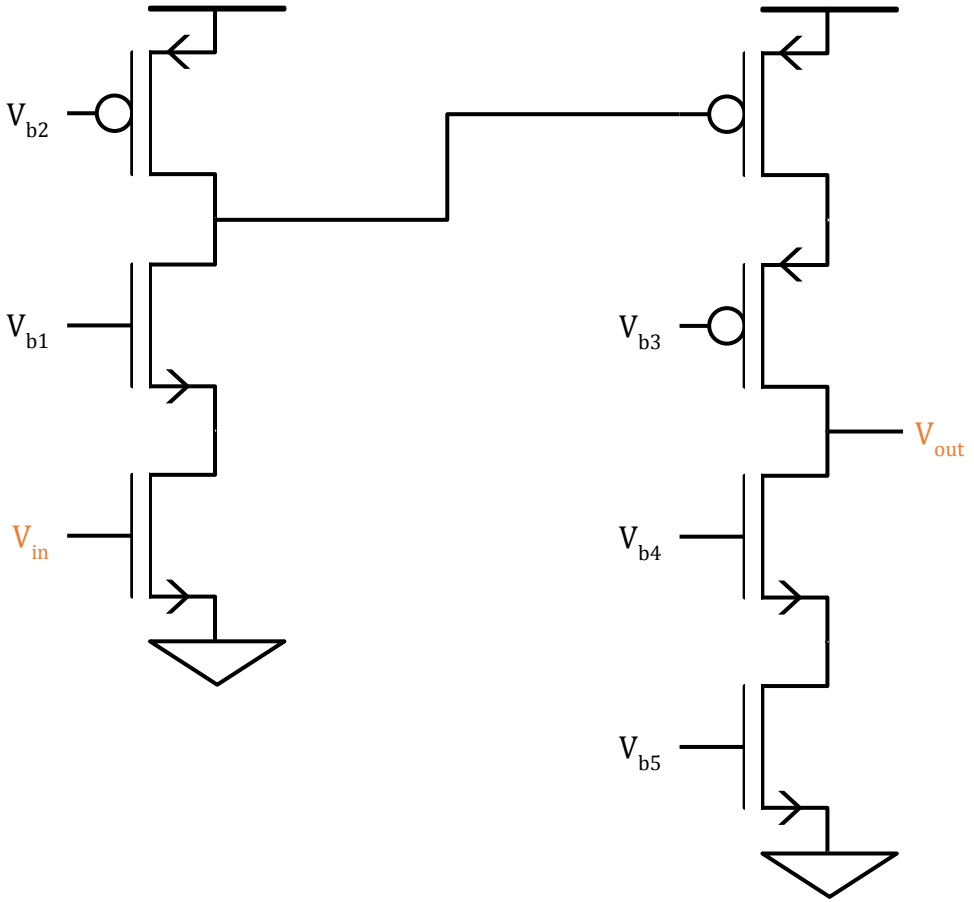
The key diagram



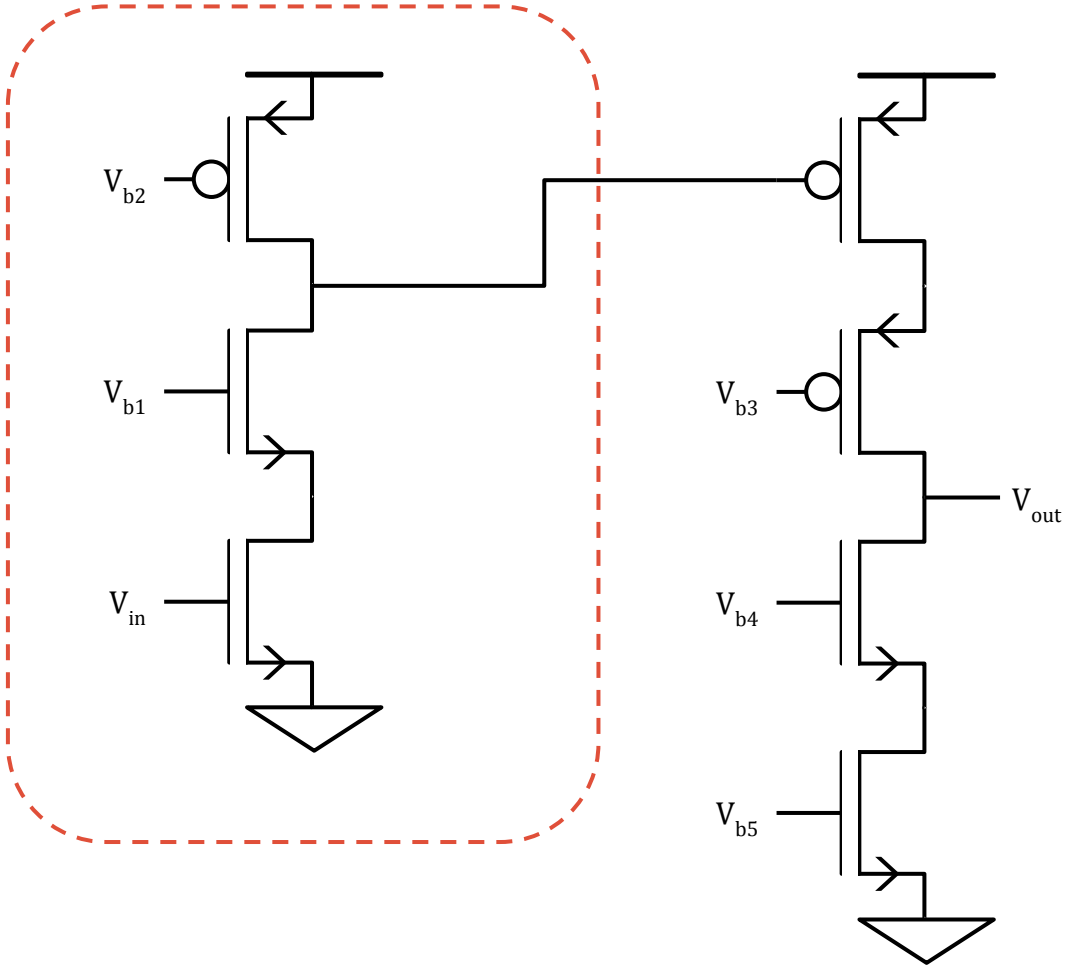
$$R_{down} = R_S + r_0 + g_m R_S r_0$$

$$R_{up} = \frac{r_0 + R_D}{1 + g_m r_0}$$

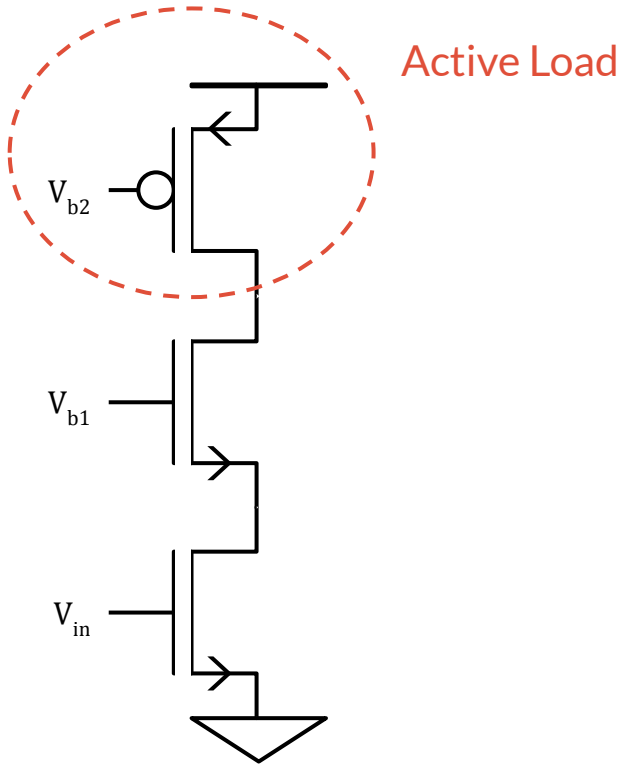
Example walkthrough

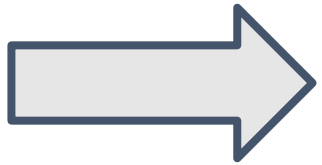


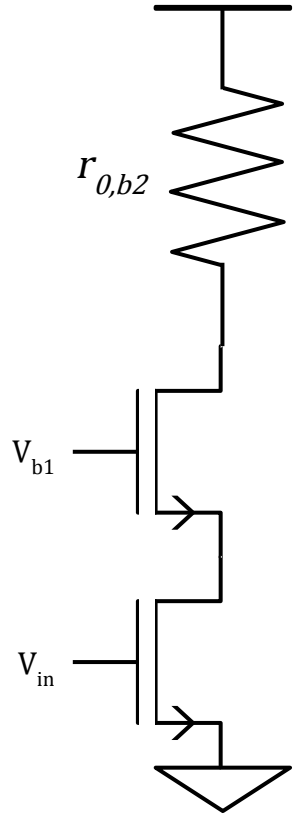
Example walkthrough



Example walkthrough

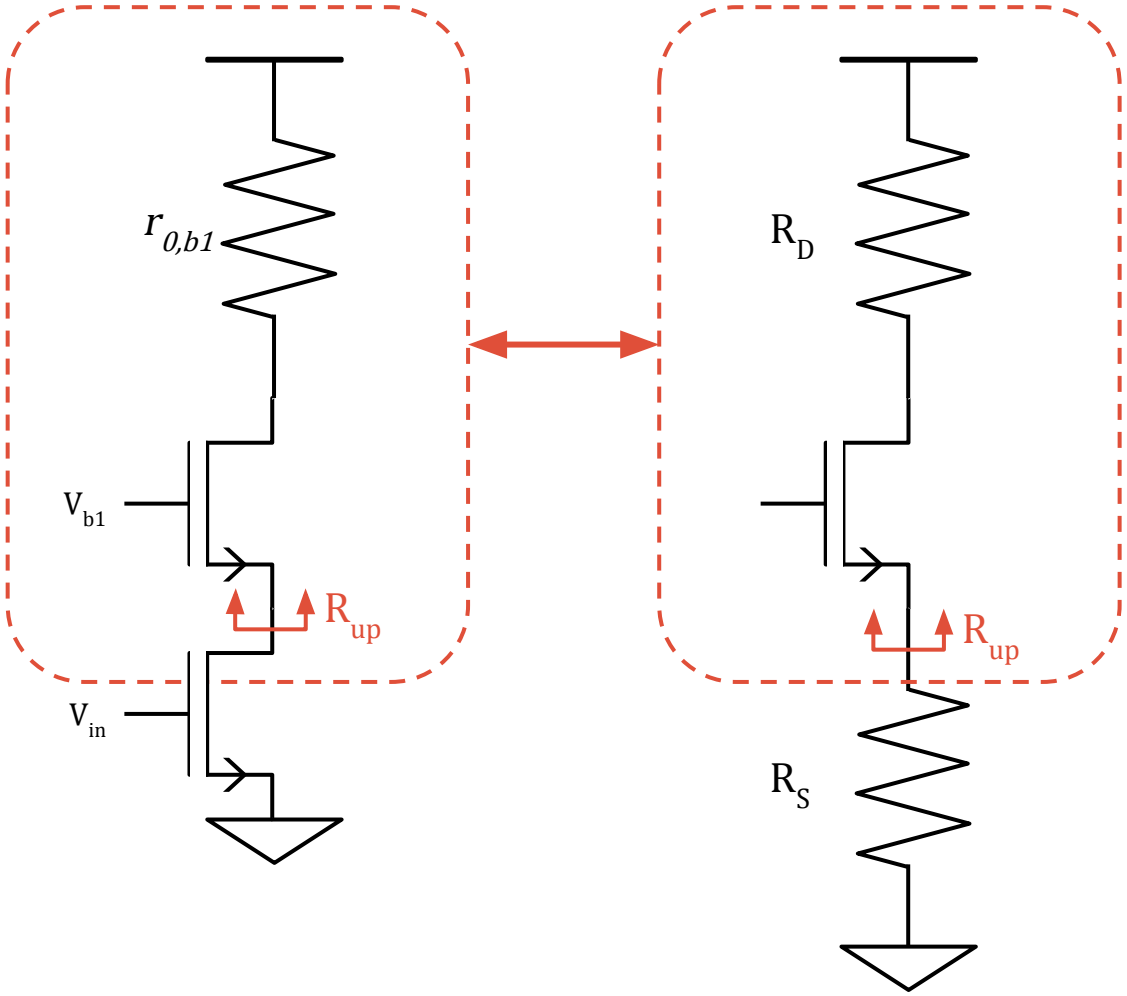




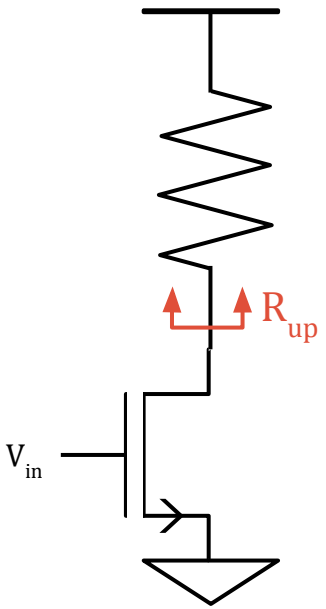


Example walkthrough

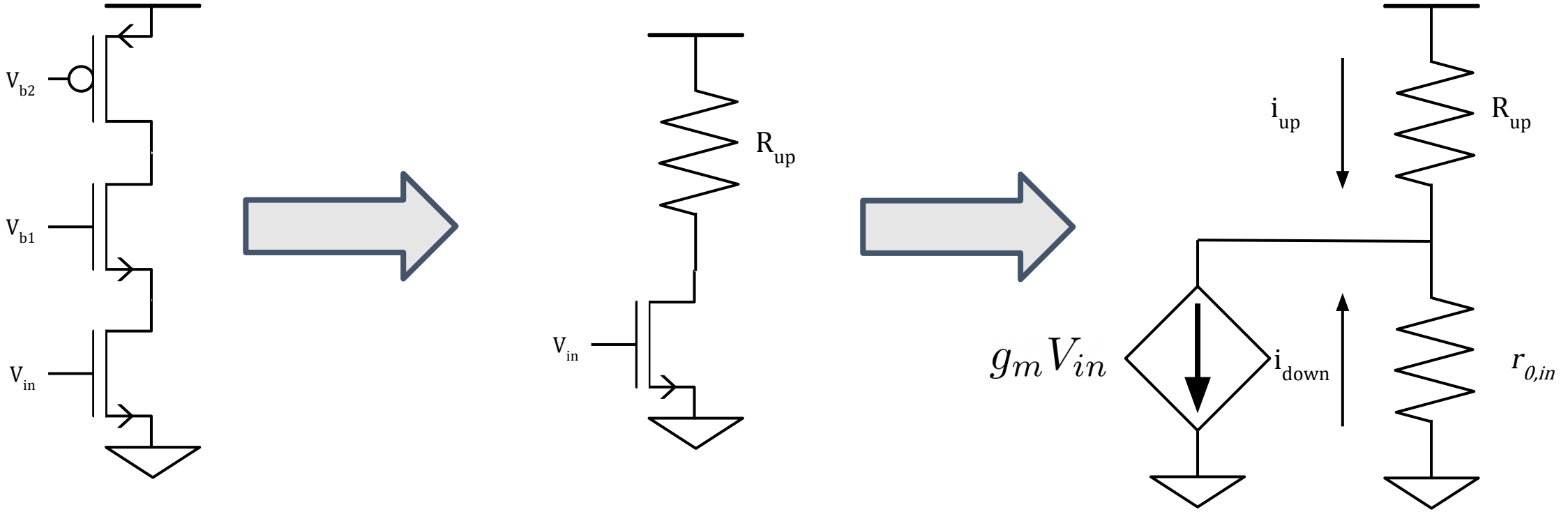
We have a current buffer



$$R_{up} = \frac{r_{0,b1} + r_{0,b2}}{1 + g_{m,b1} r_{0,b1}}$$



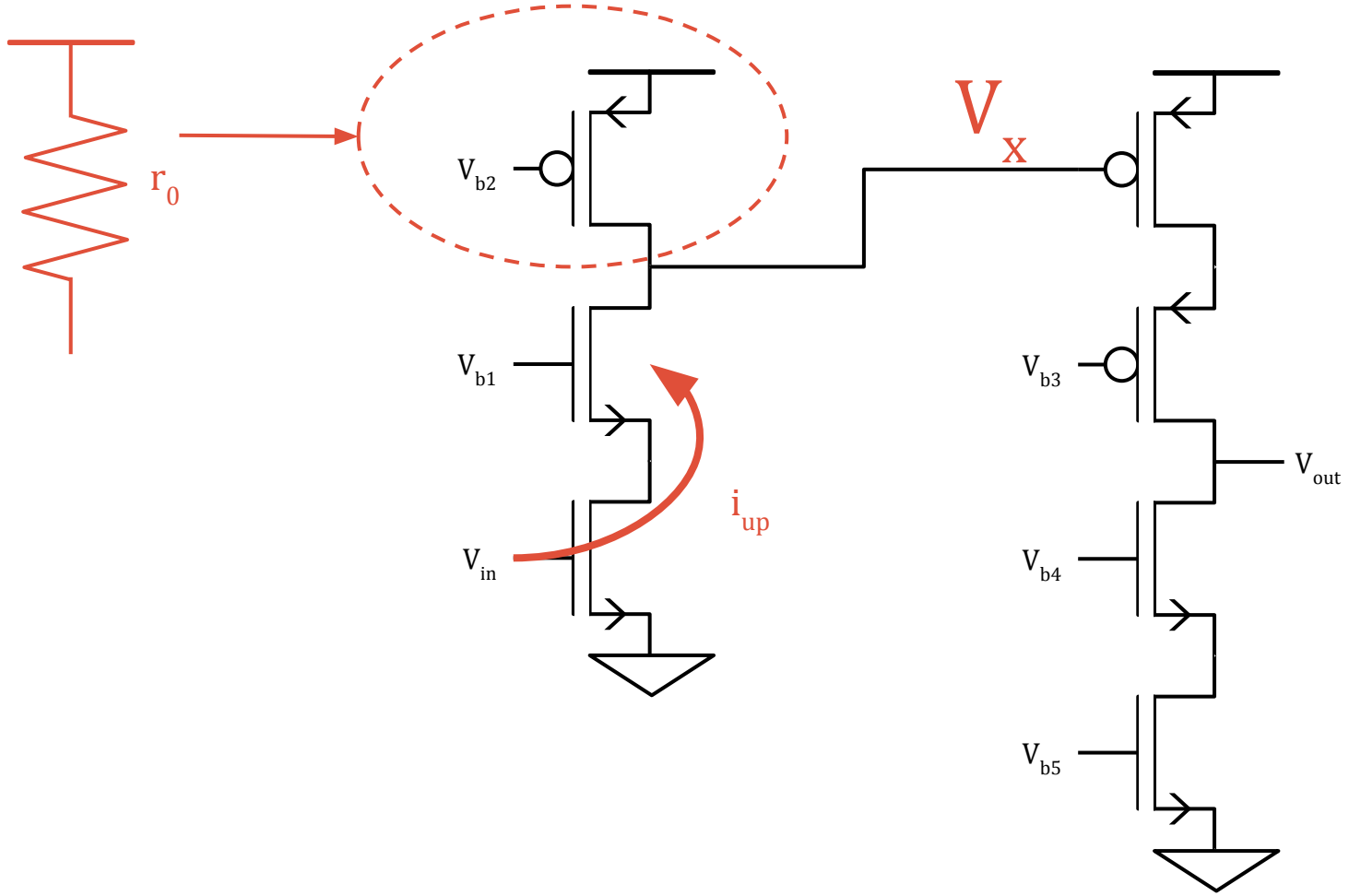
Example walkthrough



$$i_{up} = -g_{m,in} V_{in} \frac{r_{0,in}}{r_{0,in} + R_{up}}$$

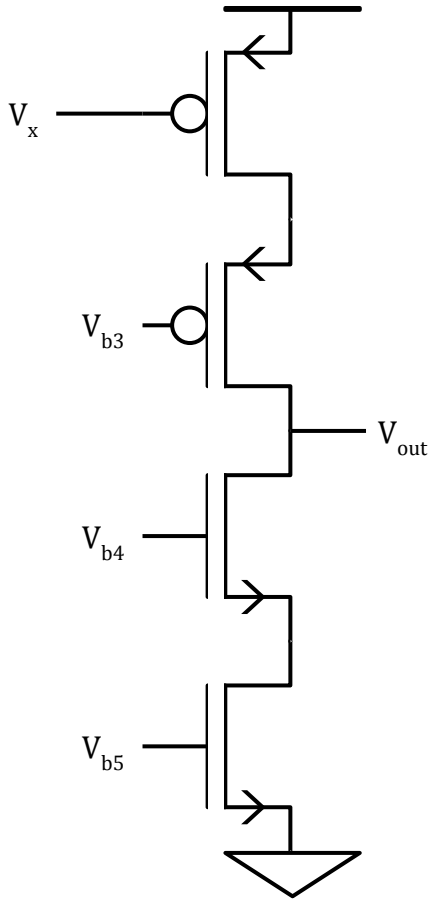
Example walkthrough

We know V_x now



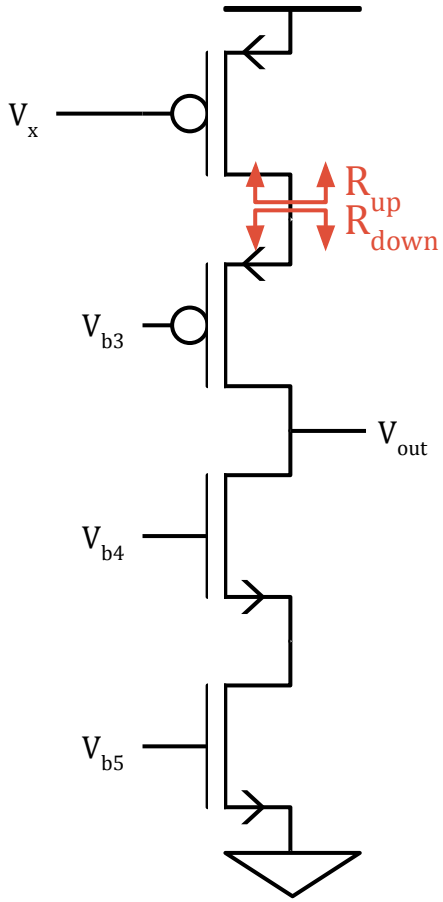
Example walkthrough

Let’s go faster by using intuition



Example walkthrough

Let’s go faster by using intuition

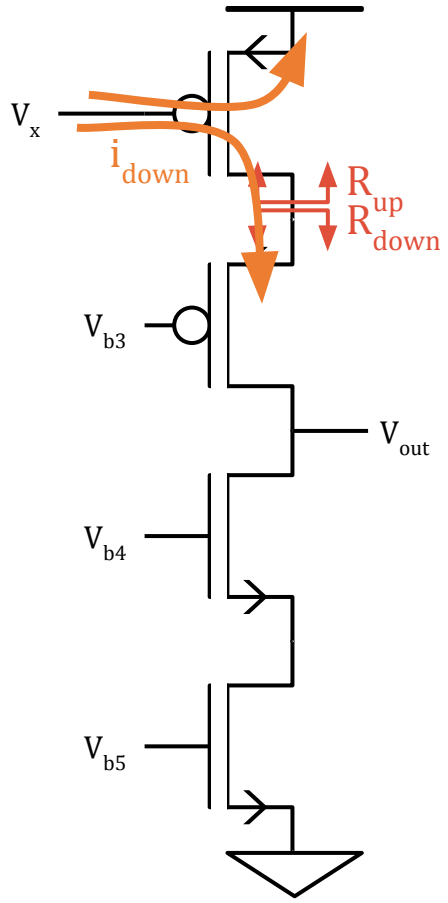


$$R_{up} = r_0$$

$$R_{down} \approx 1/g_m$$

Example walkthrough

Let's go faster by using intuition



$$R_{up} = r_0$$

$$R_{down} \approx 1/g_m$$

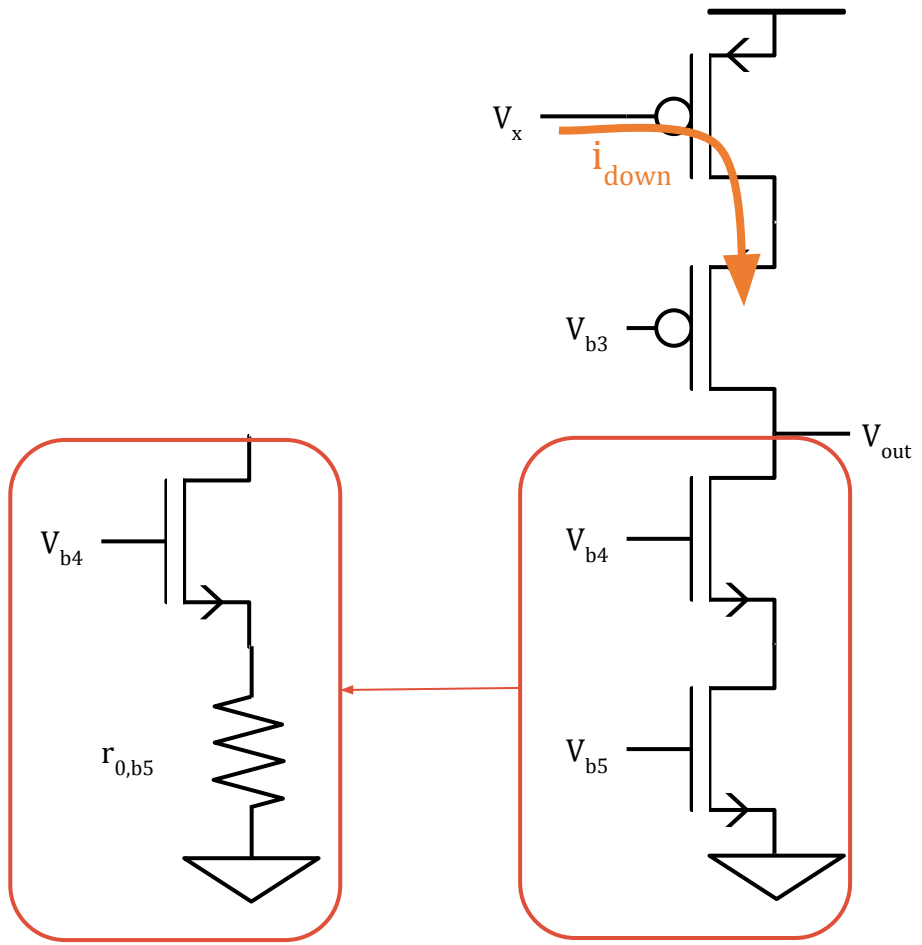
$$i_{down} = -g_{m,x} V_x \frac{R_{up}}{R_{up} + R_{down}}$$

$$i_{down} = \frac{-g_{am,x} r_{0,x}}{r_{0,x} + 1/g_{m,b3}} V_x$$

Example walkthrough

Let's go faster by using intuition

$$i_{down} = \frac{-g_{am,x} r_{0,x}}{r_{0,x} + 1/g_{m,b3}} V_x$$

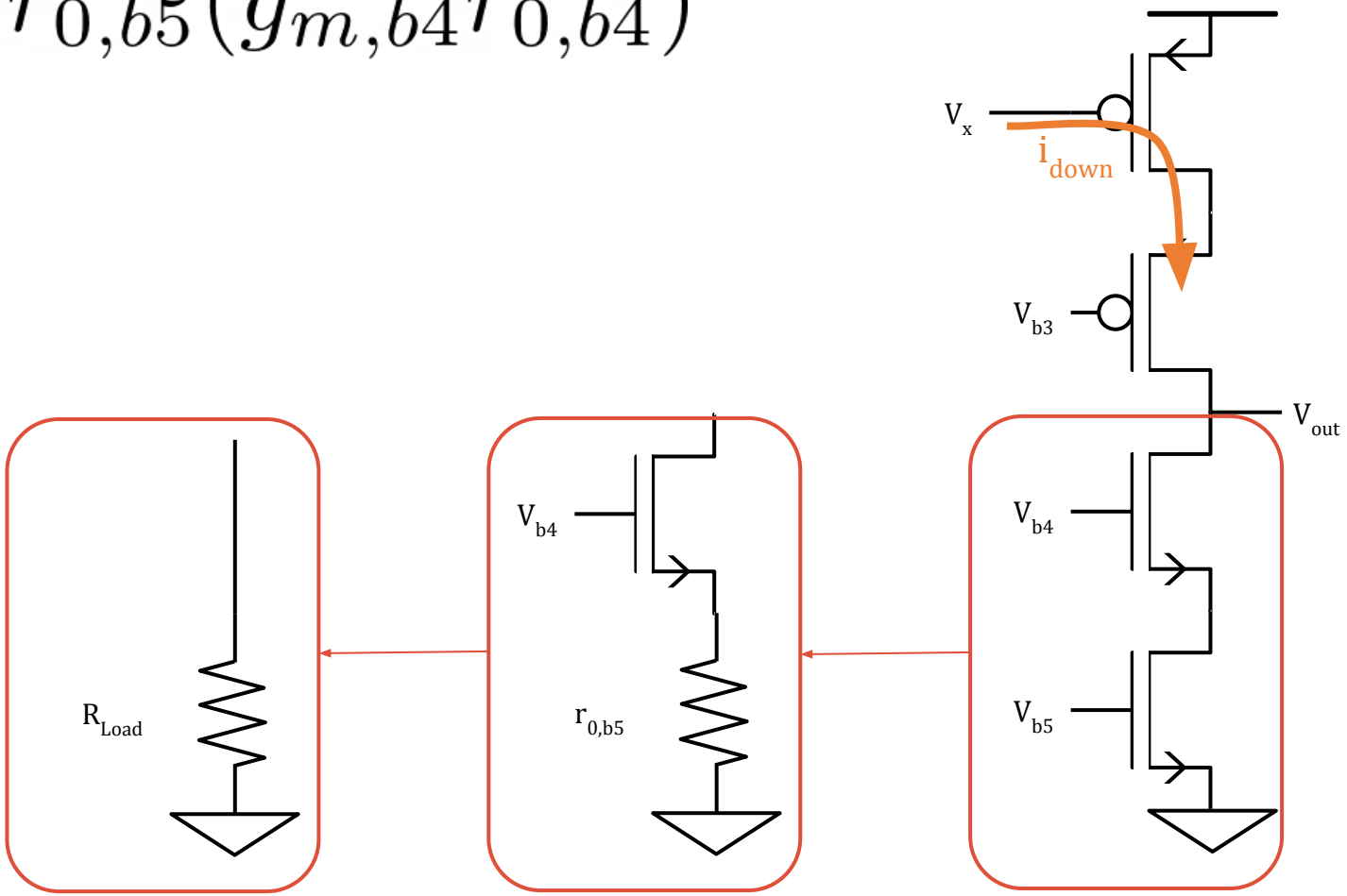


Example walkthrough

Let's go faster by using intuition

$$R_{load} \approx r_{0,b5}(g_{m,b4}r_{0,b4})$$

$$i_{down} = \frac{-g_{am,x}r_{0,x}}{r_{0,x} + 1/g_{m,b3}}V_x$$



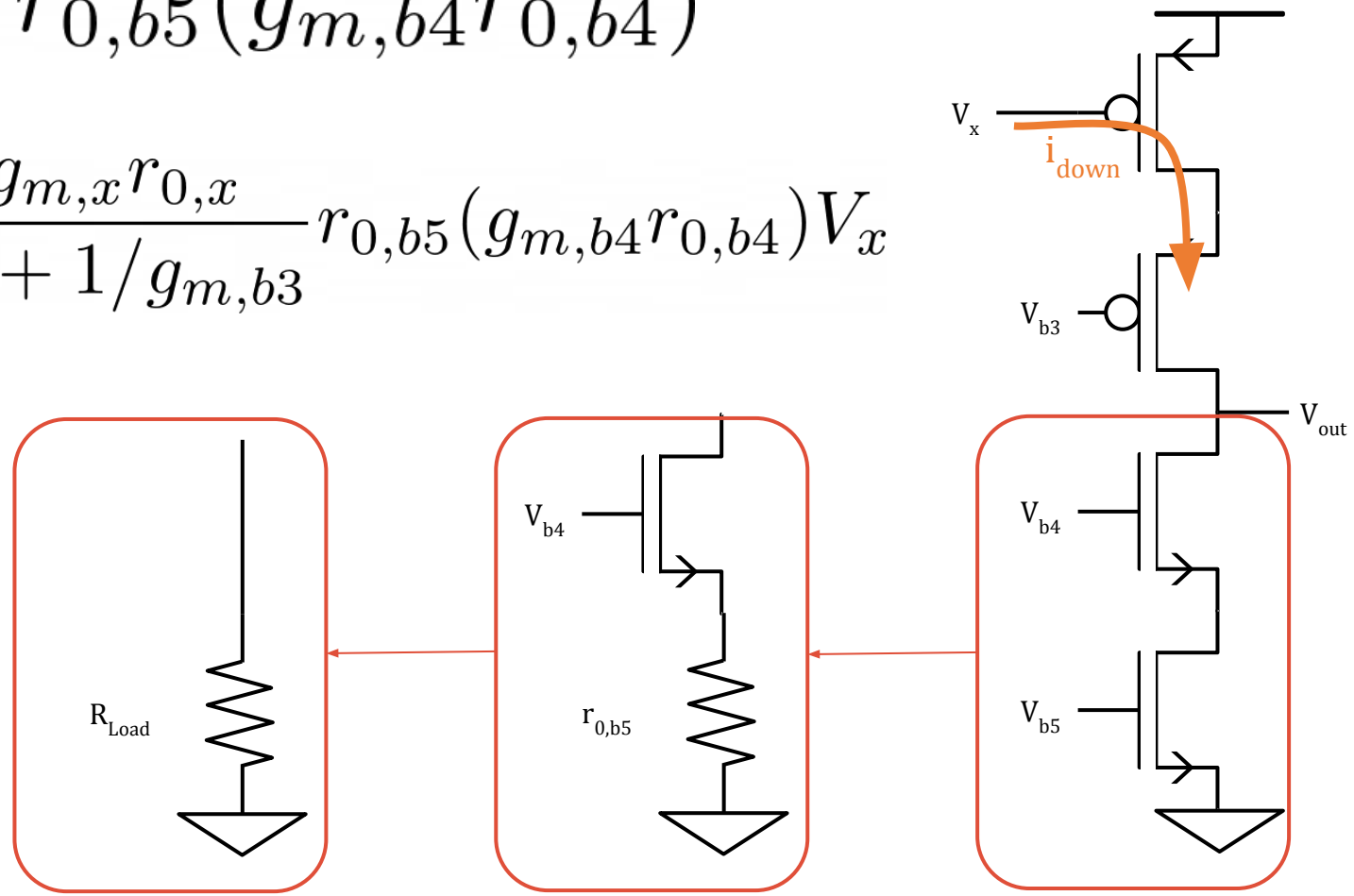
Example walkthrough

Let's go faster by using intuition

$$i_{down} = \frac{-g_{am,x} r_{0,x}}{r_{0,x} + 1/g_{m,b3}} V_x$$

$$R_{load} \approx r_{0,b5}(g_{m,b4} r_{0,b4})$$

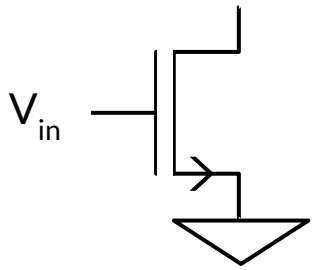
$$V_{out} \approx \frac{-g_{m,x} r_{0,x}}{r_{0,x} + 1/g_{m,b3}} r_{0,b5}(g_{m,b4} r_{0,b4}) V_x$$



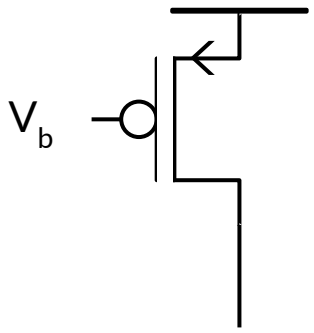
Small Signal DC Analysis

Designing circuits with building blocks

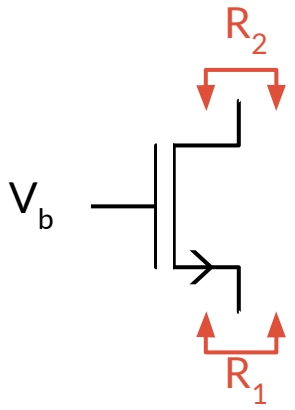
The three most used building blocks



V → I Converter



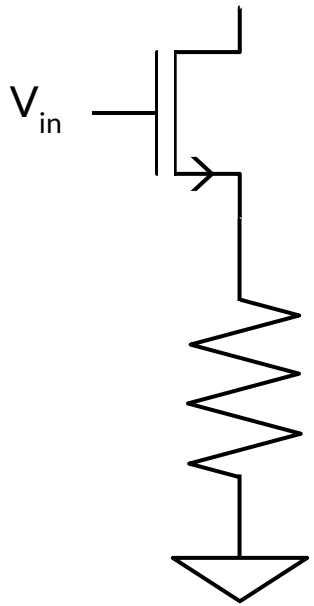
I → V Converter



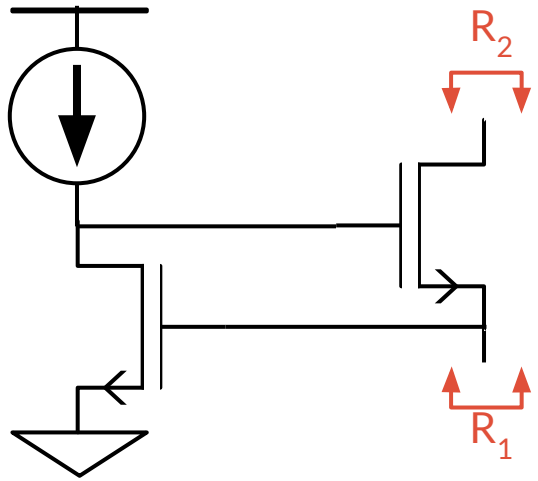
Current Buffer

The source draws-in current with its low impedance.
The drain re-emits it with high impedance.

But there are more!

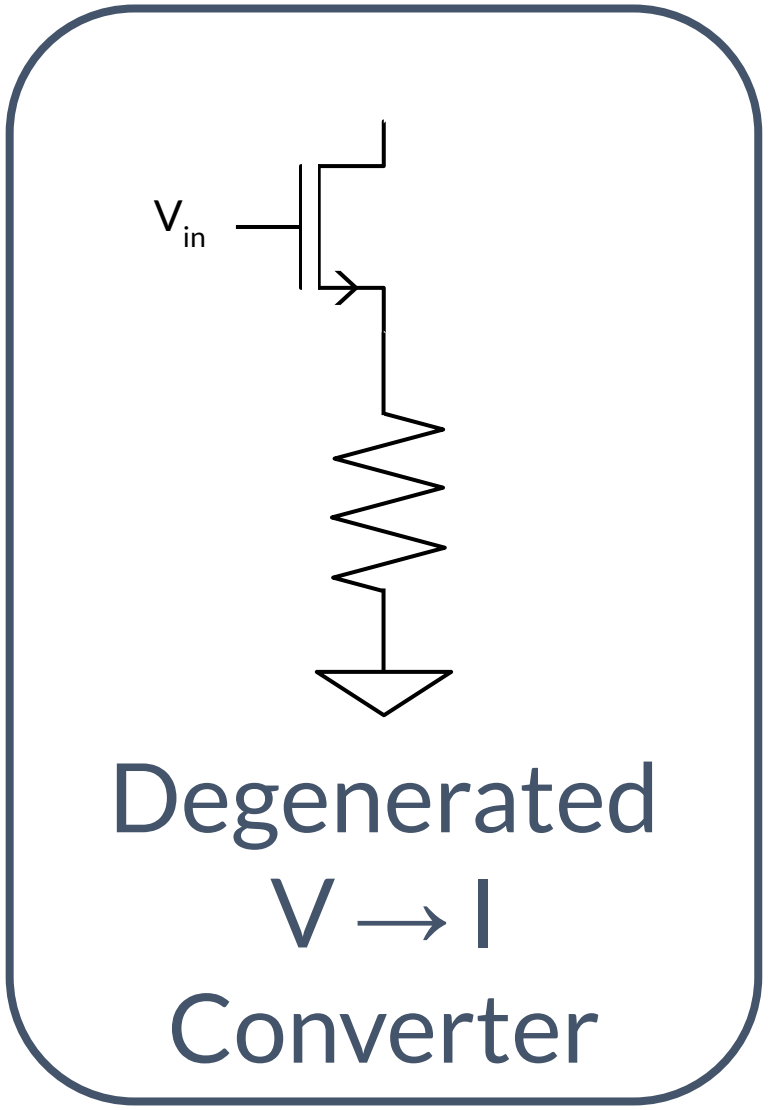


Degenerated
$V \rightarrow I$
Converter



"Super"
Common-Gate

But there are more!



The resistor decreases the gain, but increases the bandwidth

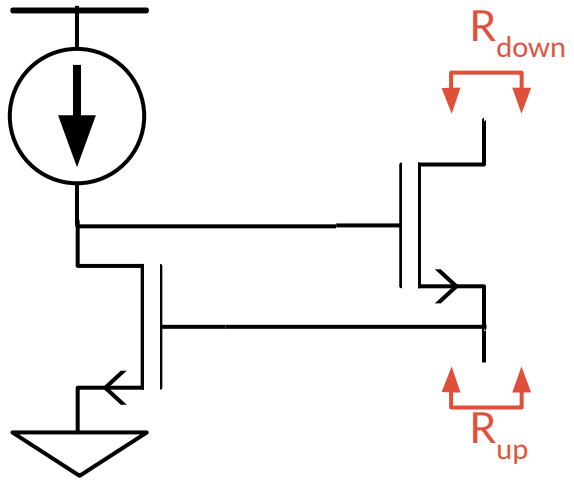
(See feedback coming up)

But there are more!

The feedback transistor “boosts” the impedance of this current buffer by a factor gm*r0

$$R_{down} = R_S + r_0 + g_m R_S r_0$$

$$R_{down} = R_S + r_0 + g_m R_s r_0 \left(1 + g_m r_0 (1 + r_0/R_I)\right)$$



“Super” Common-Gate

DC Biasing And Sizing Transistors

Device equations and gm/Id

Back to the MOSFET I-V equation

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(V_{gs} - V_{th}\right)^2$$

Key Observation

Current is linear in the width (intuitive)

$$I_D = W f(V_{gs}, L)$$

Consequences: gm/Id is a constant ratio!

gm/Id only depends on how the transistor is biased! It is independent of W

$$I_D = W f\left(V_{gs}, L\right)$$

$$g_m = \frac{\partial I_D}{\partial V_{gs}} = W f'\left(V_{gs}, L\right)$$

$$\frac{g_m}{I_D} = h\left(V_{gs}, L\right)$$

Design Methodology

Use gm/Id to describe how a transistor is biased and operating

$$g_m = \frac{g_m}{I_D} I_D$$

$$W = I_D / \frac{I_D}{W}$$

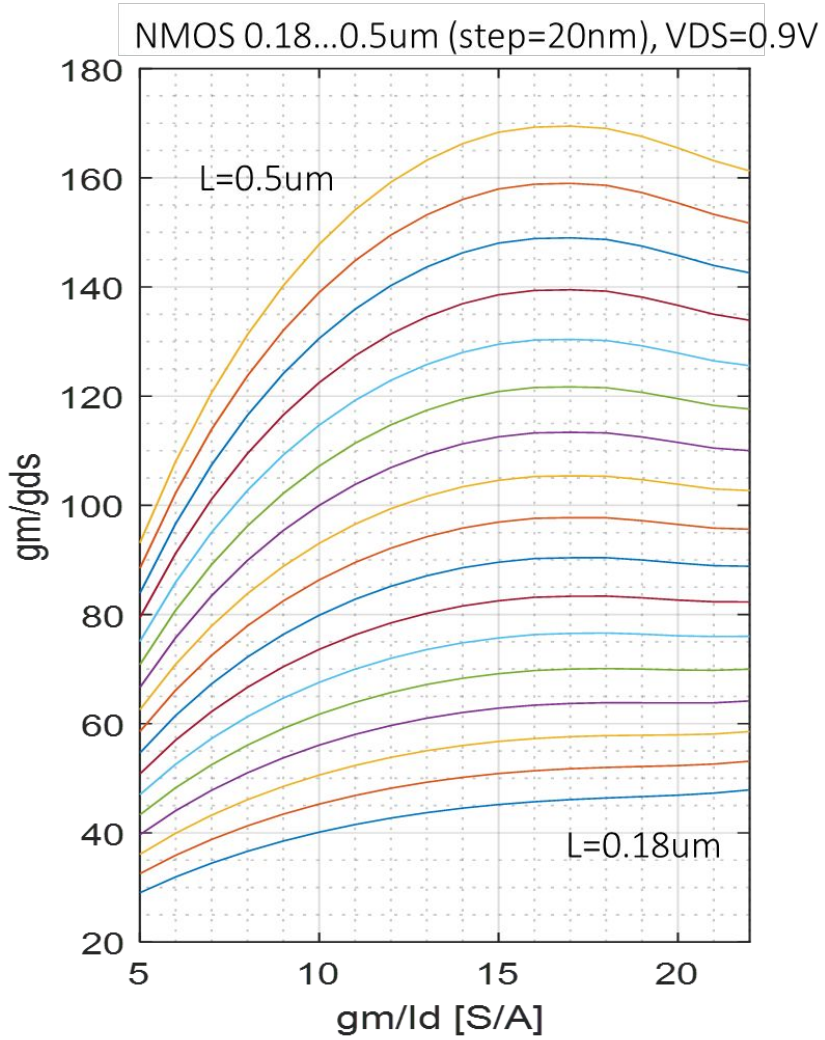
$$C_{gg} = g_m / \frac{g_m}{C_{gg}}$$

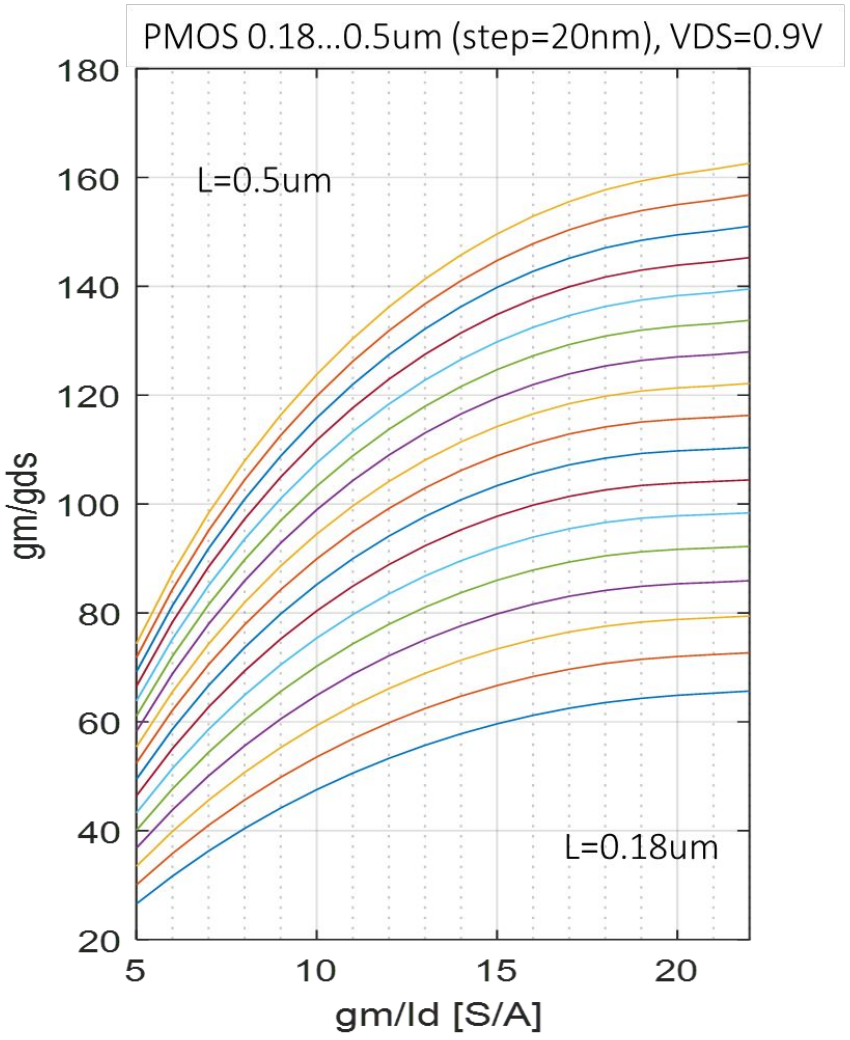
$$\frac{I_D}{W} = f_\alpha \left(\frac{g_m}{I_D}, L \right)$$

$$\frac{g_m}{C_{gg}} = \omega_T = f_\beta \left(\frac{g_m}{I_D}, L \right)$$

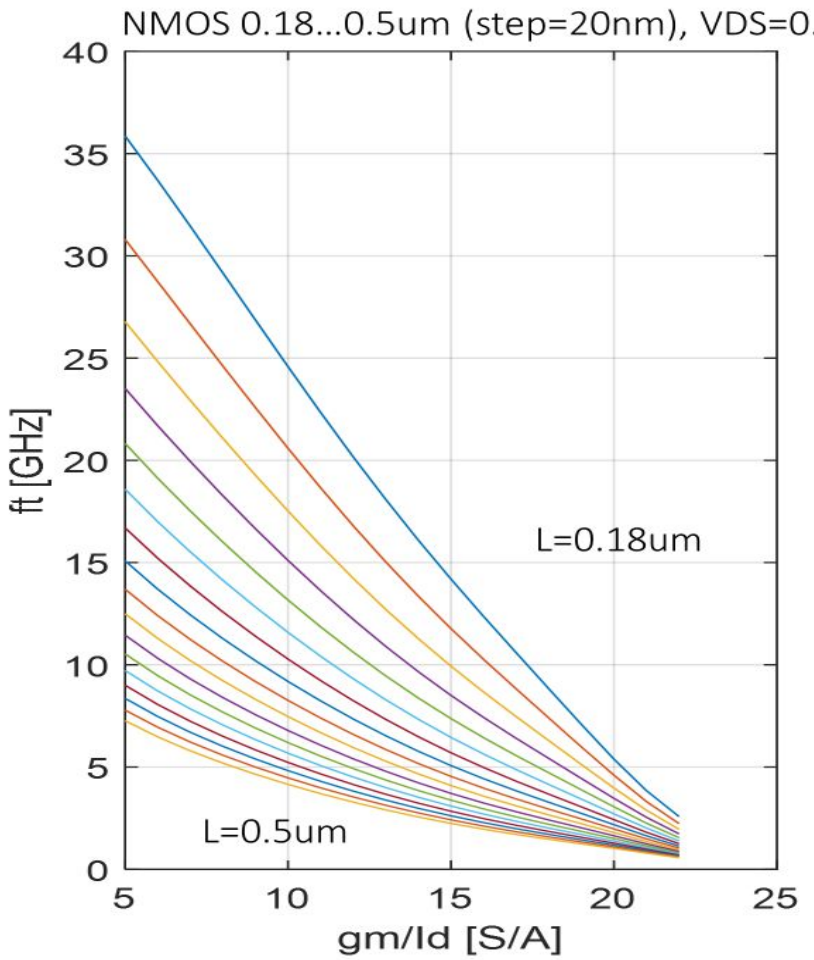
$$V_{gs} = f_\gamma \left(\frac{g_m}{I_D}, L \right)$$

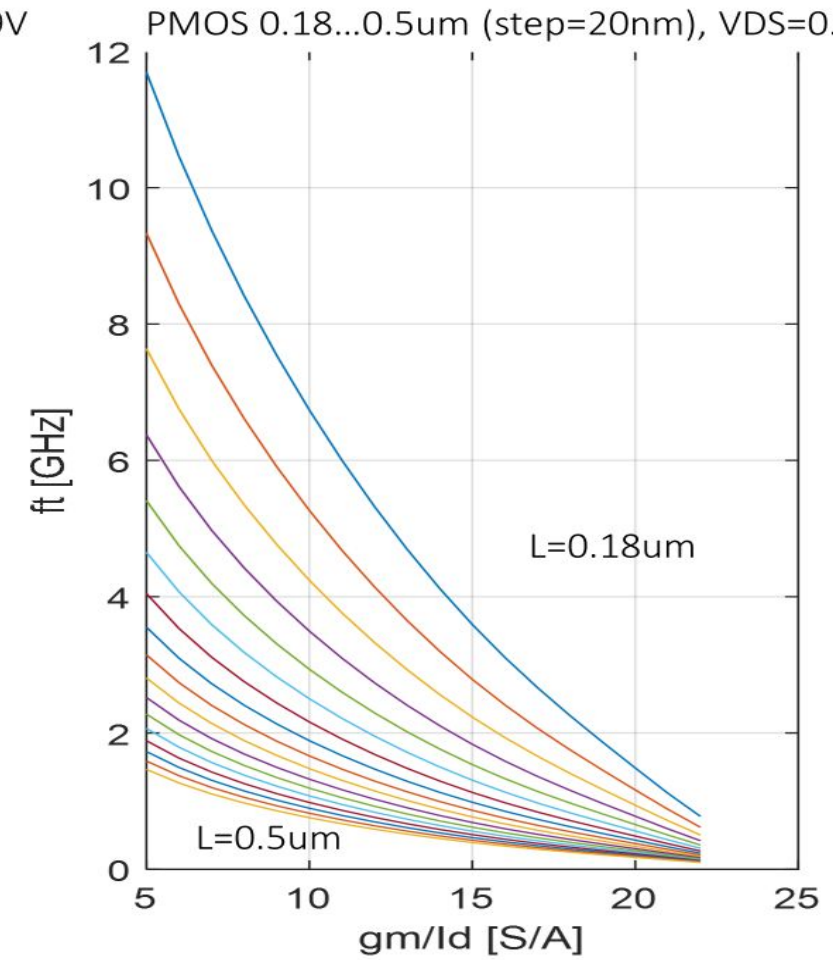
gm/gds = gm*ro → Intrinsic Gain Plots



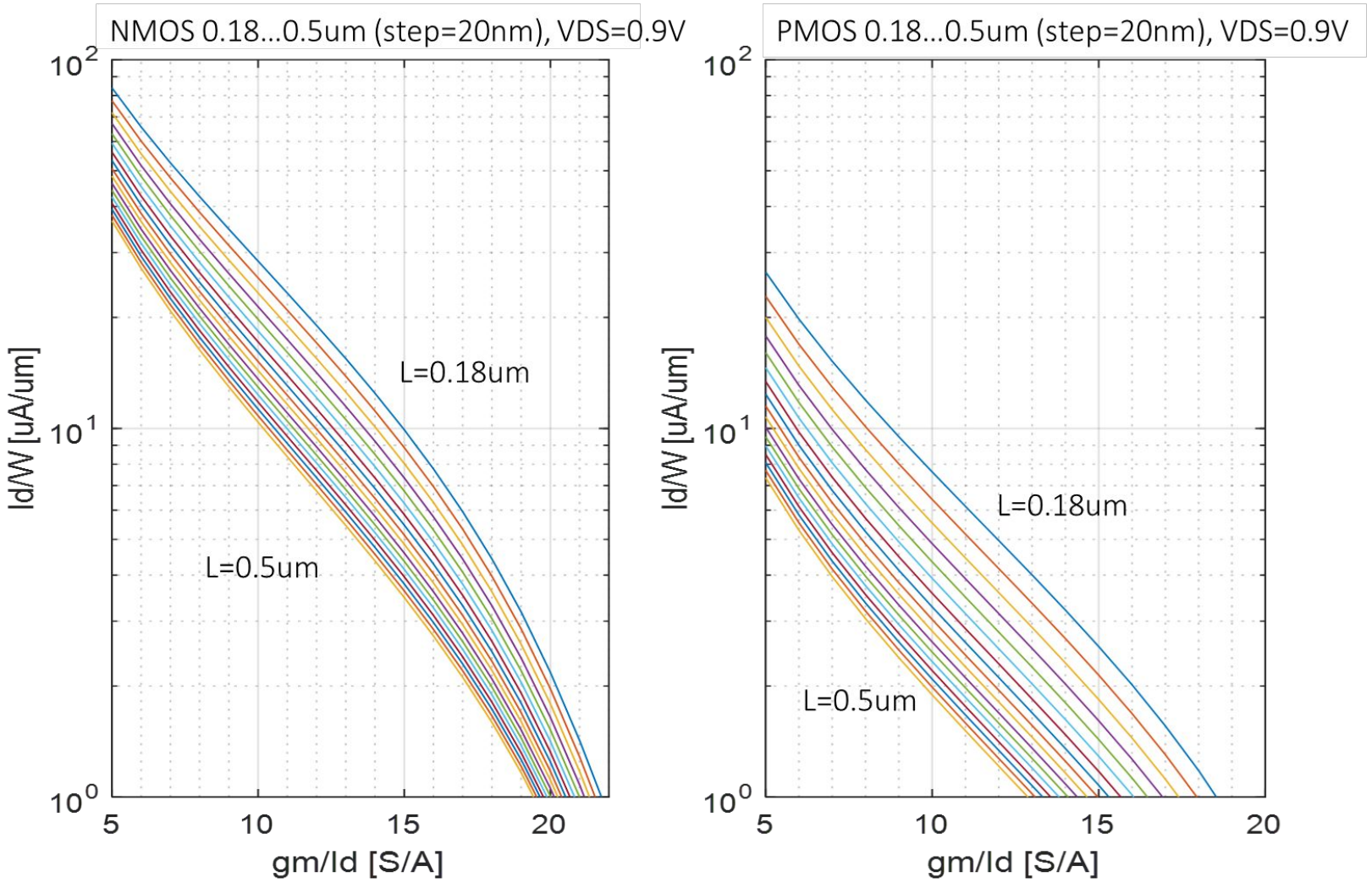


fT = gm/Cgg/2pi → Transit Frequency Plots

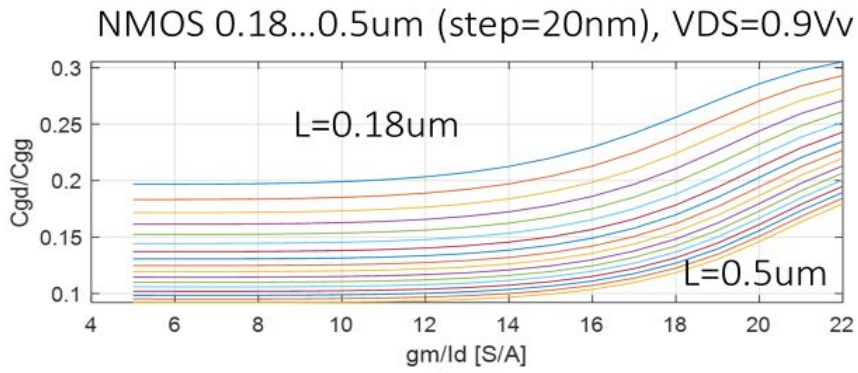


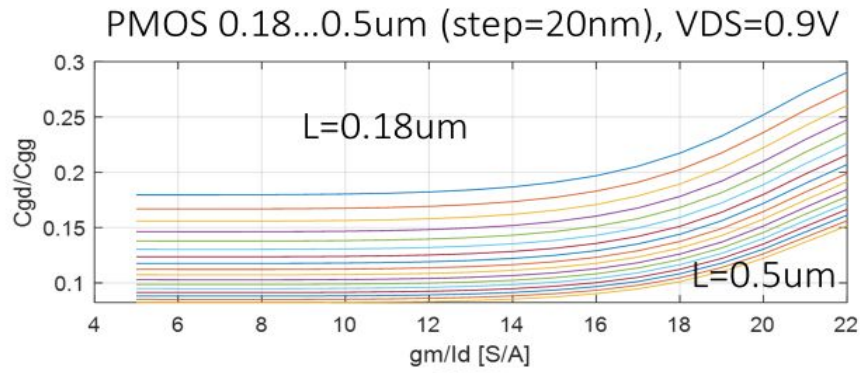


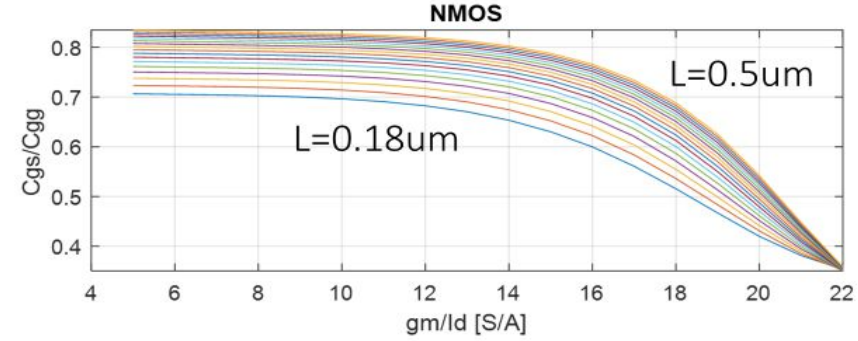
Id/W → Current Density Plots

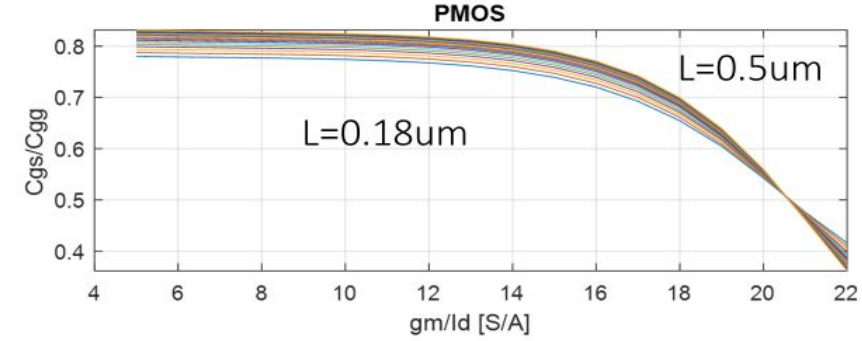


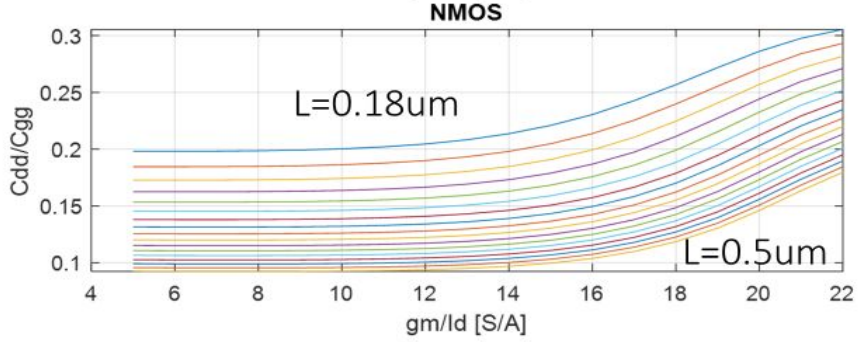
Extrinsic Capacitances ratios

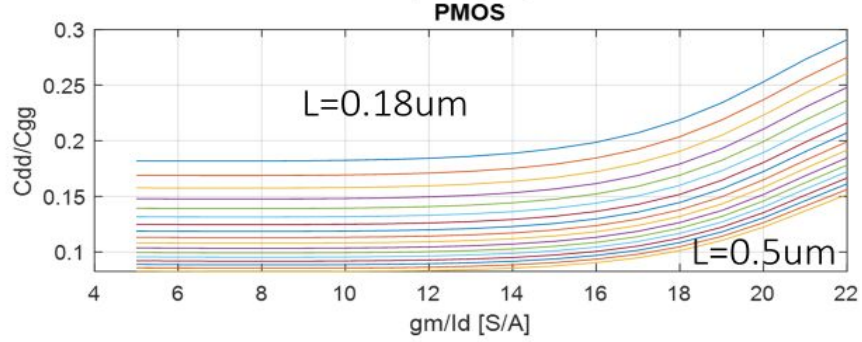








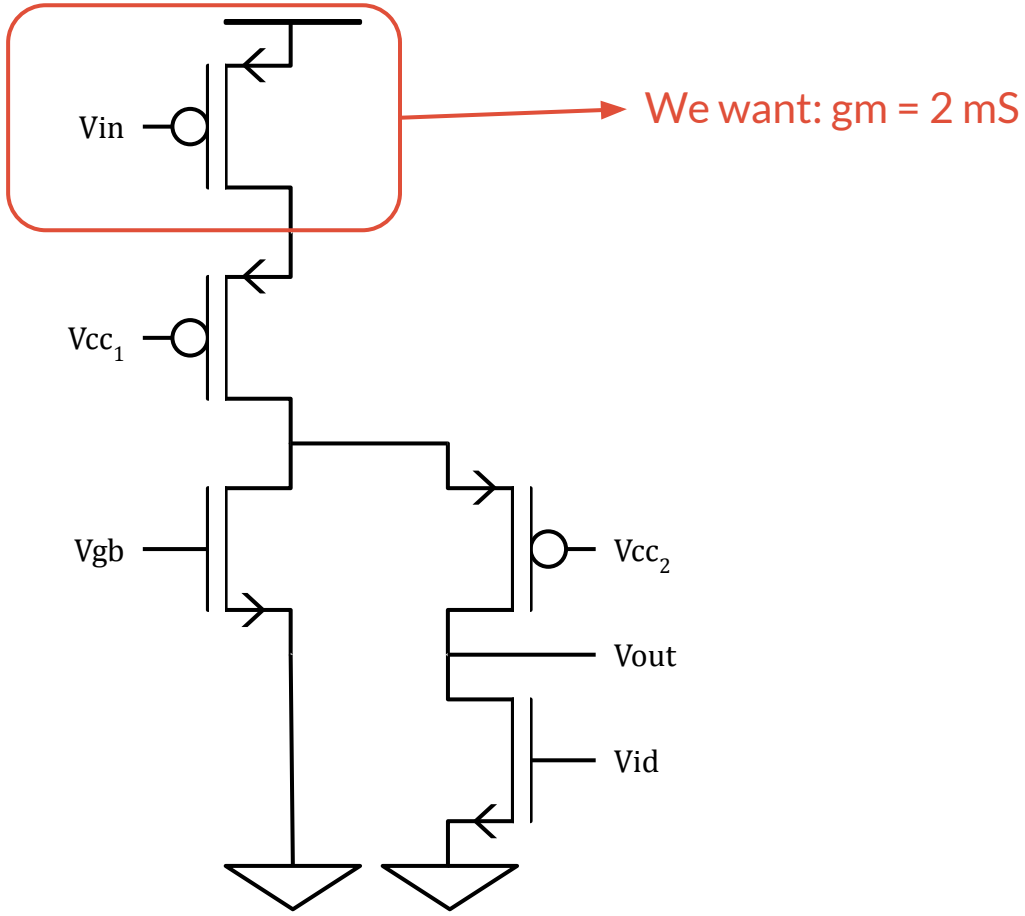




DC Biasing And Sizing Transistors

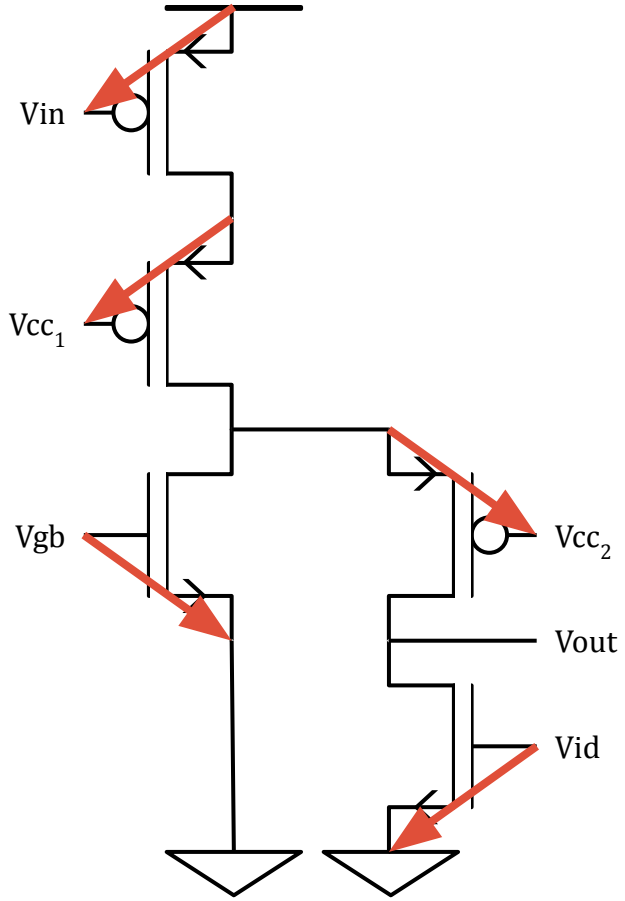
How to size transistors to get a desired gm

Typical situation: We want some gm



Step 1: Obtain gm/Id, L

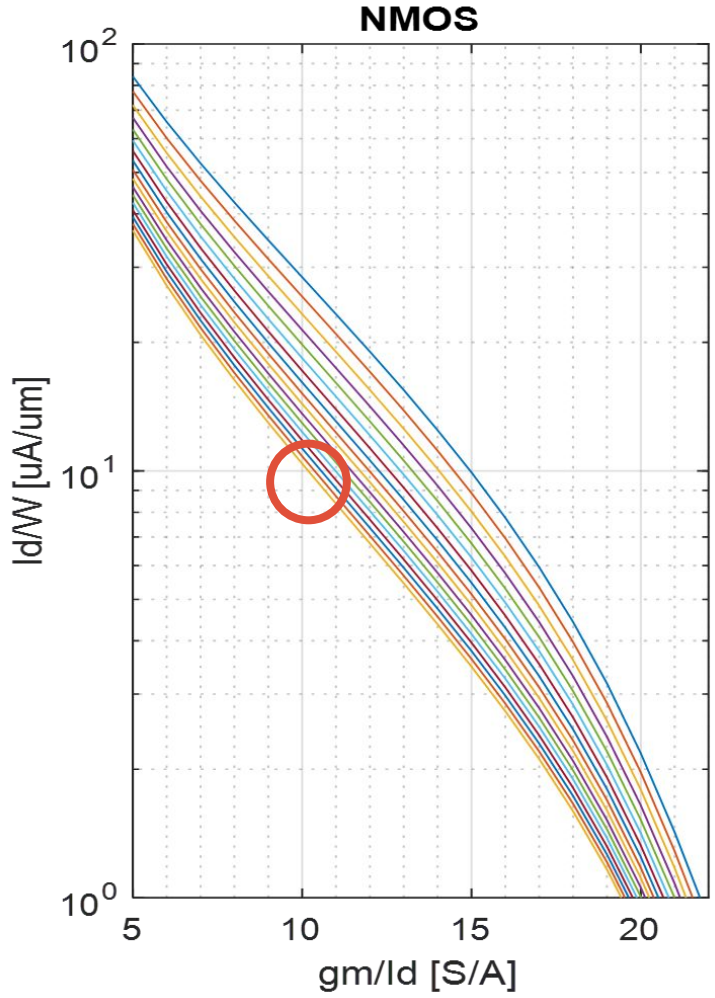
We will cover later how their optimal values can be found from noise and bandwidth considerations.



Step 2: Given gm/Id, we can find the current density, etc

$$\frac{g_m}{I_D}$$

$$\frac{I_D}{W} = f_\alpha\left(\frac{g_m}{I_D}, L\right)$$
$$\frac{g_m}{C_{gg}} = \omega_T = f_\beta\left(\frac{g_m}{I_D}, L\right)$$
$$V_{gs} = f_\gamma\left(\frac{g_m}{I_D}, L\right)$$



Step 3: Given the ratios, we can find transistor widths, etc

$$\frac{g_m}{I_D}$$

$$\frac{I_D}{W} = f_\alpha\left(\frac{g_m}{I_D}, L\right)$$
$$\frac{g_m}{C_{gg}} = \omega_T = f_\beta\left(\frac{g_m}{I_D}, L\right)$$
$$V_{gs} = f_\gamma\left(\frac{g_m}{I_D}, L\right)$$

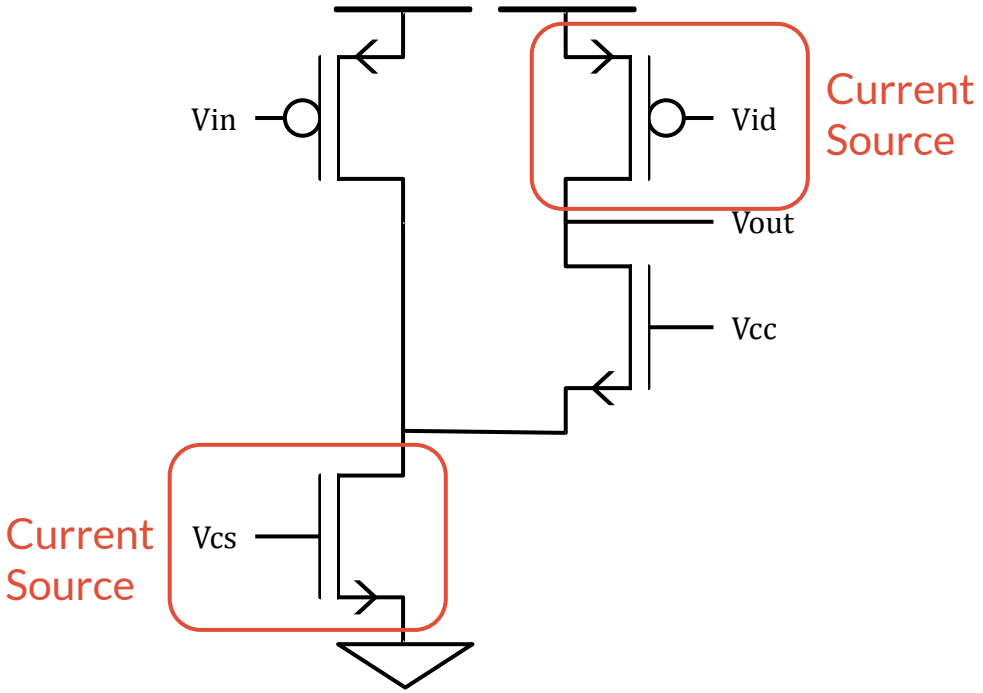
$$I_D = g_m / \frac{g_m}{I_D}$$

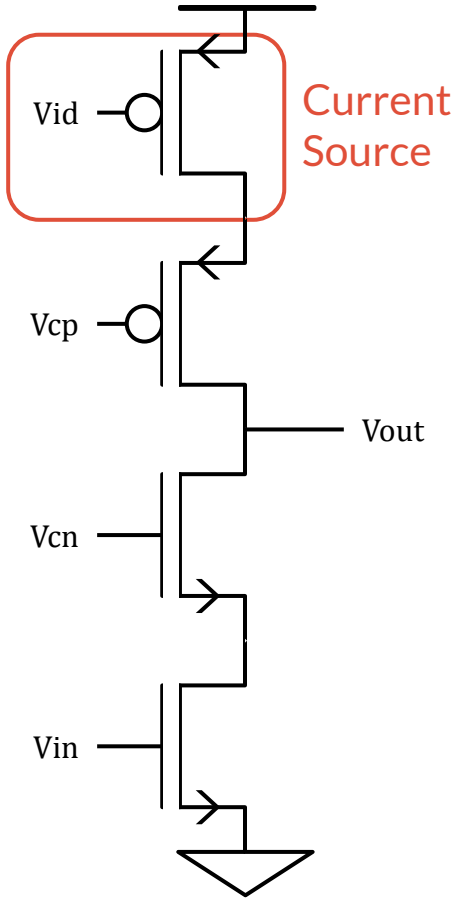
$$W = I_D / \frac{I_D}{W}$$
$$C_{gg} = g_m / \frac{g_m}{C_{gg}}$$

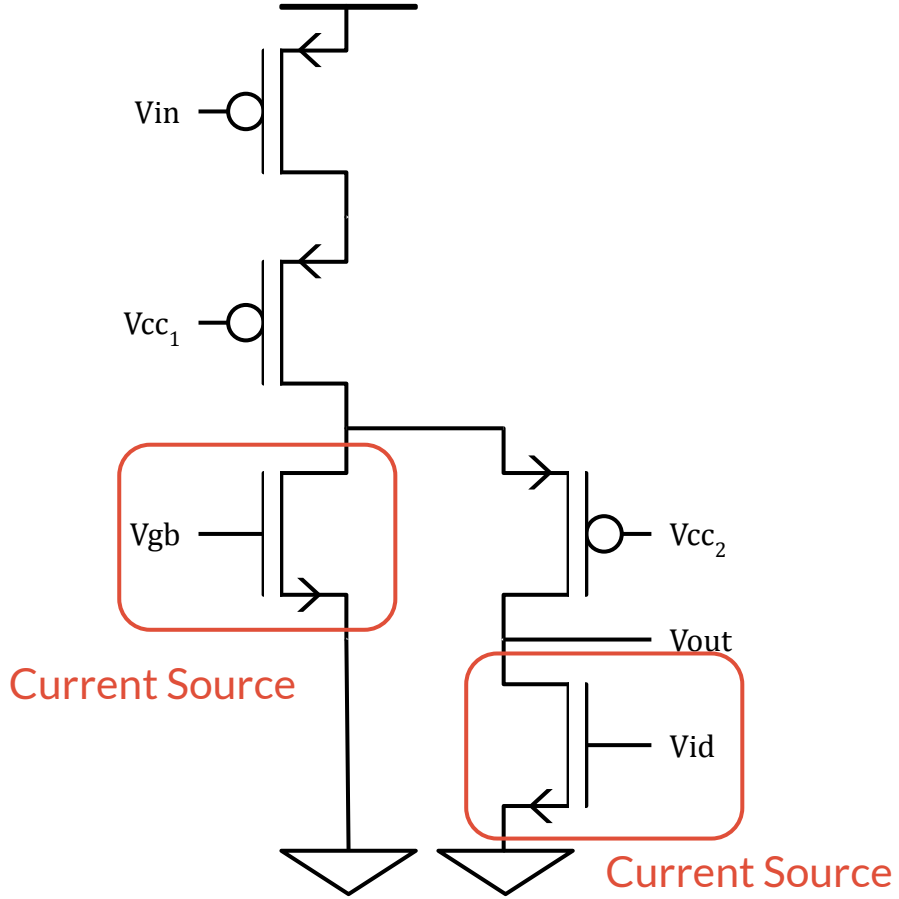
DC Biasing And Sizing Transistors

Current sources

The current sources simply set the desired amount of gm







Intermission

Our first design exercise

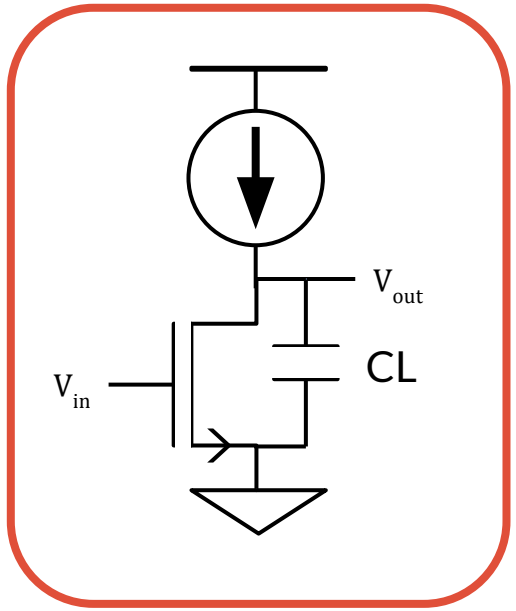
Generic 180nm PDK / 1.8V Supply

No Deep N-Wells: MOSFET body connected to GND/VDD

Task: Designing An Open Loop Intrinsic Amplifier

Part 1: Intrinsic Gain Stage

- Id< 5uA
- CL=250fF
- Vout = 0.9V at DC (see next slide)
- Goals:
  - Gain-Bandwidth Product: >16MHz
  - Maximize Gain

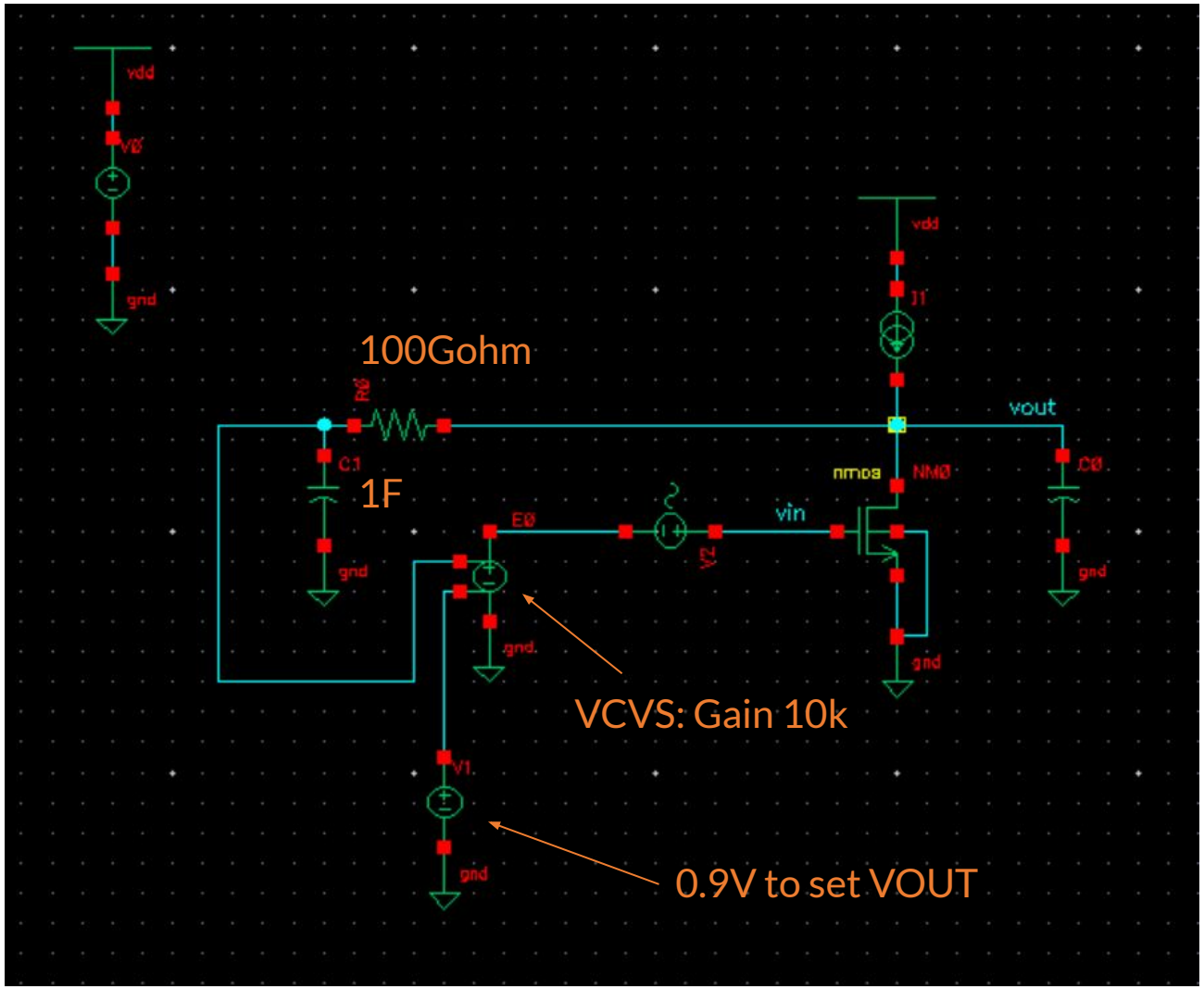


Methodology:

1. By hand: derive gain in terms of gm, gds then derive the expression of the pole and the GBW product
2. Calculate gm to obtain needed GBW
3. Pick an appropriate gm/gds and L to achieve desired gain.
4. Given gm/gds and L, we've fixed gm/Id, fT and Id/W.
5. Using Id/W, find the needed W
6. Run a simulation

Sample Intrinsic Gain Stage Implementation

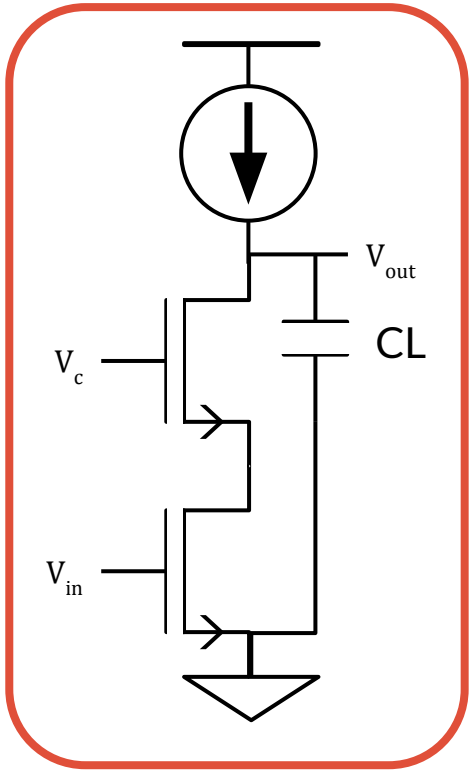
Note: The auxiliary circuit is an ideal op-amp connected to a lowpass filter. The lowpass filter only lets the DC signal through. The op-amp biases the nMOS such that VOUT = 0.9V in DC



Task: Designing An Open Loop Amplifier

Part 2: Cascoded Stage

- Id< 5uA
- CL=250fF
- Vout = 0.9V at DC (see previous slide)
- Goals:
  - Gain-Bandwidth Product: >16MHz
  - Maximize Gain



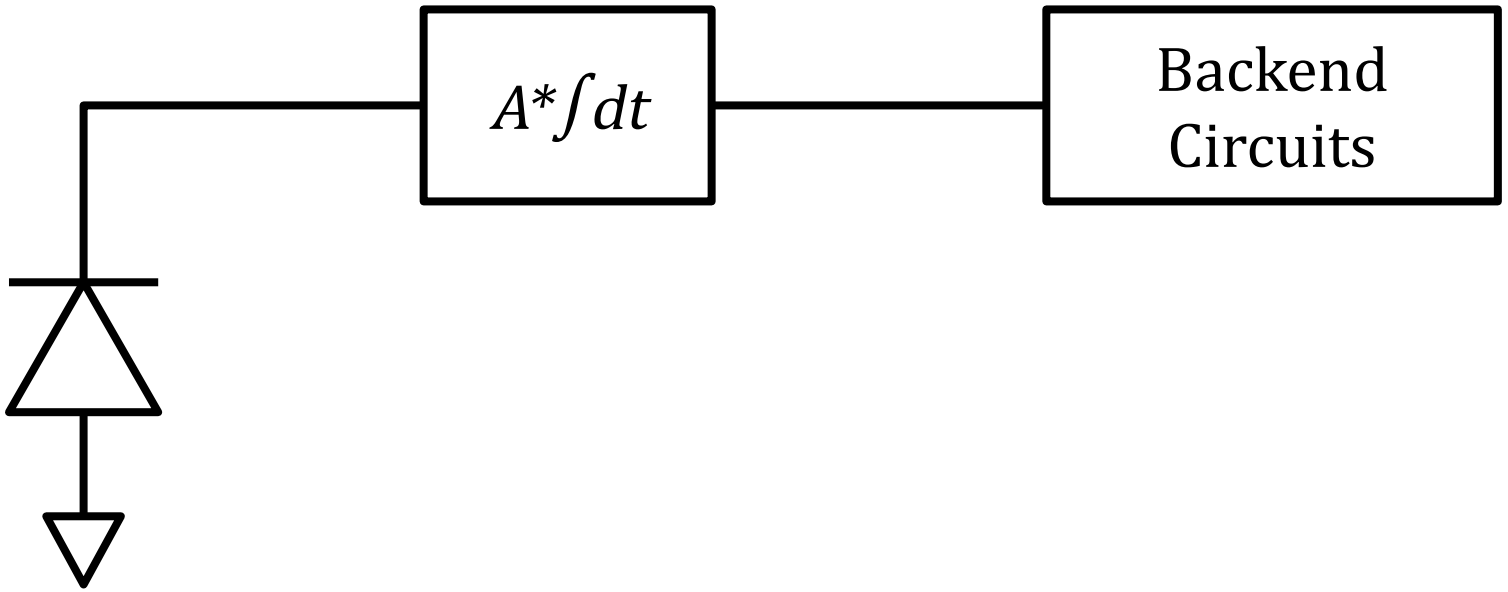
Methodology:

1. Simply add a cascode with the same dimensions of the input transistor
2. Derive the equations
3. See what maximum gain can be achieved
4. Run a simulation. You may need to try different voltages for V_c

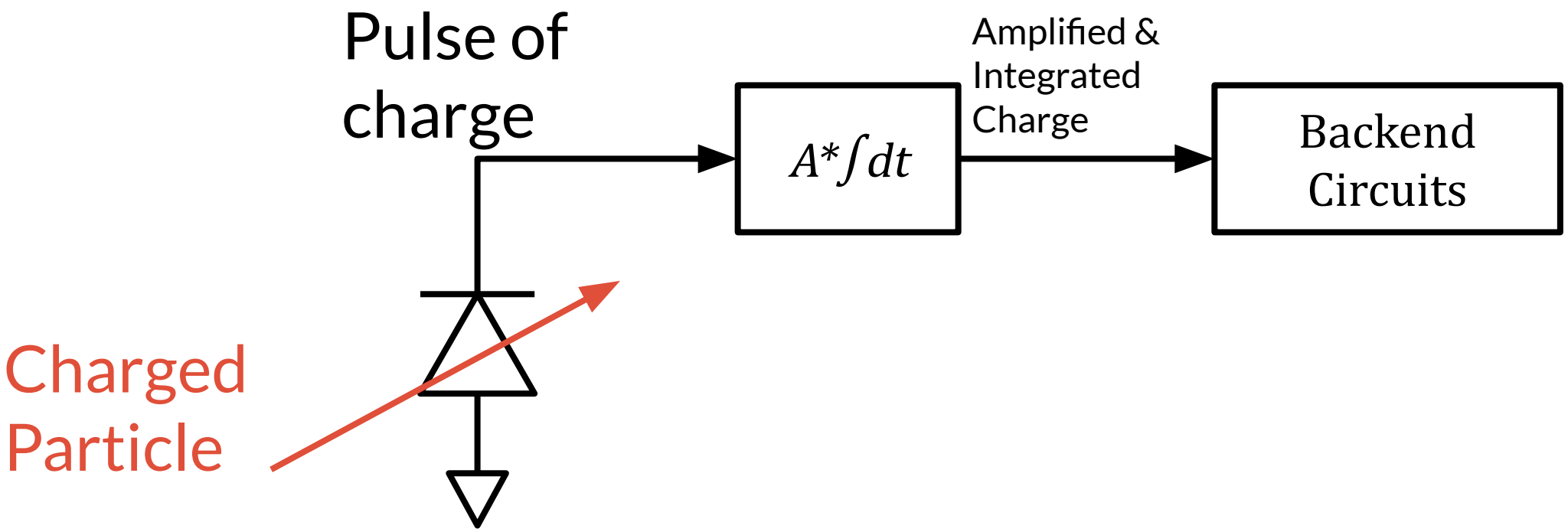
AC Analysis And Feedback

Charge-sensitive amplifiers and diode readouts

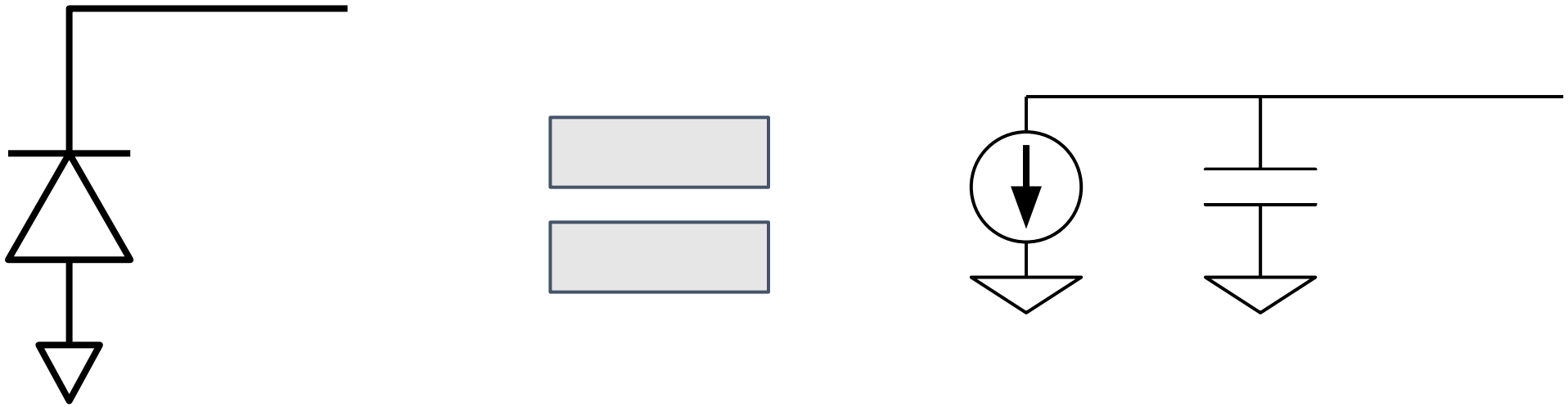
What have we been working towards?



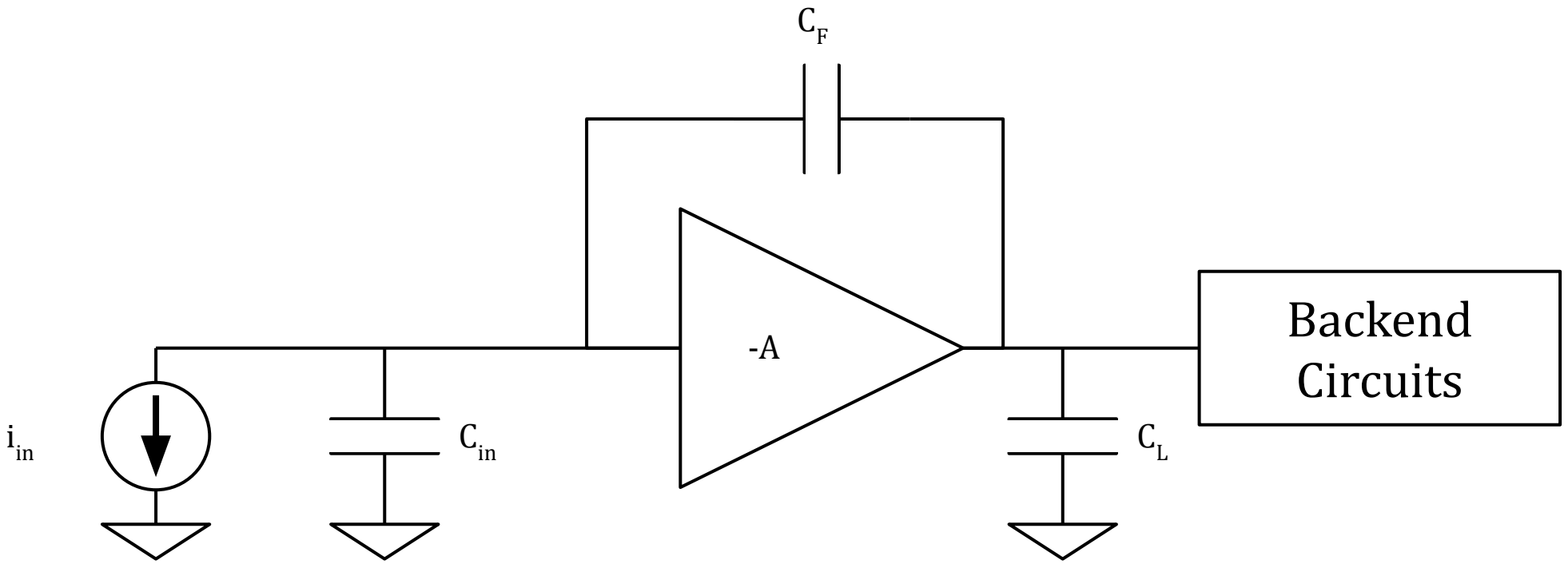
What have we been working towards?



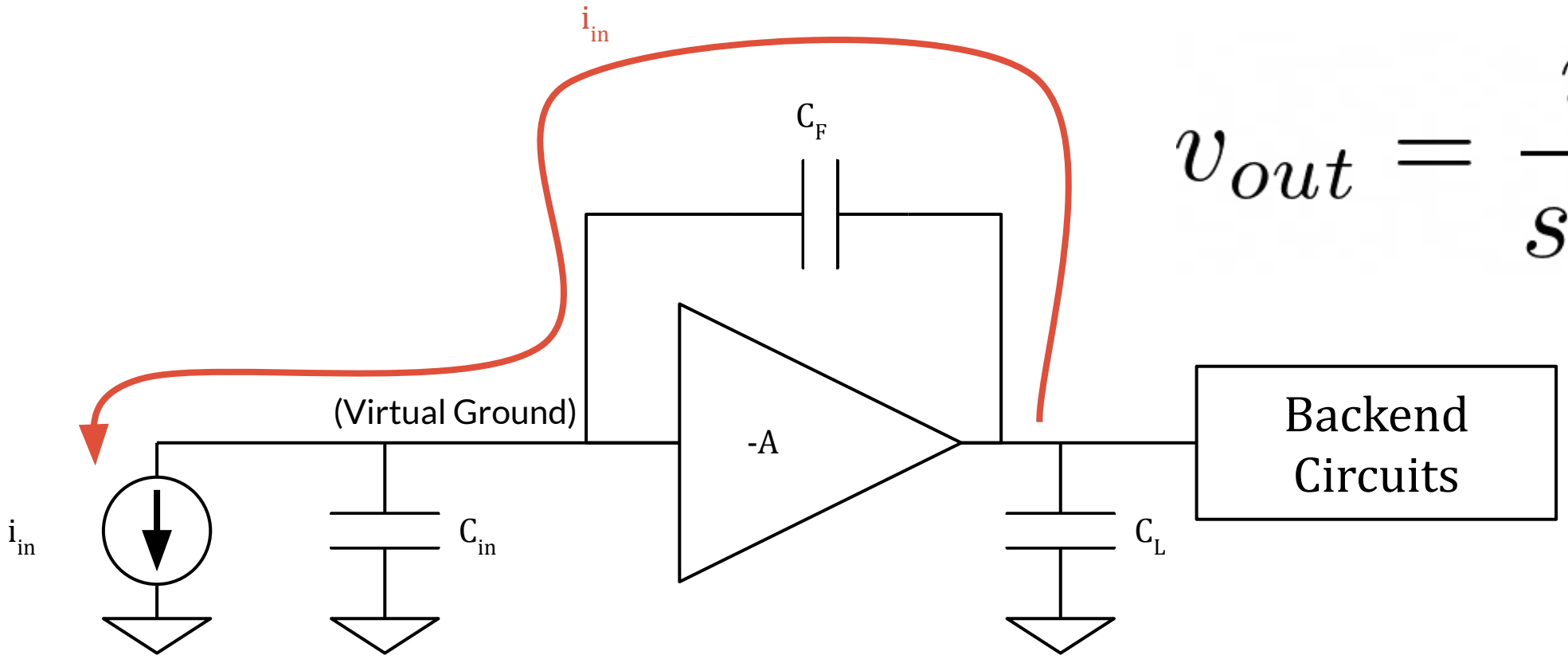
How does a particle sensor look like?



The full Charge-Sensitive Amplifier (CSA) system



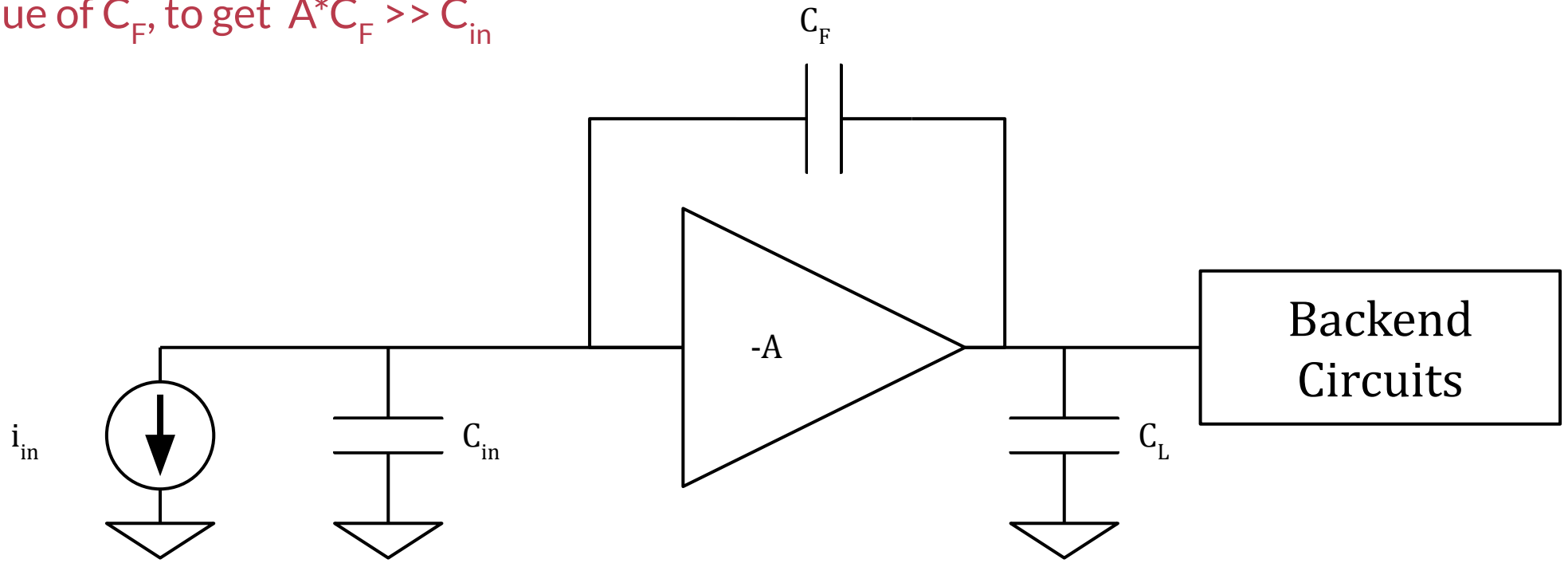
Ideal CSA with A=∞



$$v_{out} = \frac{i_{in}}{sC_F}$$

Note: How much gain is good enough?

For a CSA, the DC loop gain is typically set by C_{in}. We have a current divider between C_{in} and C_F. While we want all current to go into C_F, some of it will go into C_{in}. The amplifier "multiplies" the value of C_F, to get $A^*C_F >> C_{in}$



We are ready to give the full CSA specs

- Diode **Input Capacitance: 100fF**
- Max processing time 7us → **Settling time at ε_d=0.01% <100ns** → Bandwidth > 15MHz
- Max signal 25fC, Max output swing of 1V → **Gain 40mV/fC**
- **Static Error: ε_s < 0.1%**
- **Input-Referred Noise: <150e-**
- Use minimum current consumption (max 12uA)

Dynamic Error: At what fraction of the final output do we consider the input fully settled?

$$\epsilon_s = \frac{L(0)}{1 + L(0)}$$

$$f_{3dB} = \frac{1}{2\pi\tau} = \frac{\ln(1/\epsilon_d)}{2\pi t_S}$$

Static Error: How far does the closed-loop gain deviate from just an ideal C_F at DC?

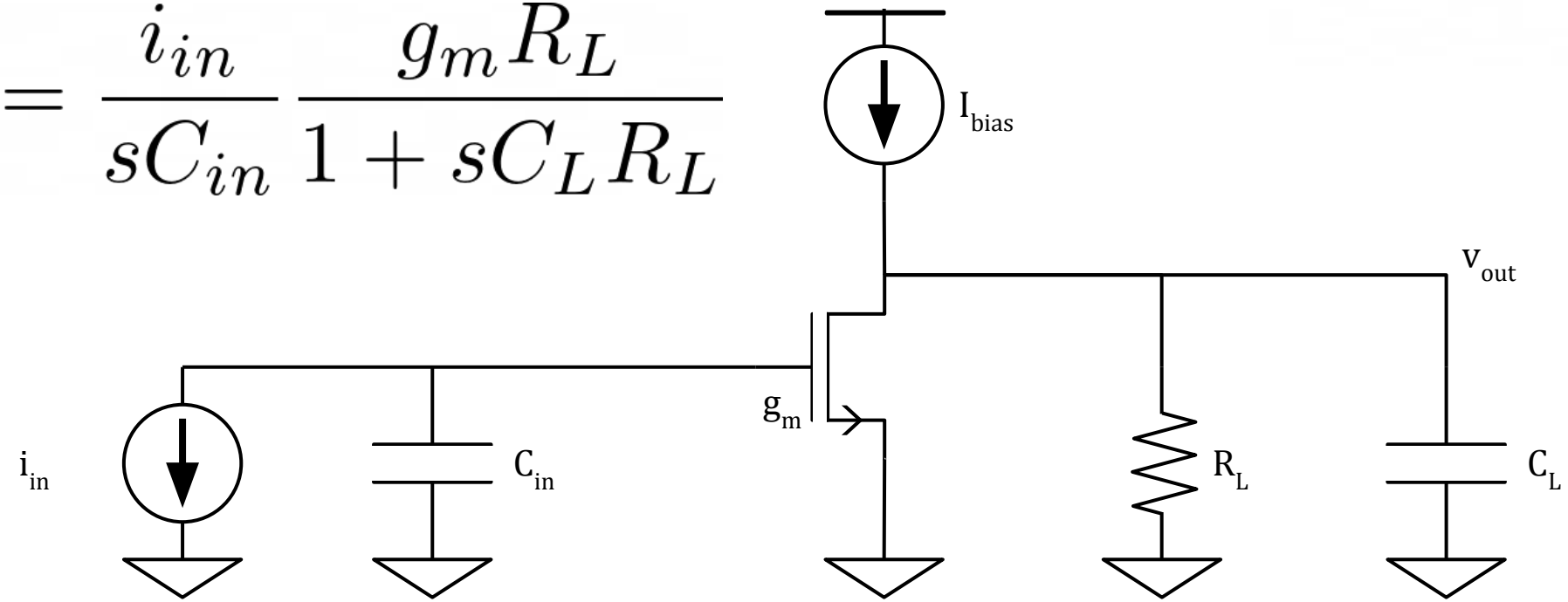
AC Analysis And Feedback

The open-loop intrinsic gain stage

The open-loop intrinsic gain stage

$$v_{out} = \frac{i_{in}}{sC_{in}} \frac{g_m R_L}{1 + sC_L R_L}$$

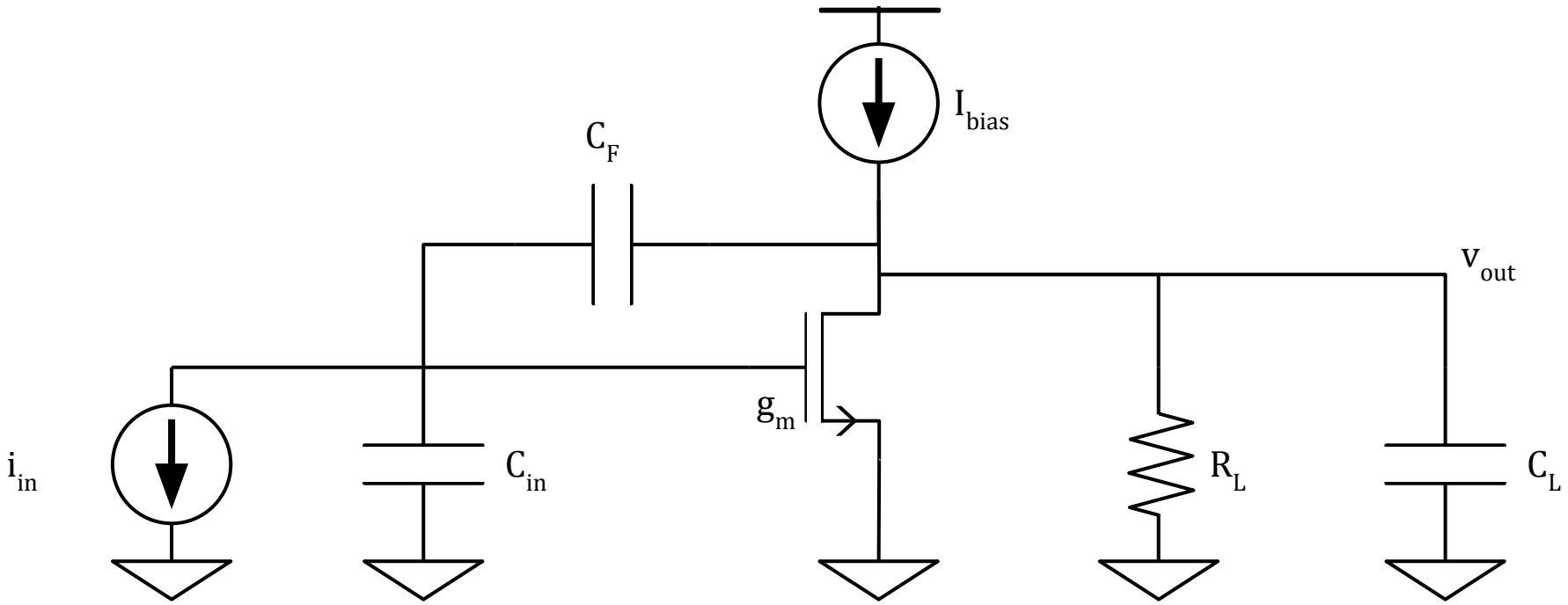
$$GBW = \omega_u \approx \frac{g_m}{C_L}$$



AC Analysis And Feedback

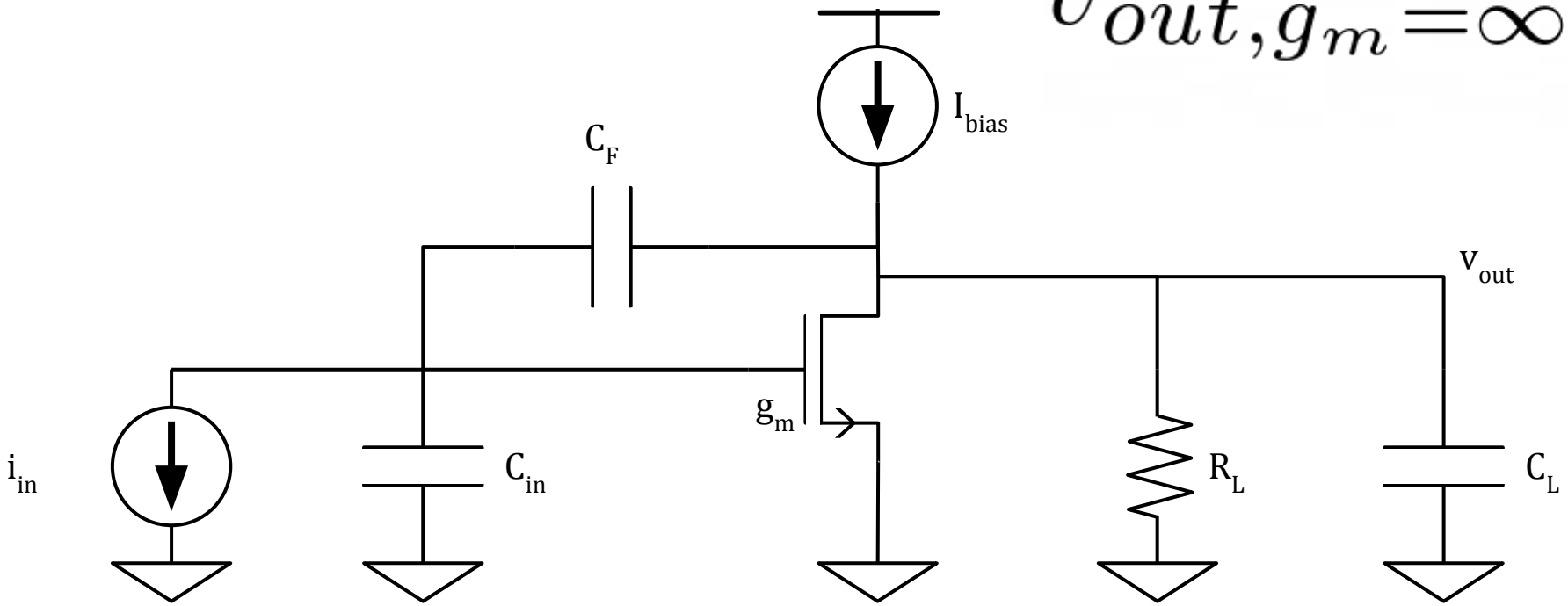
Adding capacitive feedback

Single-stage CSA



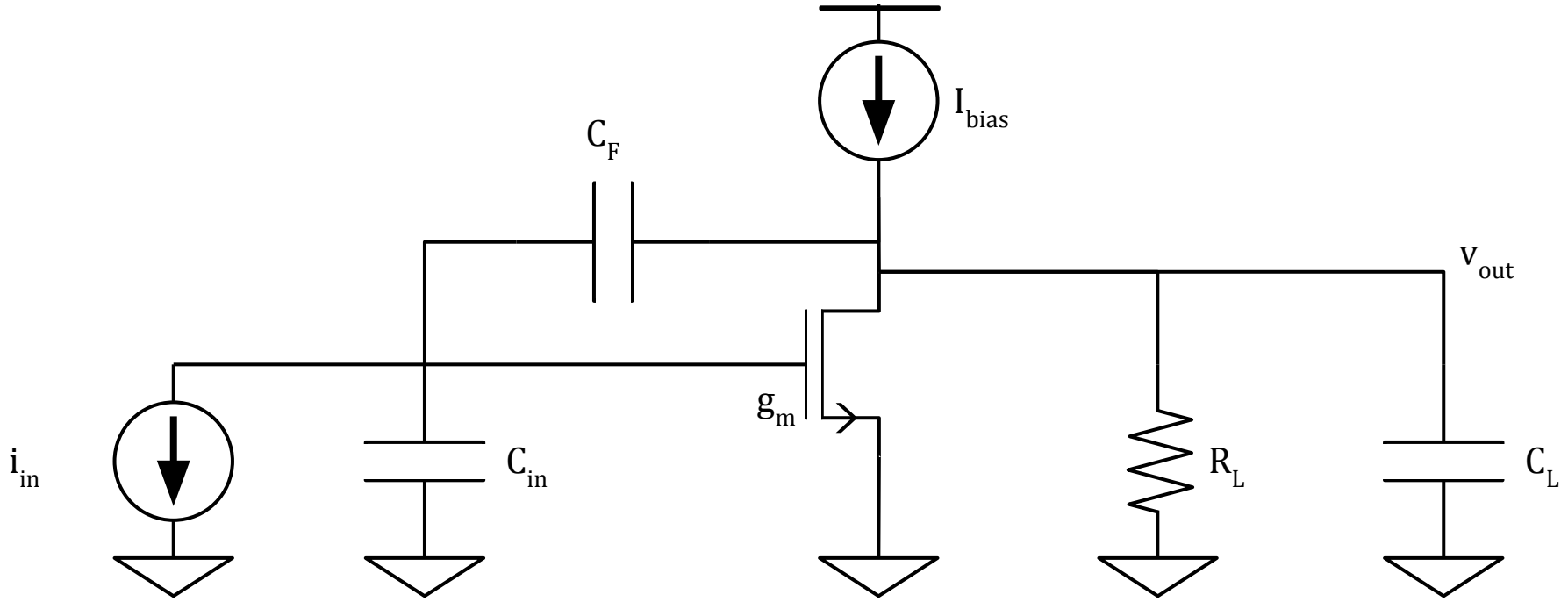
Single-stage CSA: Ideal Gain

$$v_{out,g_m=\infty} = \frac{i_{in}}{sC_{in}}$$



Single-stage CSA: The key formula

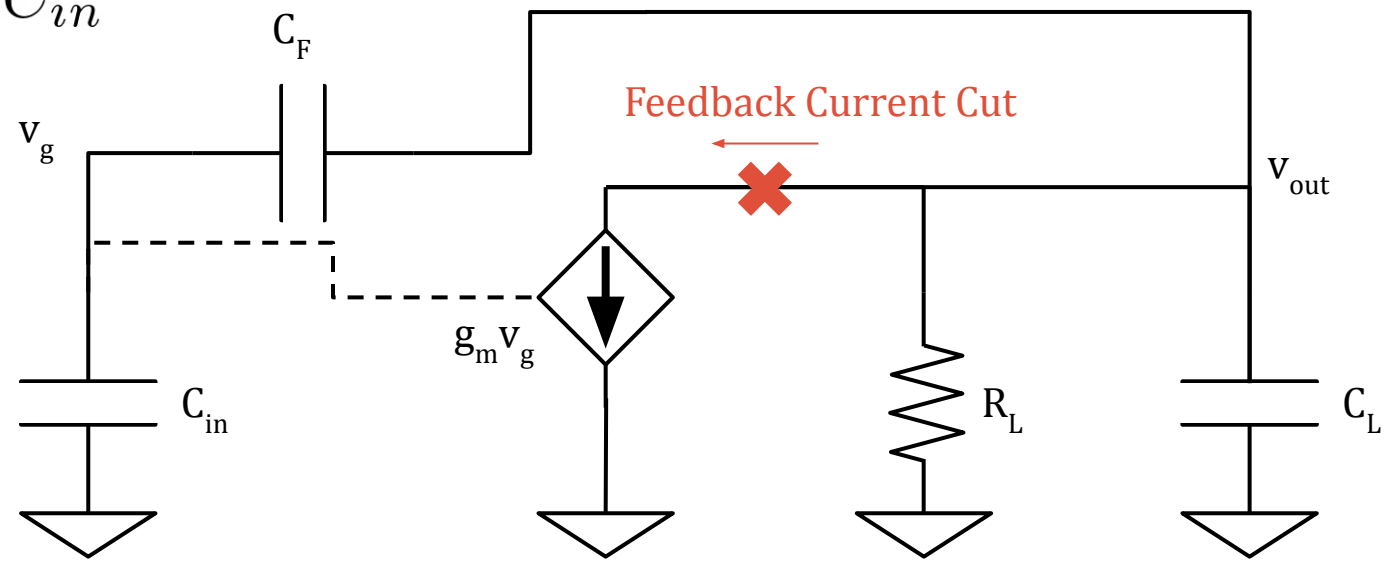
$$v_{out} \approx v_{out,g_m=\infty} \frac{L(s)}{1+L(s)} = \frac{i_{in}}{sC_F} \frac{L(s)}{1+L(s)}$$



Single-stage CSA: Loop gain

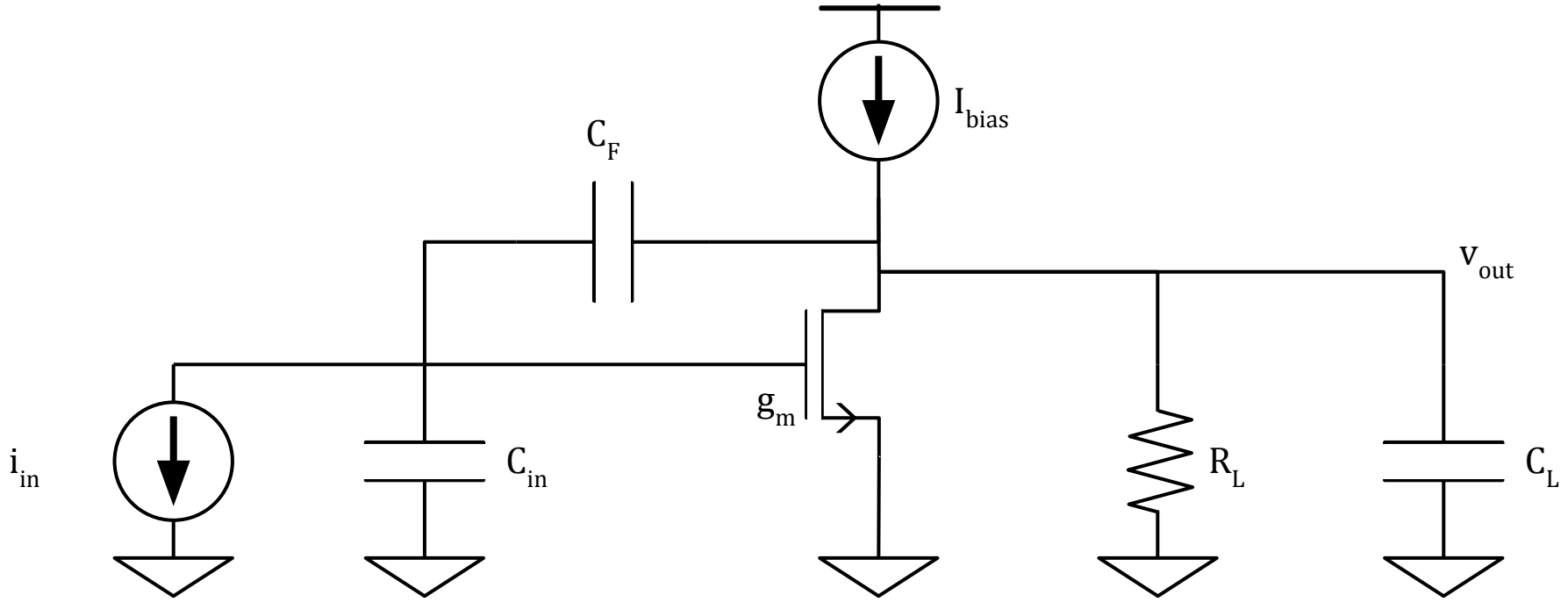
$$L(s) = \frac{R_L}{1 + sR_L C_{Ltot}} \frac{C_F}{C_{in} + C_F} g_m$$

$$C_{Ltot} = C_L + \frac{C_F C_{in}}{C_F + C_{in}}$$



Single-stage CSA: The key formula

$$v_{out} \approx v_{out,g_m=\infty} \frac{L(s)}{1+L(s)} = \frac{i_{in}}{sC_F} \frac{L(s)}{1+L(s)}$$



Single-stage CSA: The key formula

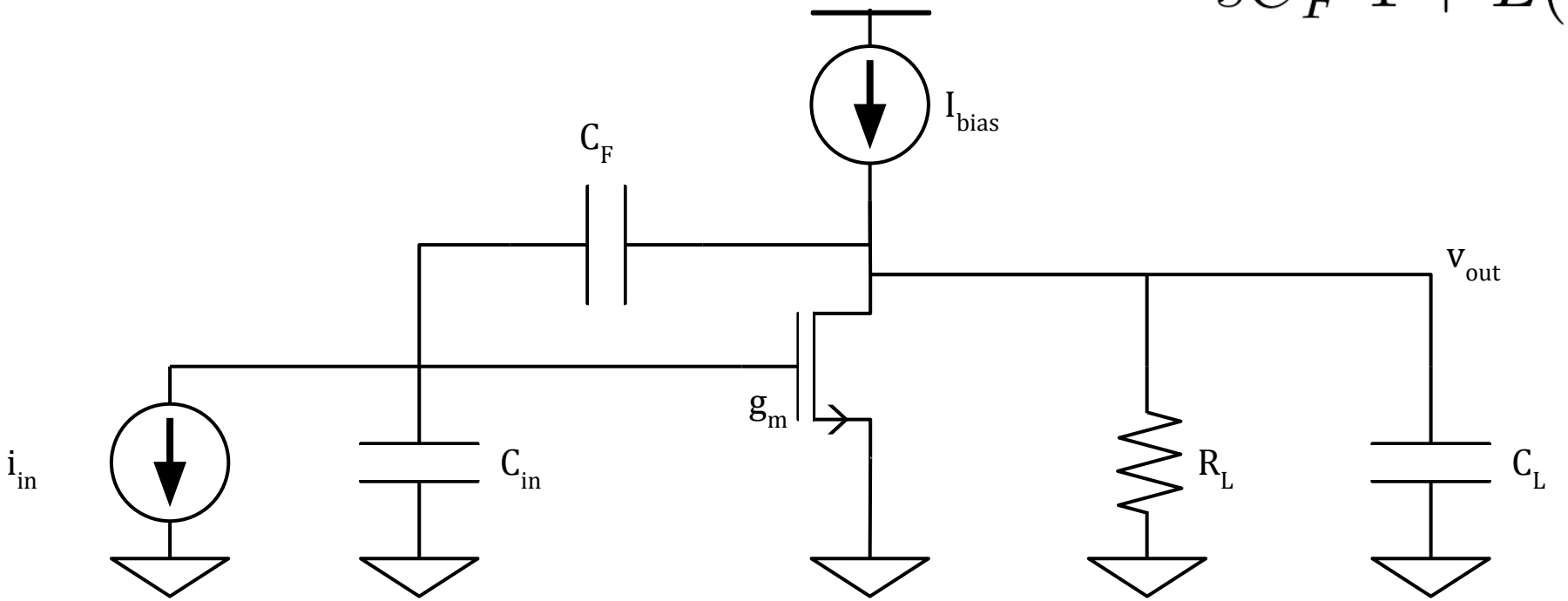
$$L(s) = \frac{L_0}{1 + s/\omega_L}$$

$$\frac{L(s)}{1 + L(s)} = \frac{L_0}{1 + L_0} \frac{1}{1 + \frac{s}{(1+L_0)\omega_L}}$$

Bandwidth of the closed-loop system is the bandwidth of the open-loop gain times the DC gain of the open-loop. (For single-pole amplifier)

Single-stage CSA

$$v_{out} \approx \frac{i_{in}}{sC_F} \frac{L(0)}{1+L(0)} \frac{1}{1+\frac{s}{L(0)\omega_L}}$$

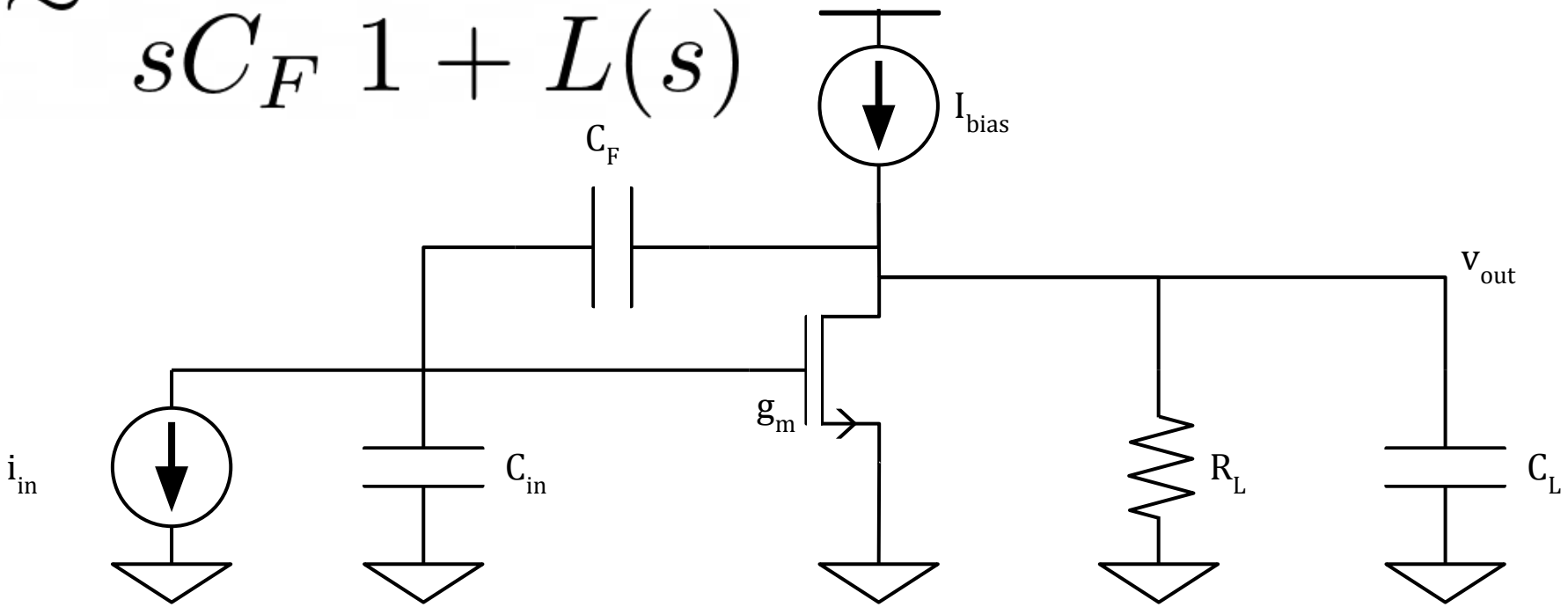


AC Analysis And Feedback

Working with multi-stage amplifiers

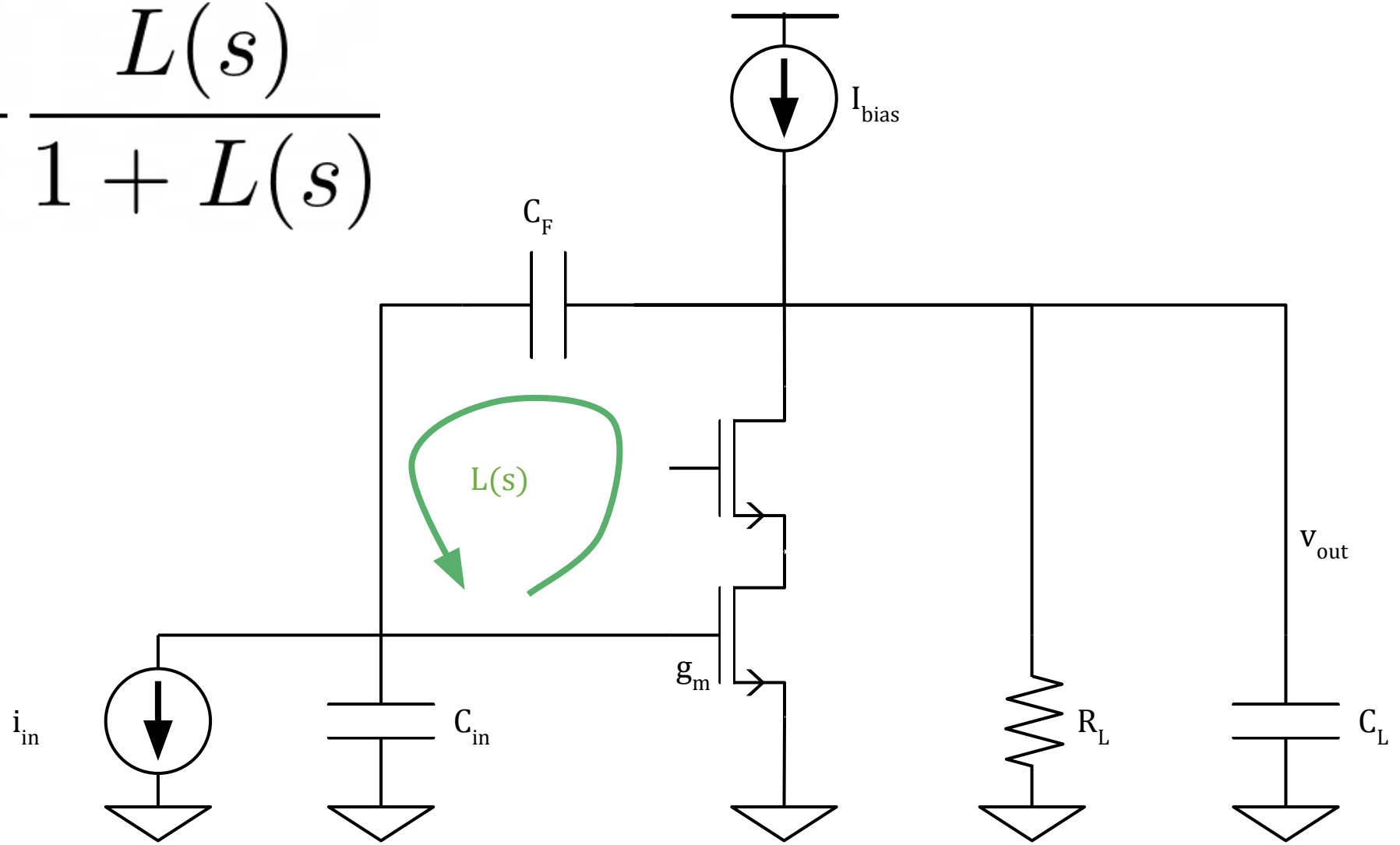
Single-stage CSA

$$v_{out} \approx \frac{i_{in}}{sC_F} \frac{L(s)}{1 + L(s)}$$



The same formula hold for multiple stages

$$v_{out} \approx \frac{i_{in}}{sC_F} \frac{L(s)}{1+L(s)}$$



How to estimate the closed loop bandwidth

Review of single-pole feedback

For a single pole system, we had:

$$L(s) = \frac{L_0}{1 + s/\omega_L} \qquad \frac{L(s)}{1+L(s)} = \frac{L_0}{1+L_0}\frac{1}{1+\frac{s}{(1+L_0)\omega_L}}$$

$$\omega_{3dB,closed\ loop} = (1 + L_0)\omega_L$$

We note: $|L(\omega_u)| = 1$ For: $\omega_u \approx \omega_L L_0$

Thus: $\omega_{3dB,closed\ loop} \approx \omega_{unity\ gain,open\ loop}$

How to estimate the closed loop bandwidth

A general approach

For ANY type of feedback system, we may write:

$$|L(\omega_u)| = 1$$

$$\omega_{3dB,closed\ loop} \approx \omega_{unity\ gain,open\ loop}$$

It's pretty accurate! See comparison table assuming two-pole system with different Qs:

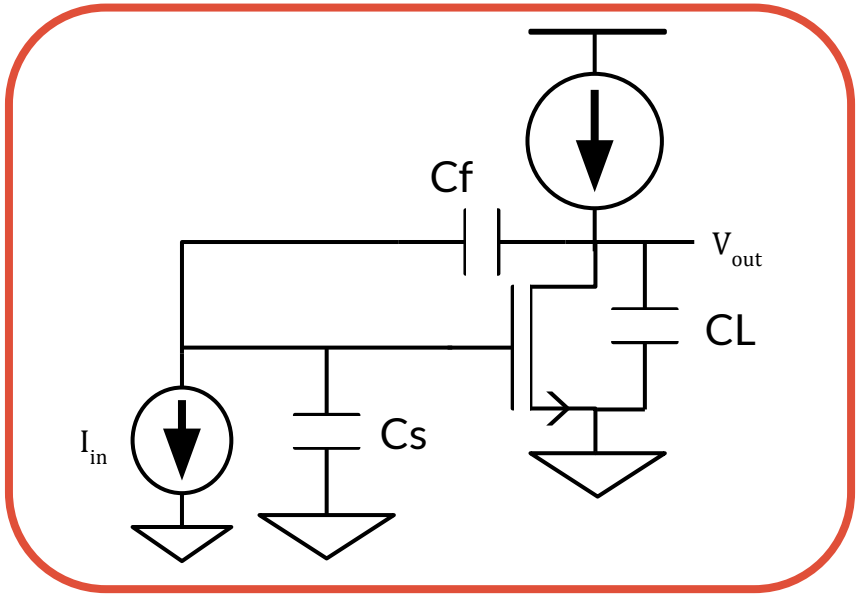
Q = 0.4	
DC Open-Loop Gain L_0	Ratio ω_{3dB}/ω_u
10	1.6312
100	1.5595
1000	1.5576
10000	1.5556
100000	1.5549

Q = 1	
DC Open-Loop Gain L_0	Ratio ω_{3dB}/ω_u
10	1.5666
100	1.5539
1000	1.5569
10000	1.5556
100000	1.5549

Task: Designing intrinsic CSA Amplifier

Part 3: Intrinsic Gain Stage with feedback

- Id< 12uA
- Cs=100fF
- CL=250fF
- Max signal 25fC / Max signal output swing 1V
  - Cf = 25fC/1V
- Size Cgs=0.1(Cf+Cs)
- Goals:
  - Gain-Bandwidth Product: >16MHz
  - Maximize Gain
  - Determine what is the minimum static error you can reach



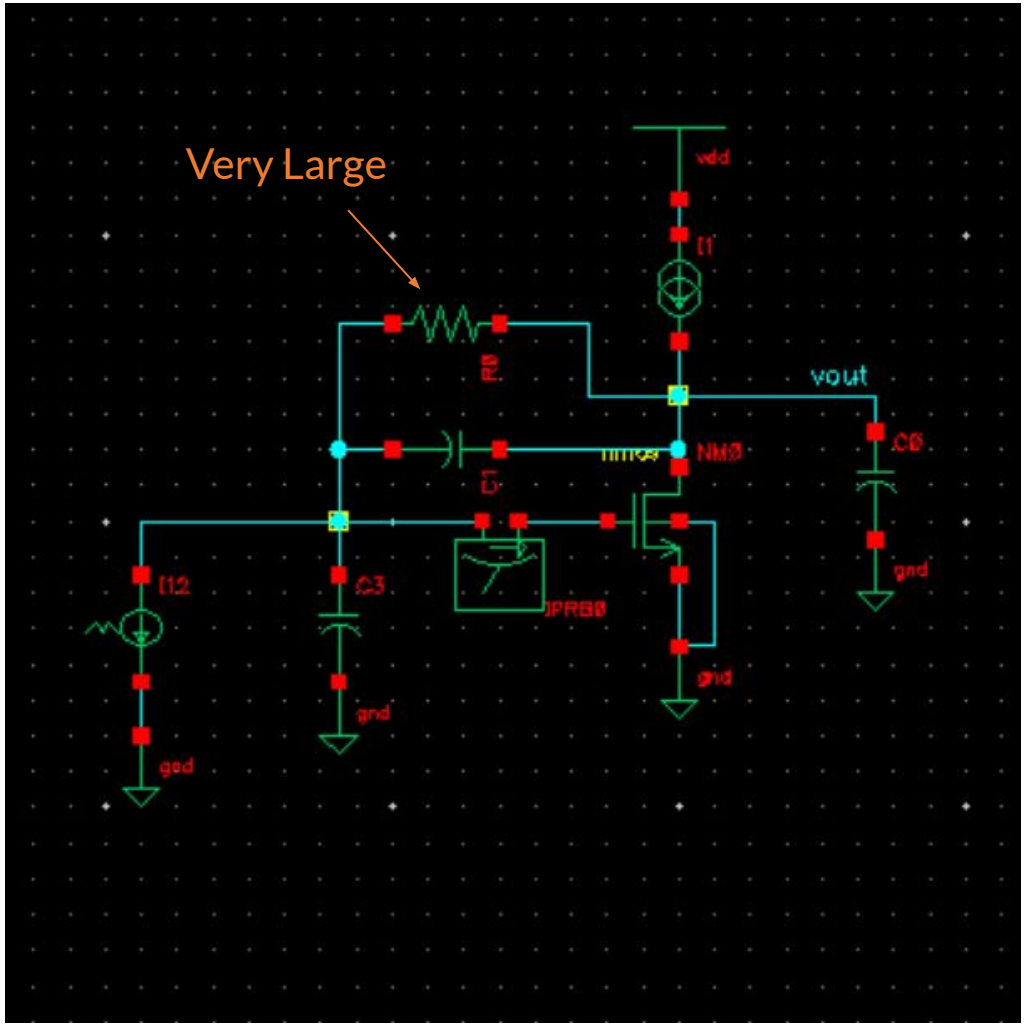
Methodology:

1. By hand: derive Loop gain in terms of gm, gds then derive the expression of the pole and the GBW product
2. Calculate the minimum gm then pick a value of gm/Id compatible with power constraints.
3. Pick an appropriate L to achieve maximum gain.
4. Given gm/Id and L, we've fixed, fT and Id/W.
5. Using Id/W, find the needed W.
6. Run a simulation (check stability)

$$\epsilon_s = \frac{L(0)}{1 + L(0)}$$

Sample Implementation

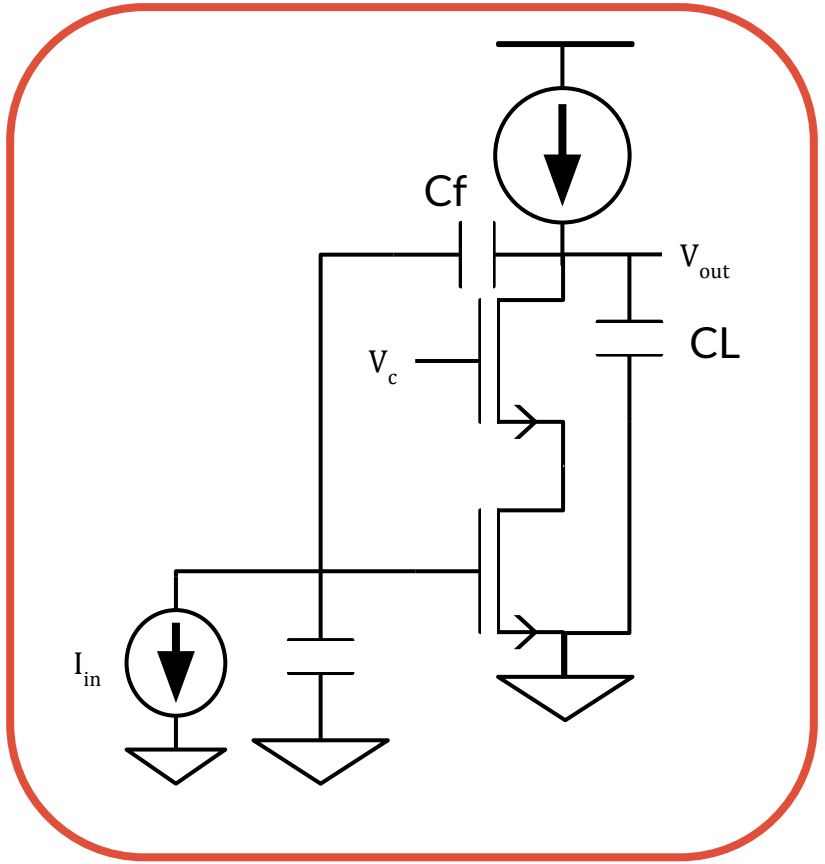
Feedback resistor used to set DC bias only



Task: Designing a CSA Amplifier (ideal load)

Part 4: Cascoded Stage

- Id< 12uA
- Cs=100fF
- CL=250fF
- Max signal 25fC / Max signal output swing 1V
  - Cf = 25fC/1V
- Size Cgs=0.1(Cf+Cs)
- Goals:
  - Gain-Bandwidth Product: >16MHz
  - Determine what is the minimum static error you can reach



Methodology:

- Simply add a cascode with the same dimensions of the input transistor
- Derive the equations
- Run a simulation (check stability)

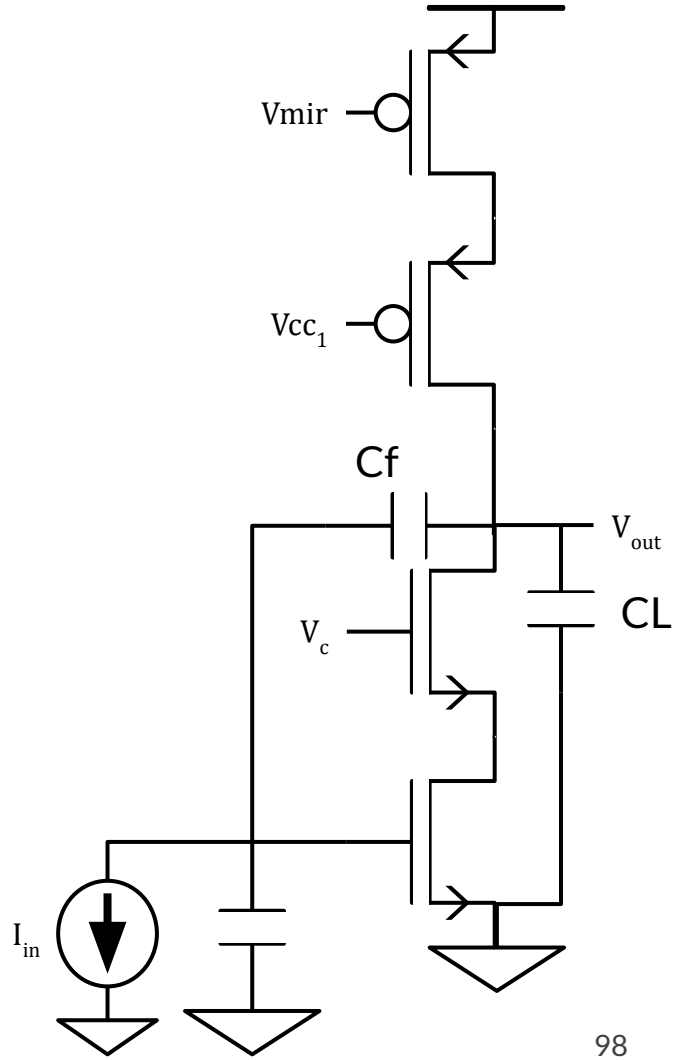
Task: Designing a CSA Amplifier (active load)

Part 5: Cascoded Stage

- Id< 12uA
- Cs=100fF
- CL=250fF
- Max signal 25fC / Max signal output swing 1V
  - Cf = 25fC/1V
- Size Cgs=0.1(Cf+Cs)
- Goals:
  - Gain-Bandwidth Product: >16MHz
  - Verify that the Static error below is below 0.1%

Methodology:

- Simply add two cascode pmos (for simplicity use the same sizes of the nmos branch and mirror the current in them.
- Derive the equation for the closed loop gain
- Run a simulation (check stability)



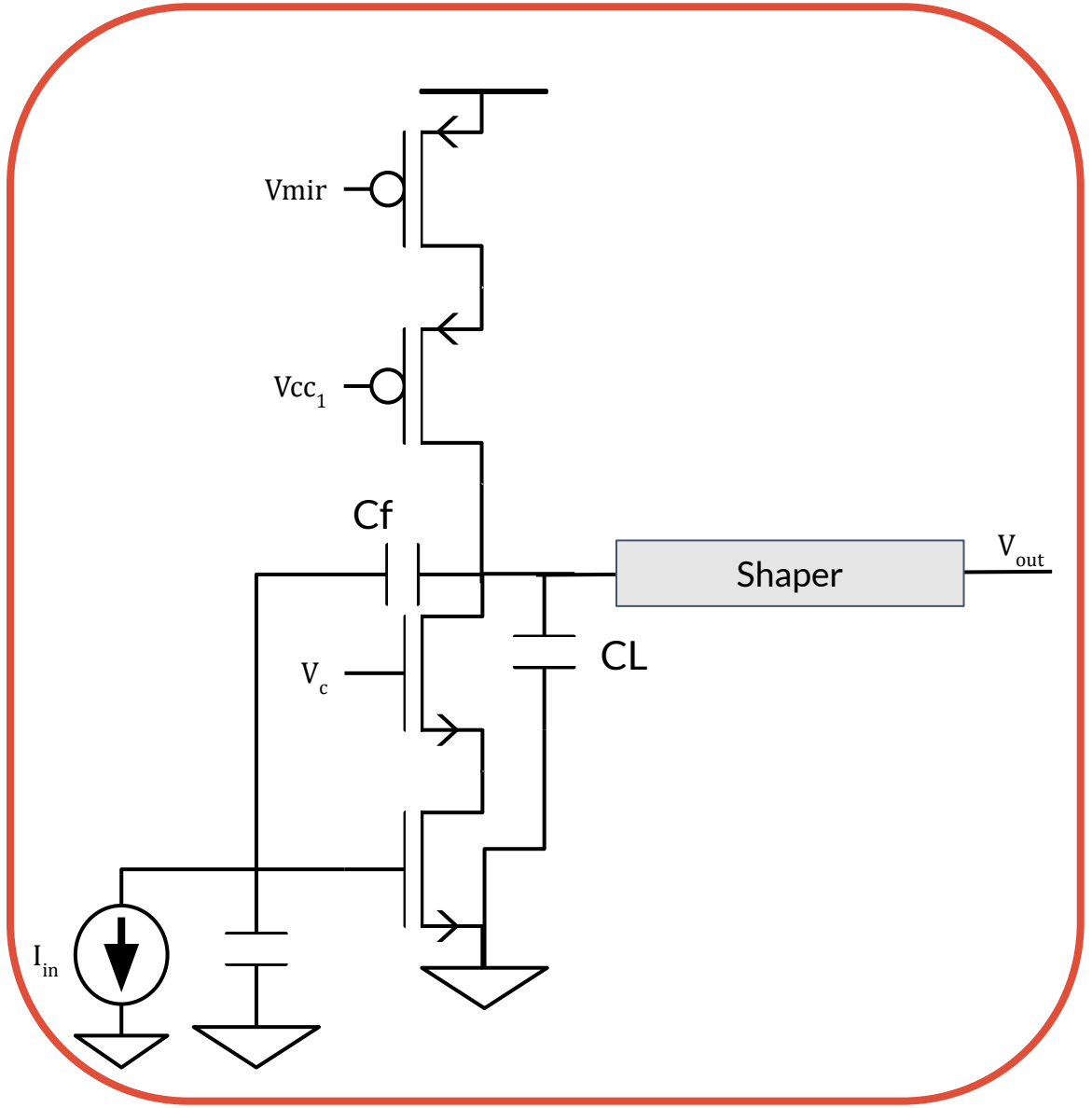
Task: Designing a CSA +Shaper

Part 6: CSA+Shaper

1. What Shaper time constant do we need to reach an ENC < 150e-?
2. Does the waveform return to 0 within 7us?

Methodology:

3. Use the ideal shaper.
4. Plot the total output noise r.m.s.
5. Calculate the ENC
6. Vary the shaper time constant until ENC <150e-



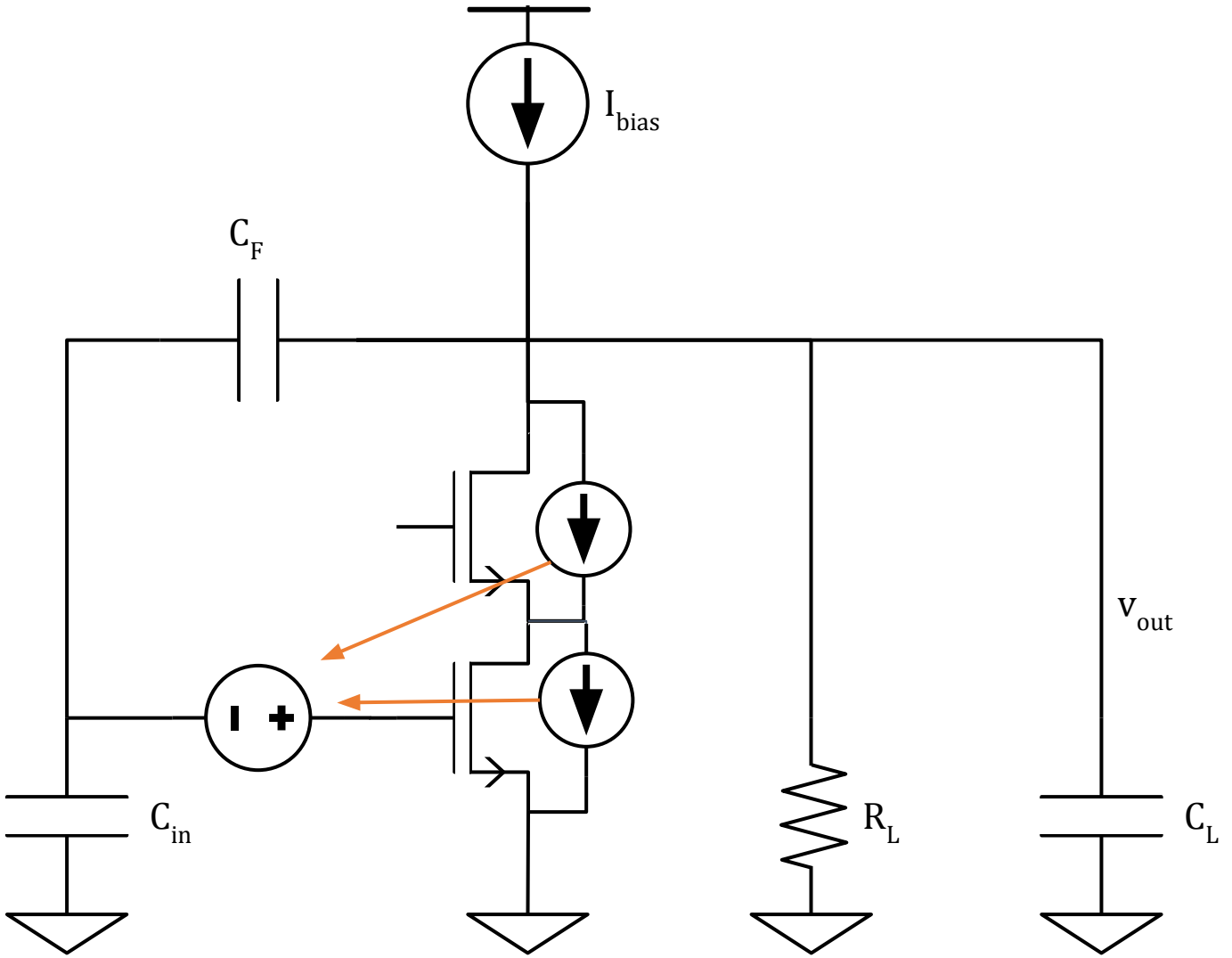
Bonus/Extra

Feedback Noise

AC Analysis And Feedback

Noise from the first transistor

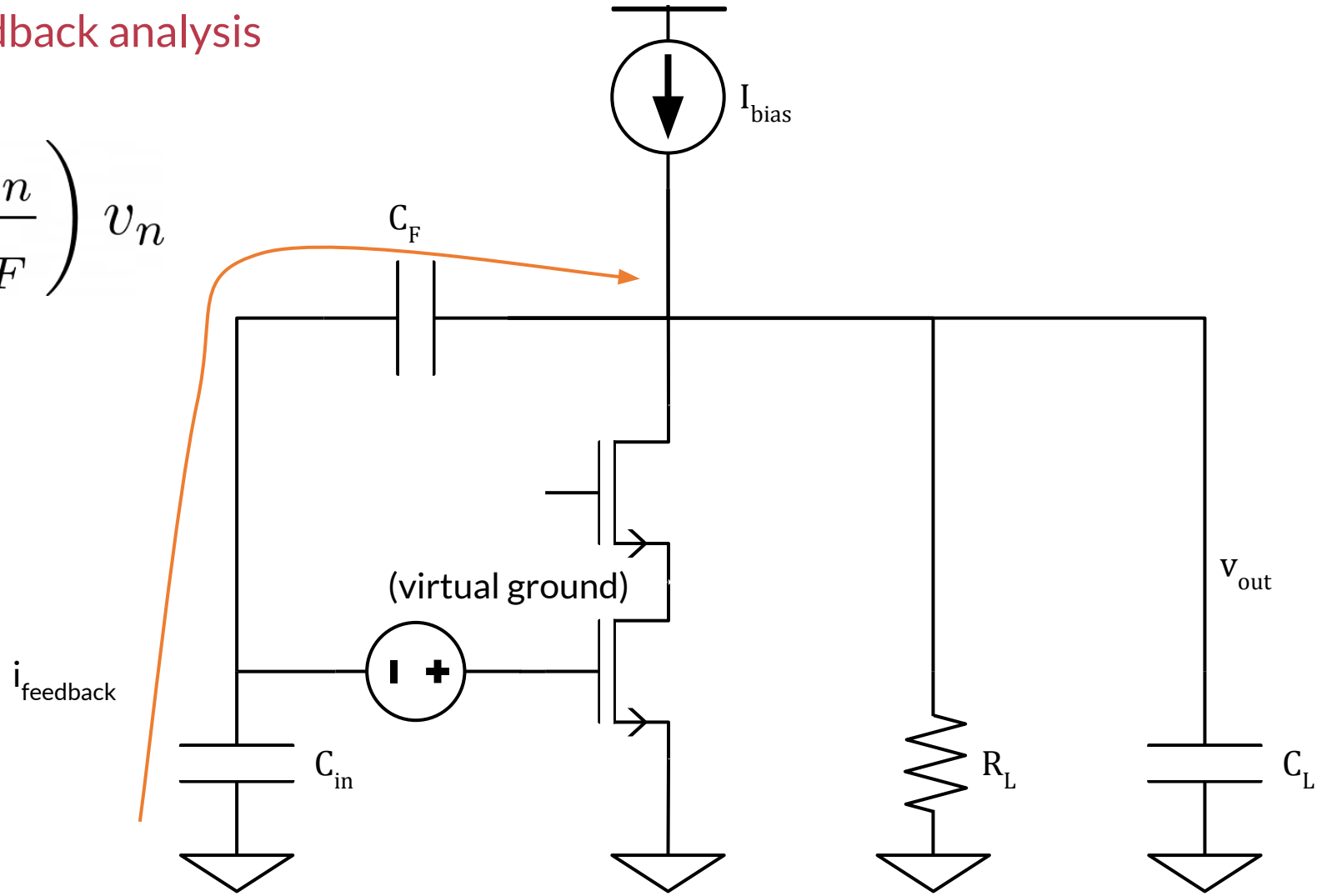
Refer All Transistor Noise To Amplifier Input



Refer All Transistor Noise To Amplifier Input

Perform the same ideal feedback analysis

$$v_{out,gm=\infty} = \left(1 + \frac{C_{in}}{C_F}\right) v_n$$

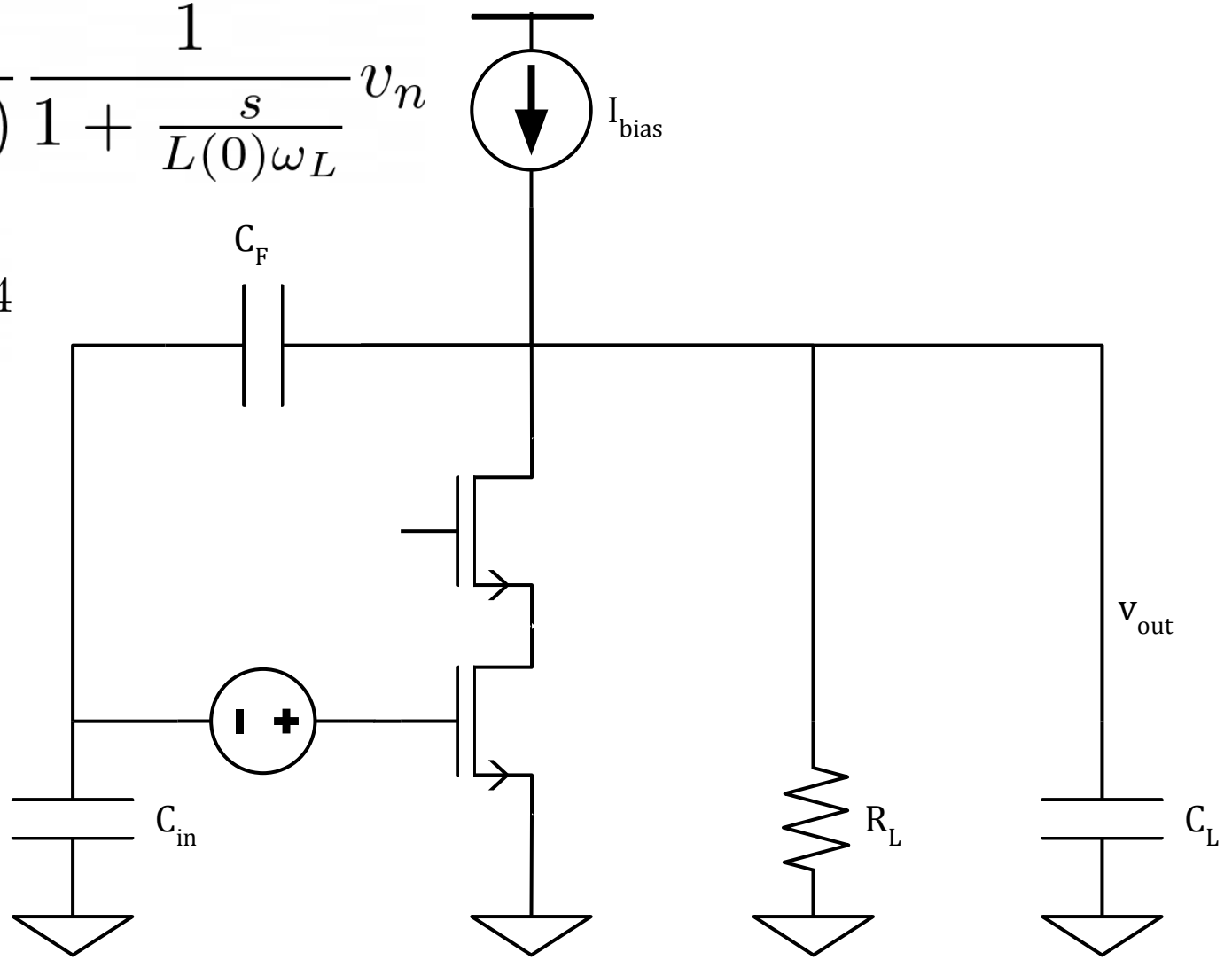


Noise Feedback (For simplicity treat as single pole)

$$v_{out,n} \approx \left(1 + \frac{C_{in}}{C_F}\right) \frac{L(0)}{1+L(0)} \frac{1}{1+\frac{s}{L(0)\omega_L}} v_n$$

$$\overline{v_{out,n}^2} \approx \left(1 + \frac{C_{in}}{C_F}\right)^2 \left|\frac{L(0)}{1+L(0)}\right|^2 \overline{v_n^2}\omega_u/4$$

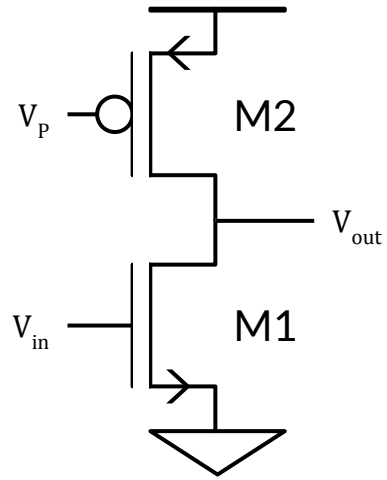
Unity gain frequency of open loop

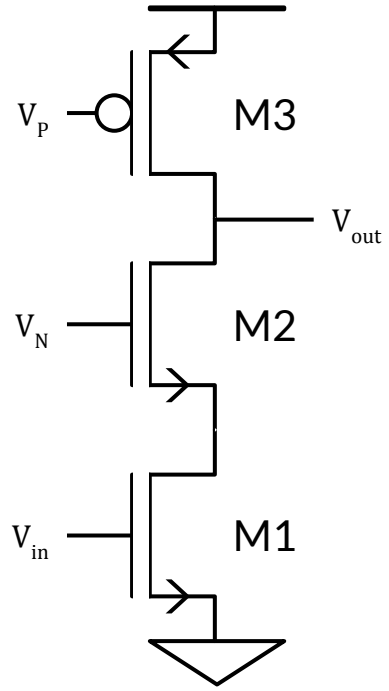


Hand Exercises

Derive The DC Gain in terms of g_{m1}, g_{gds1}, g_{m2} etc

Do NOT use KVL/KCL. Only the previous impedance formulas and current dividers

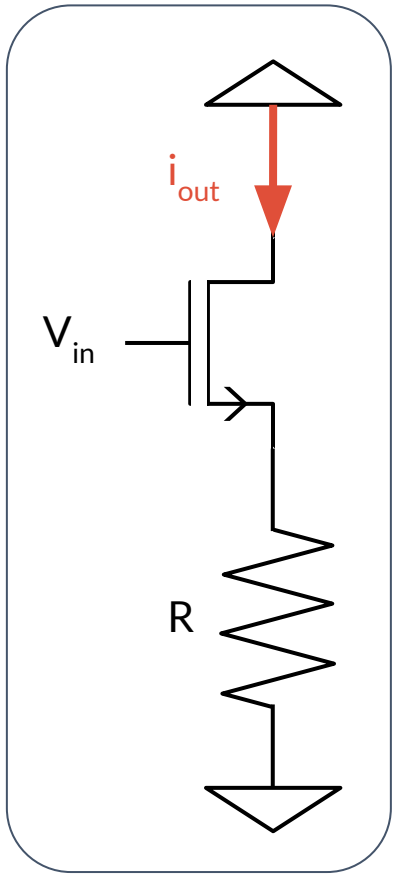


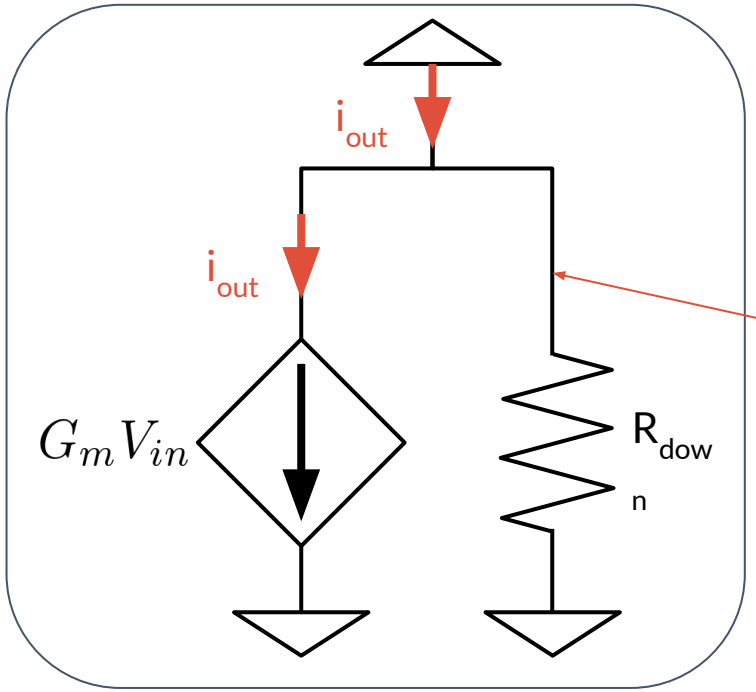


No body effect

Derive the transimpedance of the degenerated common source

Reminder: A current source acts ideally when it is at 0V, so have i_{out} come from ground.



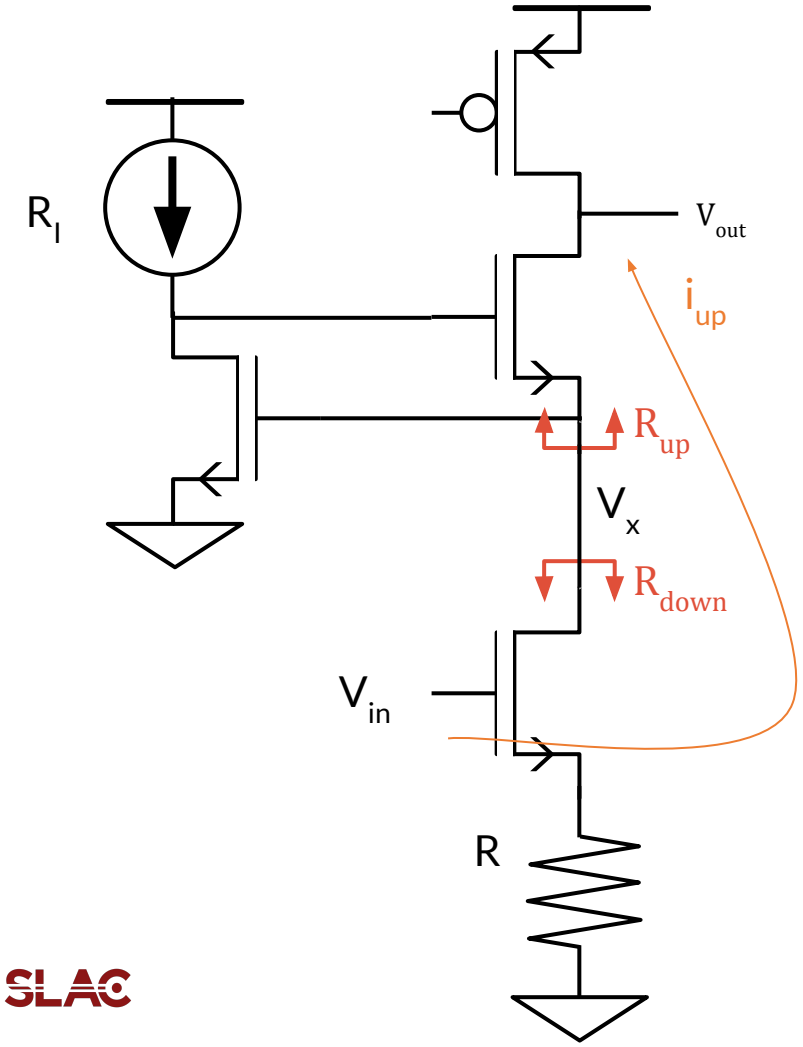


$$G_m = \left.\frac{i_{out}}{V_{in}}\right|_{V_{out}=0}$$

No loss due to the current source driving a voltage

Finale: Find DC gain without KVL/KCL

Assume all transistors have same gm and r0. Use only the impedance formulas found in the slides. The value for R_{up} for a "super" common gate stage is provided



Methodology:

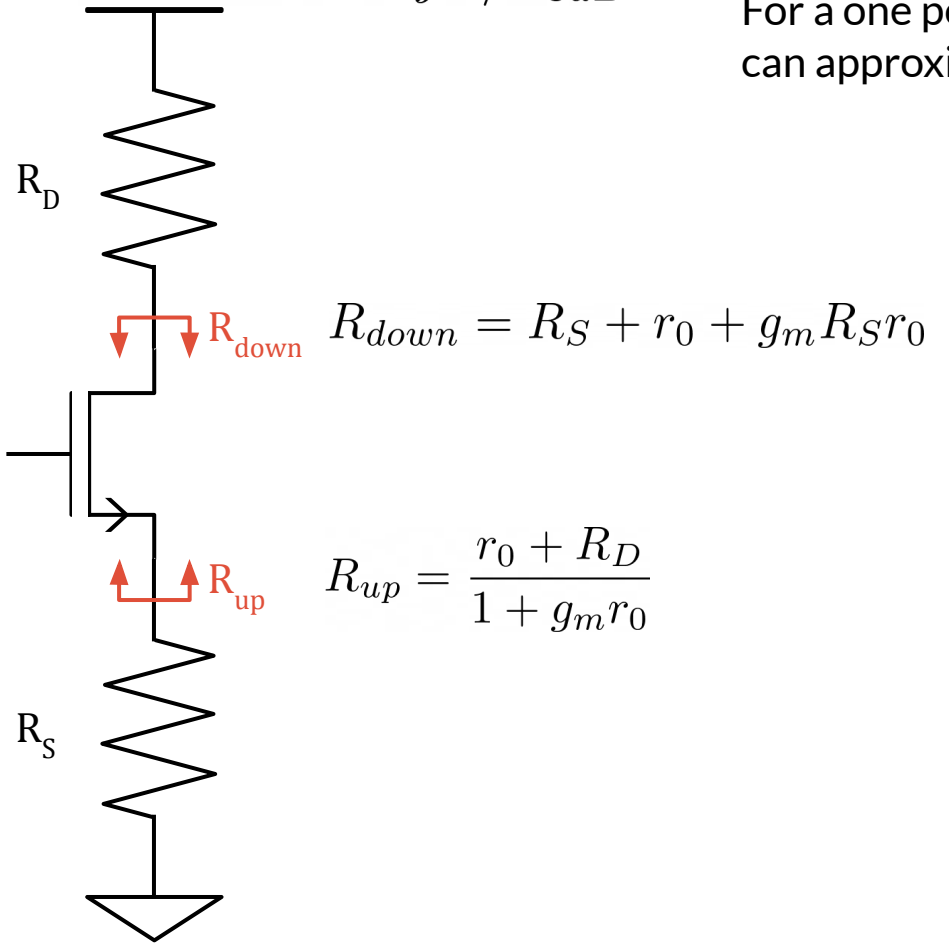
1. Find the equivalent impedances R_{down} using the common gate formulas from the handout.
2. Find the equivalent impedance R_{up} using the "super" common gate formulas from the handout.
3. The current injected by the input transistor into the node V_x is given by the formula derived in the previous exercise.
4. Part of this injected current will flow down, and part of it will flow up into the output load. The ratio of how much current will flow up is given by the current divider ratio of R_{down} and R_{up}.

Formulas

$$H(j\omega) = \frac{A}{1 + j\omega/\omega_{3dB}}$$

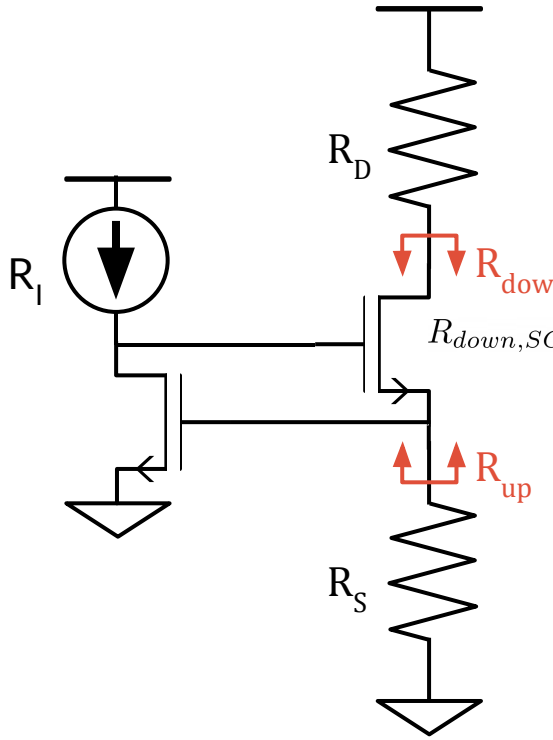
The 3dB frequency occurs when $v_{out}(\omega_{3dB}) = v_{out}(\omega = 0)/\sqrt{2}$

For a one pole system, the pole is the 3dB frequency. For a two pole system, we can approximate the 3dB frequency by the lowest frequency pole.



$$R_{down} = R_S + r_0 + g_m R_S r_0$$

$$R_{up} = \frac{r_0 + R_D}{1 + g_m r_0}$$



$$R_{down,SCG} = R_S + r_0 + g_m r_0 R_S (1 + g_m r_0 (1 + r_0/R_I))$$

$$R_{up,SCG} = \frac{r_0 + R_D}{1 + g_m r_0 + \frac{(g_m r_0)^2}{1 + r_0/R_I}}$$