28nm CMOS 4D Pixel detector readout chip
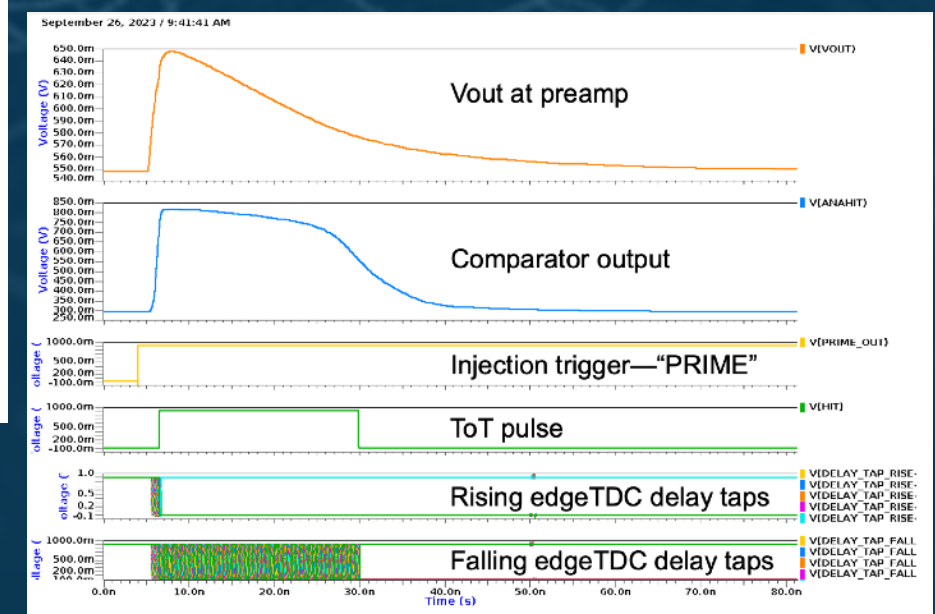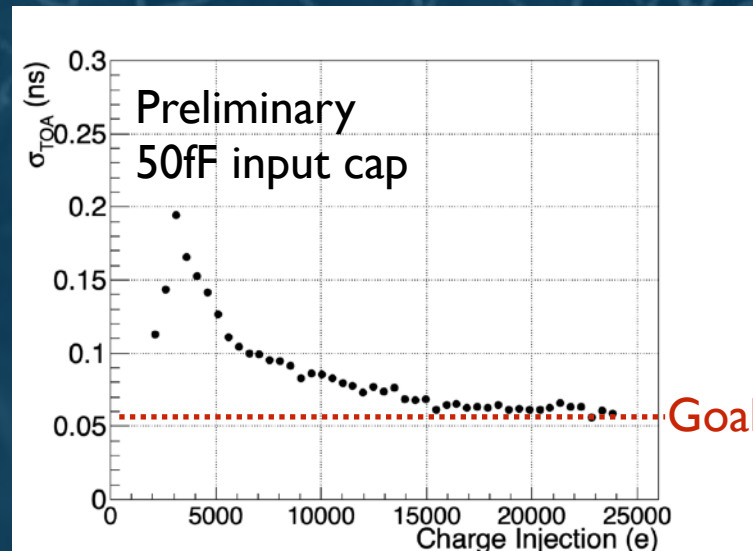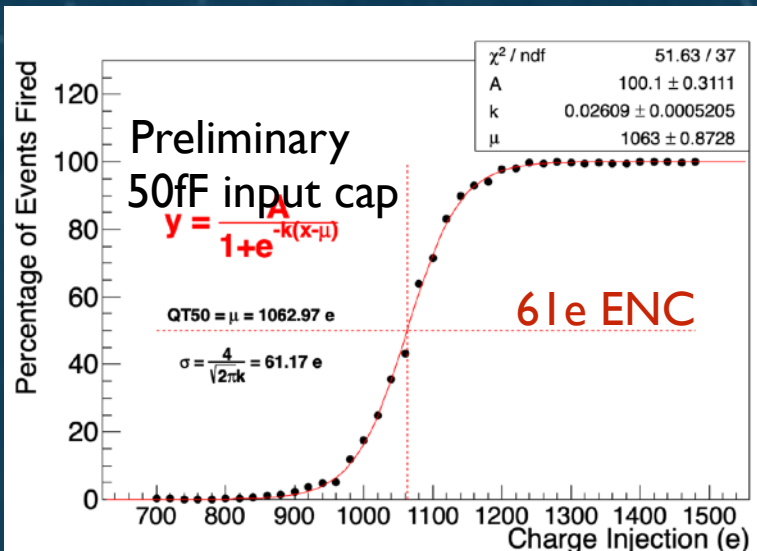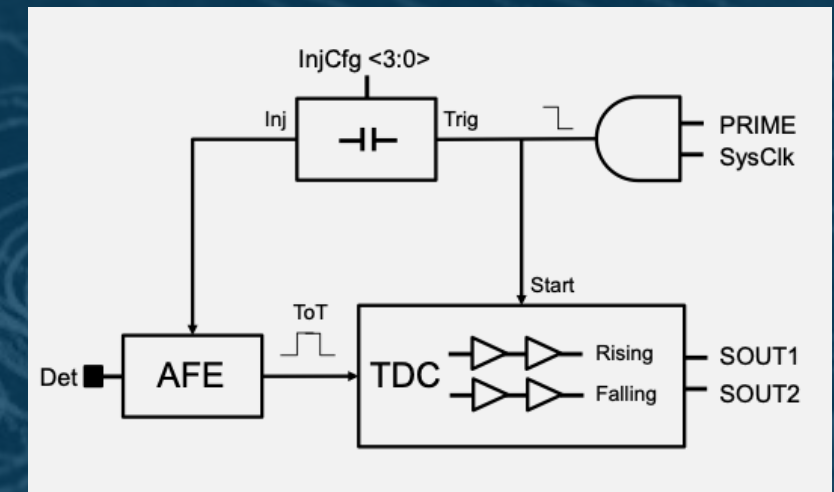
RDC4 - 16.10.23

T. Heim, M. Garcia-Sciveres, C. Grace,
A. Krieger, Z. Zhang — LBNL

U.S. DEPARTMENT OF **ENERGY**   **UNIVERSITY OF CALIFORNIA**

- ATLAS ITk Pixel inner system designed for half of the original HL-LHC run time → planned to be replaced half-way through HL-LHC era

- Final opportunity for more than a decade to test and operate a real 4D tracker in the flesh, but have to set achievable specs

    - Maintain current ITk specs:

        - 50um by 50um pixel pitch

        - Analog front-end: <100e noise, <1000e threshold, <5uW, 30um x 30um

    - Add:

        - ~50ps timing resolution (AFE, TDC, readout logic) (3D sensor technology)

- 65nm technology fully exploited with current needs (>90% routing density in ITkPix pixel)

- Any additional logic requires miniaturization → 28nm CMOS

    - LBNL has started effort in 28nm CMOS chip design with focus on analog

- Submitted two 28nm mini-ASICS:

  - Pebbles: implements Big-Rock AFE with on-chip test bench (received Oct 2022)

  - Metarock: improved Big-Rock AFE with realistic TDC (currently being manufactures)

- Big-Rock AFE: 10x30um2, 4uW, <100e noise, ~50ps timing @ 50fF detector capacitance

- Pixel TDC: 15x15um2, 1-2uW average, 40MHz clock

Preliminary 50fF input cap

$$y = \frac{A}{1+e^{-k(x-\mu)}}$$

χ^2 / ndf	51.63 / 37
A	100.1 ± 0.3111
k	0.02609 ± 0.0005205
μ	1063 ± 0.8728

QT50 = μ = 1062.97 e

$\sigma = \frac{4}{\sqrt{2\pi}k} = 61.17$ e

61e ENC

Preliminary 50fF input cap

Goal

Vout at preamp

Comparator output

Injection trigger—"PRIME"

ToT pulse

Rising edgeTDC delay taps

Falling edgeTDC delay taps

September 26, 2023 / 9:41:41 AM
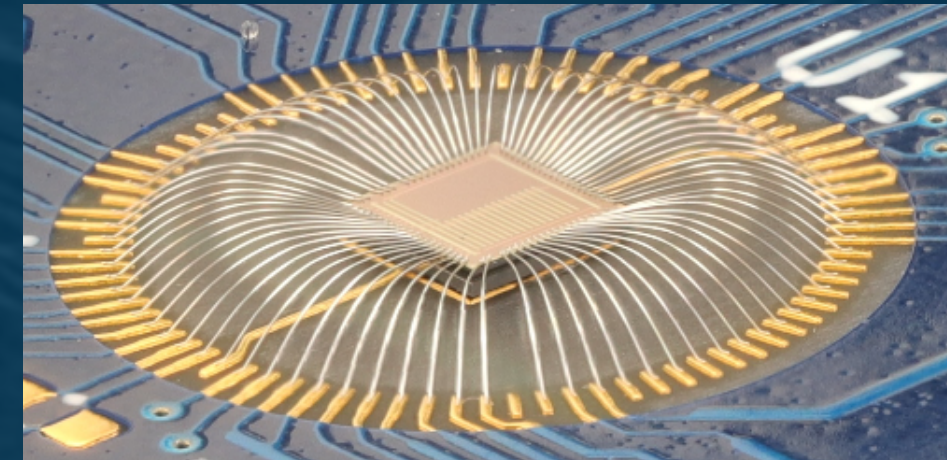
Also aiming to test 28nm for operation at cryogenic conditions, Pebbles includes cryo-suitable reference voltage circuits, Metarock includes single transistor test circuits.