SLAC CPAD RDC4 Activities & Interests

SLAC TID & FPD

16 October 2023

SLAC NATIONAL ACCELERATOR LABORATORY

Stanford University | U.S. DEPARTMENT OF ENERGY

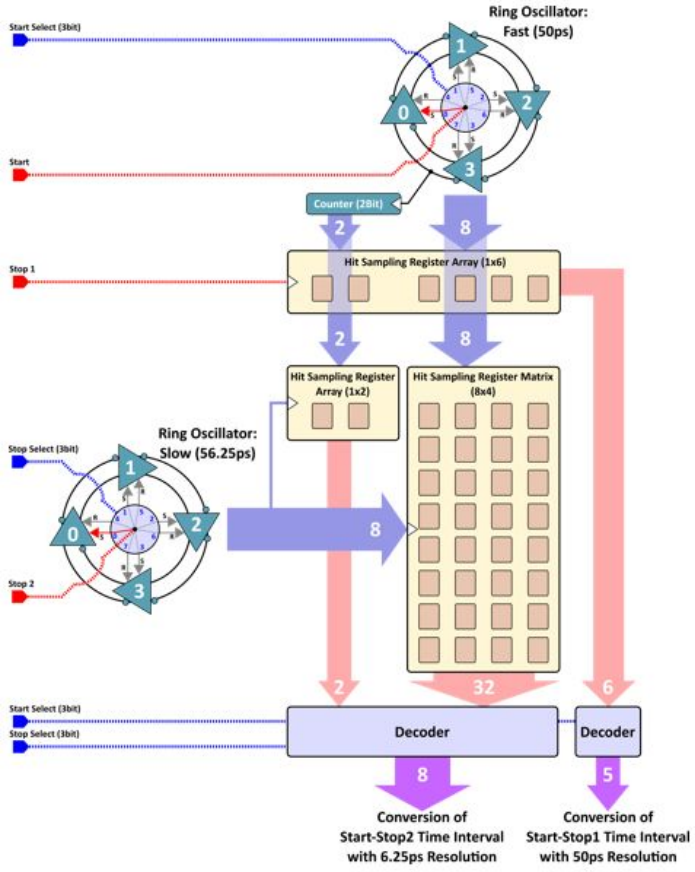
SLAC CPAD RDC4: 4D tracking

- **Co-design of overall detector/sensor/ASICs on-going at SLAC**

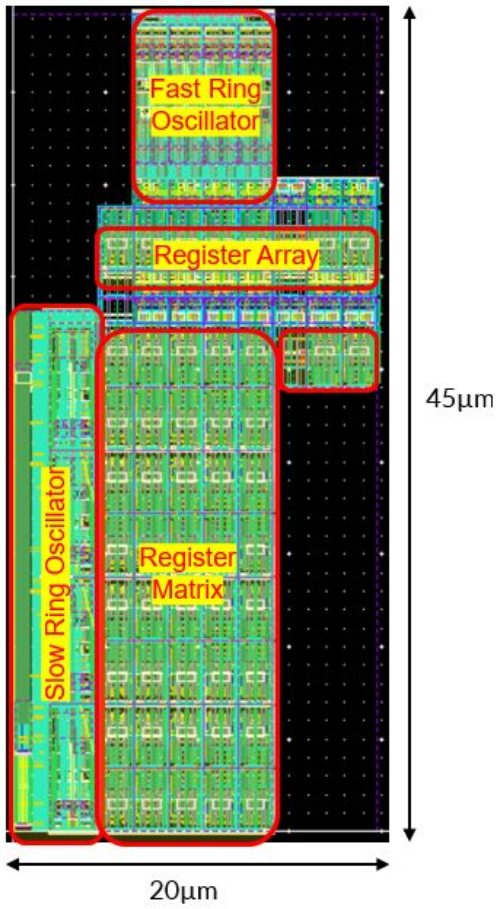
- Physics, simulation, and detector optimization
  - HL-LHC 4D tracking upgrade and future Higgs Factories and high energy colliders (Ariel Schwartzman + students)
  - 4D Clustering/Seeding/Tracking algorithms and physics event reconstruction
  - Synergies with 5D calorimetry
- DOE's Accelerate Innovations in Emerging Technologies - *3D Integrated Sensing Solutions* project (SLAC, FNAL, LLNL)
  - Develop LGAD sensors in commercial 12" CMOS process and couple to dedicated front-end in 28nm with wafer-to-wafer bonding (Julie Segal, Christopher Kenney, Lorenzo Rota, Bojan Markovic)
- DOE's HEP Detector R&D program - Development of electronics for 4D in 28nm node:
  - Sub-10ps TDC (Bojan Markovic)
  - Constant fraction discriminator (CFD) (Victor Turbiner, EE Ph.D student)
  - ADC (Aldo Pena Perez)

- **Collaboration opportunities:** development of common IP blocks in TSMC 28nm node

SLAC CPAD RDC4: 4D tracking



a)



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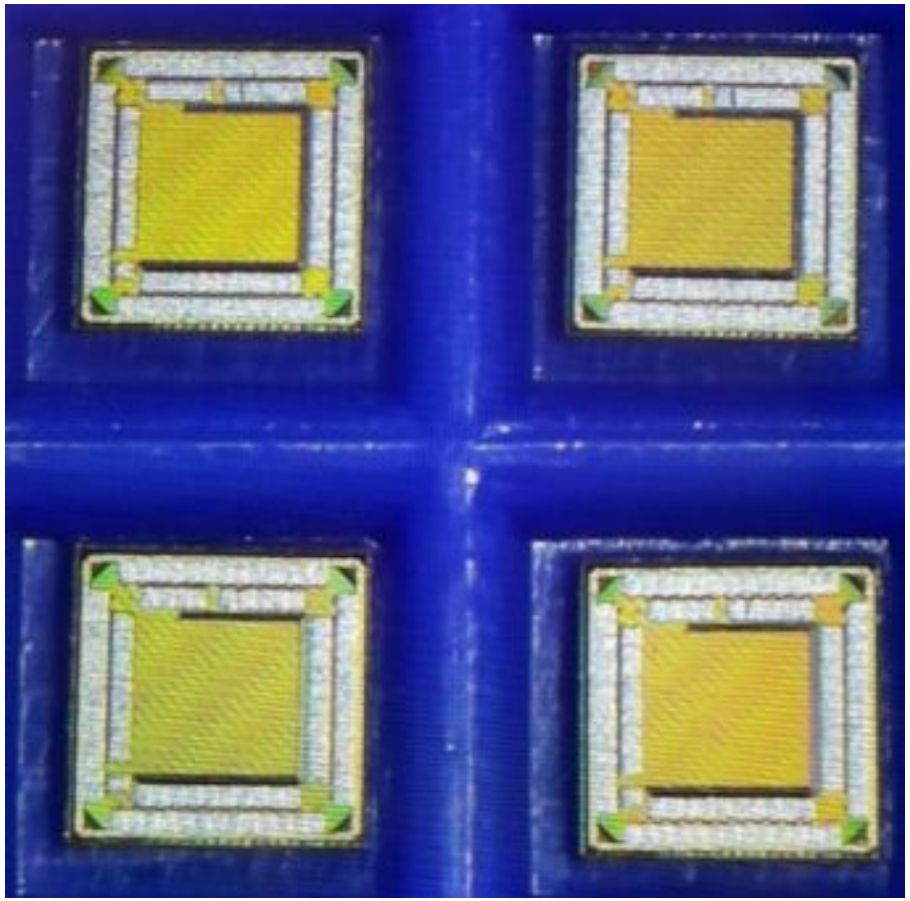


PIs: Bojan Markovic, Ariel Schwartzmann, Julie Segal

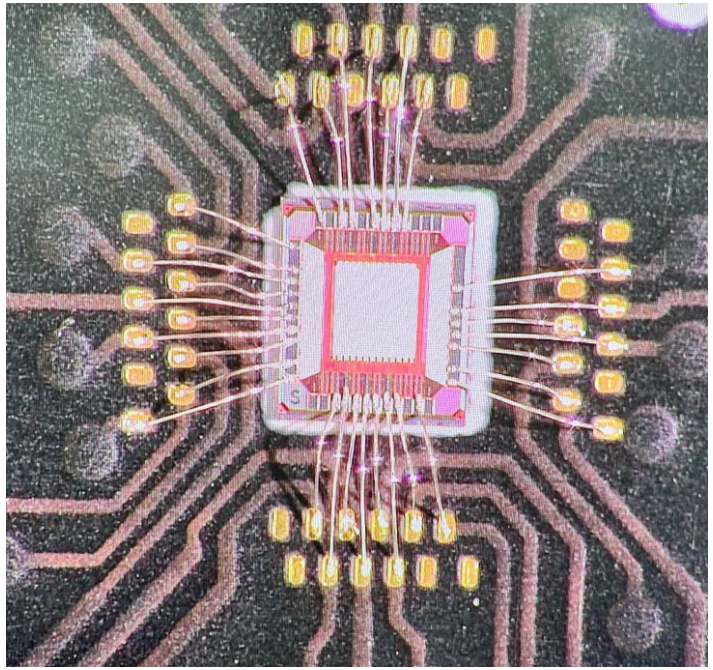
SLAC CPAD RDC4: Large-area MAPS with ~ns timing

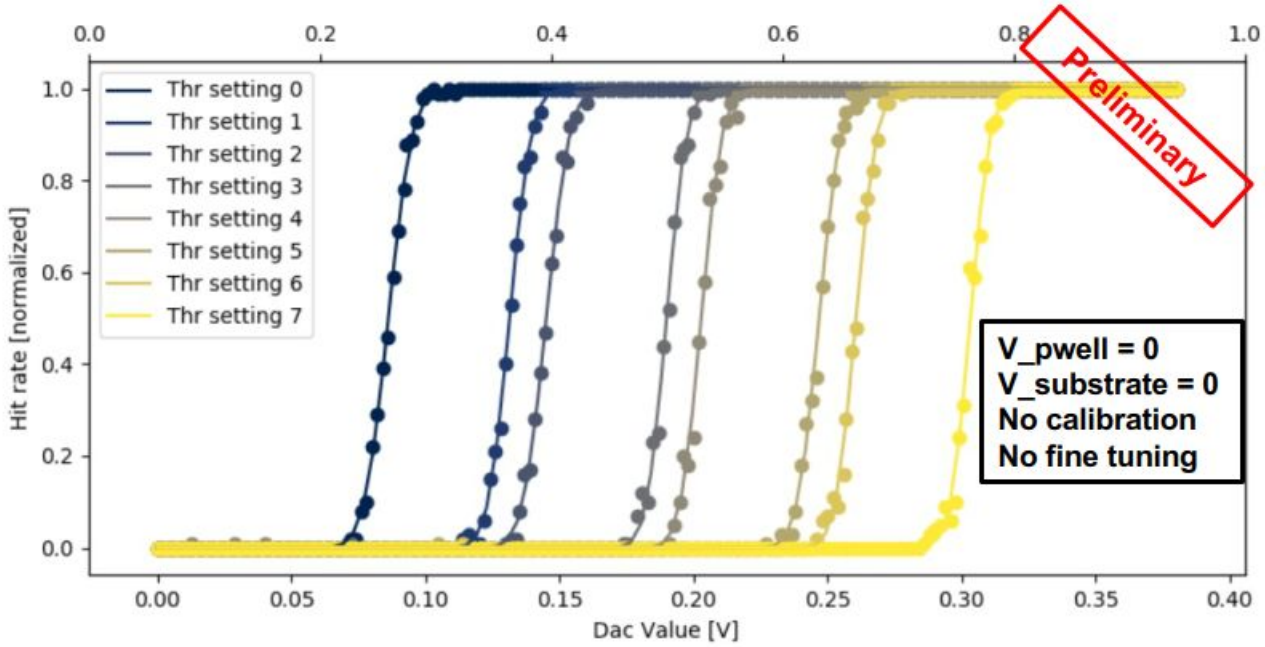
- **Motivation: develop new generation of large-area, ultra-low-mass detectors**
- R&D on Monolithic Active Pixel Sensors (MAPS) for high precision tracker and high granularity calorimetry
- Goals: can we combine low-power, large-area and ~ns timing in a single die?
- Focus is on co-design at system level: power distribution, yield, physics-driven optimization

- **Collaboration:** CERN WP1.2, University of Oregon, etc.
- Technology: TowerJazz-Panasonic 65nm Imaging process
- Submitted LOI in DRD7, MAPS work-package

- **Collaboration opportunities:**
  - Development of common IP blocks in TPSCo 65nm node
  - Testing and characterization of prototypes, beam times, etc.

SLAC CPAD RDC4: Large-area MAPS with ~ns timing



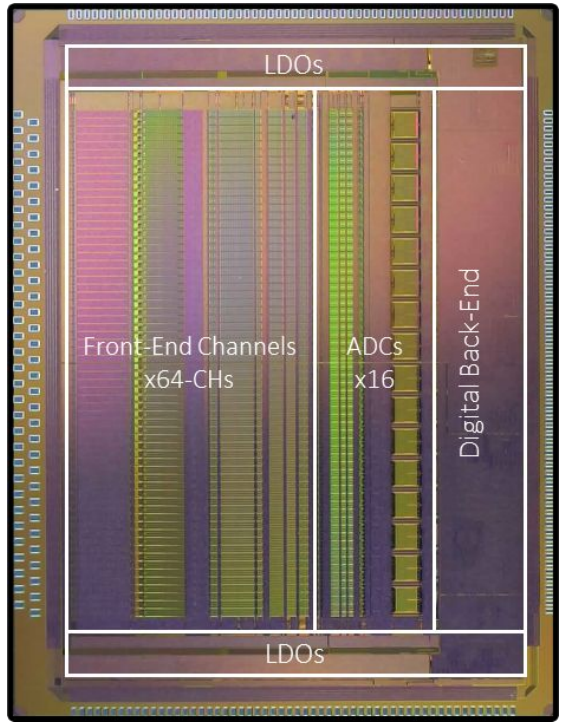


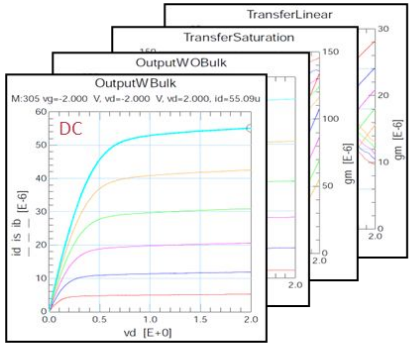
- First prototype is functional (NAPA-v1, demonstrator)
- Characterization is on-going
- Design of NAPA-v2 on-going

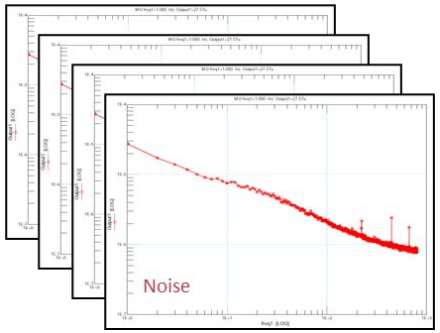
SLAC CPAD RDC4: Cryogenic CMOS

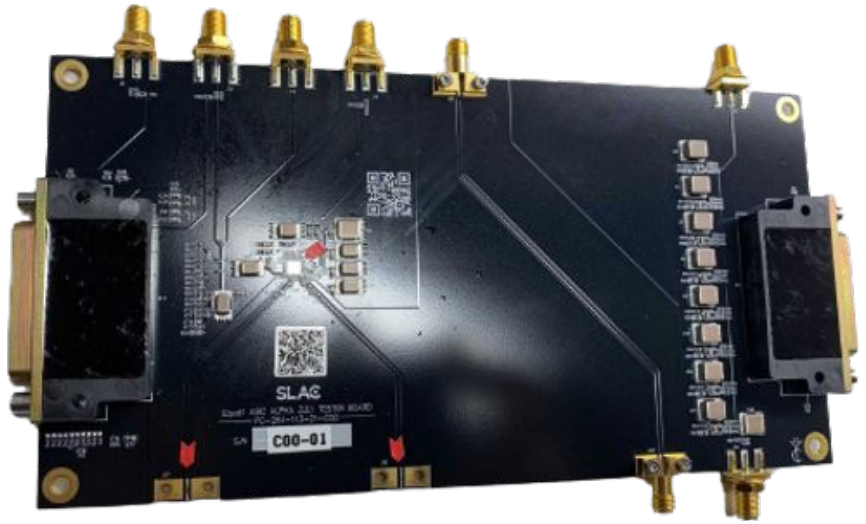
- **Several developments of Cryogenic CMOS for different applications/temperatures at SLAC:**
  - **nEXO:** Neutrinoless Double-beta Decay experiment
  - **Dune:** Deep Underground Neutrino Experiment (DUNE)
  - **GammaTPC telescope:** GAMPix ASIC
  - **Cryo-CMOS at 4K:** Quantum Sensing and SoC
- **Goal:** integrate more functionality in readout ASICs operating at cryogenic temperatures
- **Technologies:**
  - TSMC 130nm
  - GF 22nm FDSOI
- **Collaboration opportunities:**
  - Development of readout ASICs and SoC
  - Characterization of technologies and development of custom models

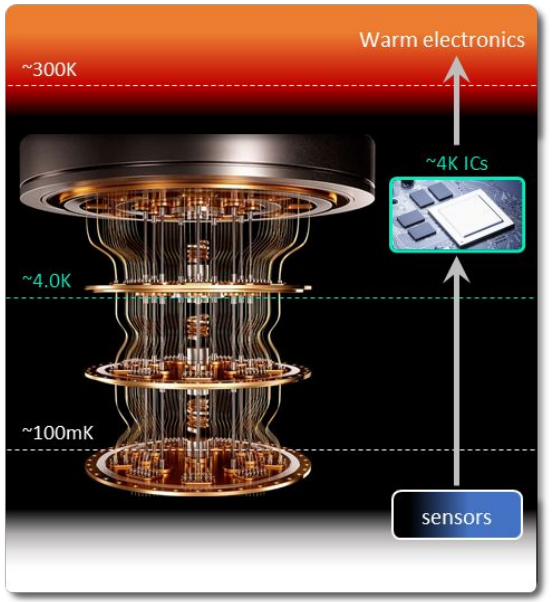
SLAC CPAD RDC4: Cryogenic CMOS









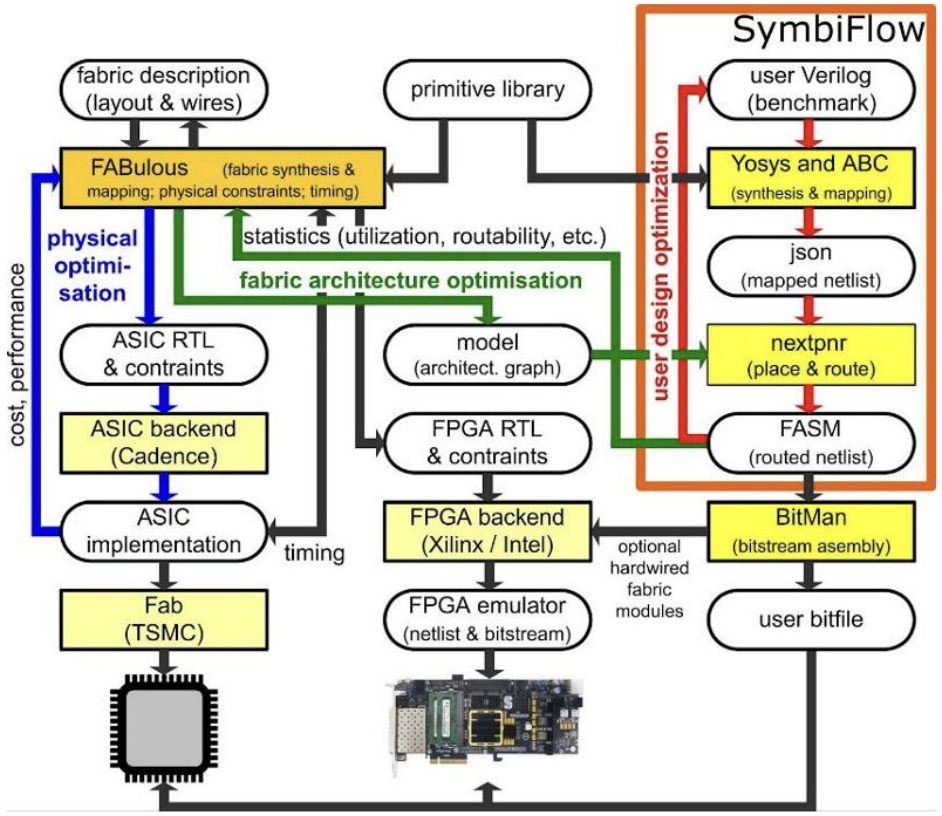


- Cryogenic waveform digitizing System-on-Chip for cold TPCs
- PDK modeling for extreme environments
- Readout card for 4K Cryo-CMOS LNA testing

PIs: Aldo Pena Perez

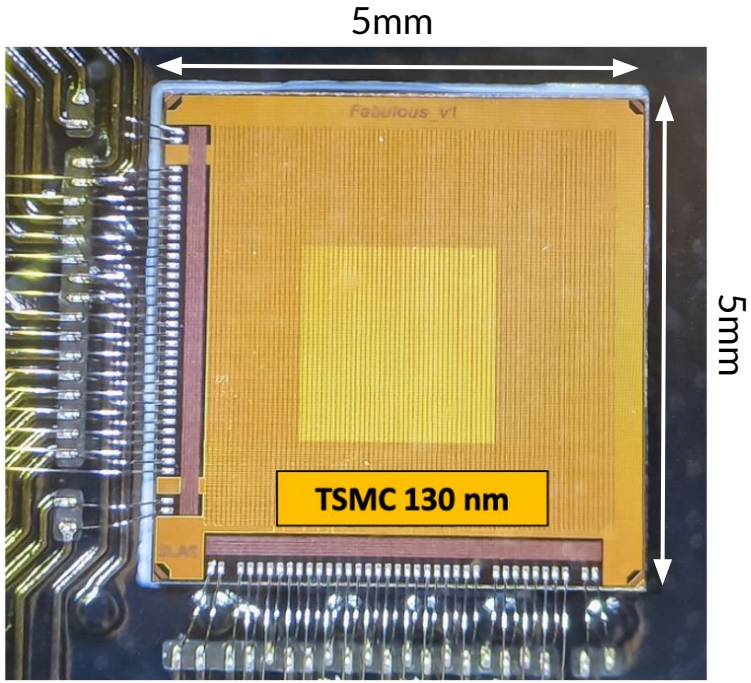
SLAC CPAD RDC4: eFPGA and Reconfigurable Digital Logic

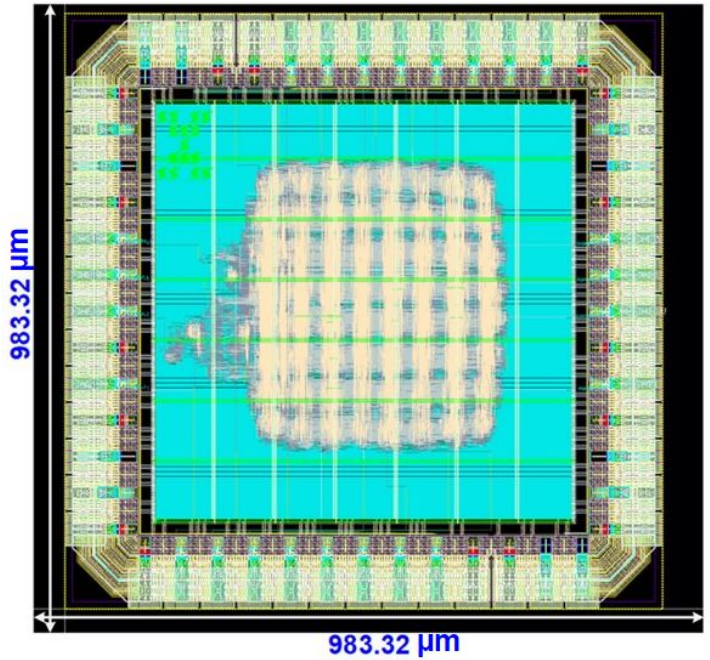
- **Goal:** move more data processing into the front-end ASICs
- Often algorithms and data processing techniques must evolve which make ASIC deployment problematic
  - Custom ASICs need to support updatable data processing pipelines
- Several popular FPGA architectures are becoming 20+ years old
  - Original patents have expired
  - Includes Spartan-3 and Virtex-II FPGAs from Xilinx
- In 2021, University of Manchester has started an **open-source** project called FABulous
  - an Embedded FPGA (eFPGA) Framework
- Idea is that you put an "reconfigurable logic" in your ASIC design
- SLAC is experimenting with this approach to determine it feasibility for front end data processing, both classical and ML based



PIs: Larry Ruckman

SLAC CPAD RDC4: eFPGA and Reconfigurable Digital Logic

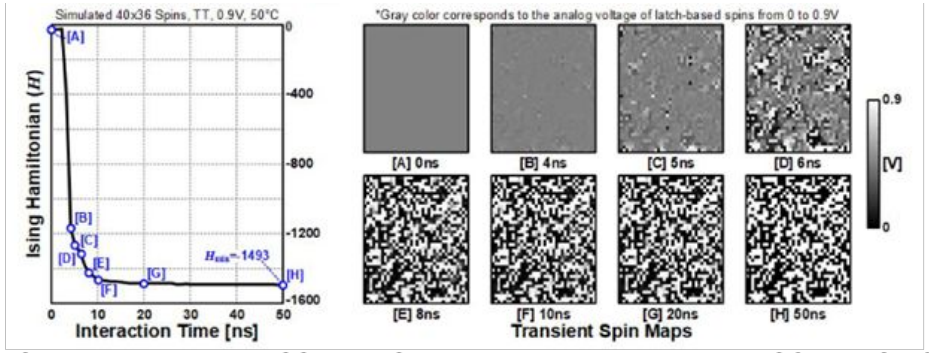




- 1st generation embedded FPGA in ASIC using open source libraries using TSMC 130nm
- 2nd generation embedded FPGA in ASIC using open source libraries using TSMC 28nm

SLAC CPAD RDC4: beyond Von-Neumann accelerators

- ASIC architecture R&D for edge data processing and other complex computing task optimization
- Process time, energy and area optimization using unconventional computing paradigm
- Investigating different approaches: in-memory computing, CMOS ISING computers
- Addresses BRN for Microelectronics PRD#4 : Class-1 optimization machines and/or non-von Neumann architectures
- HEP applications in form of solving QUBO problems



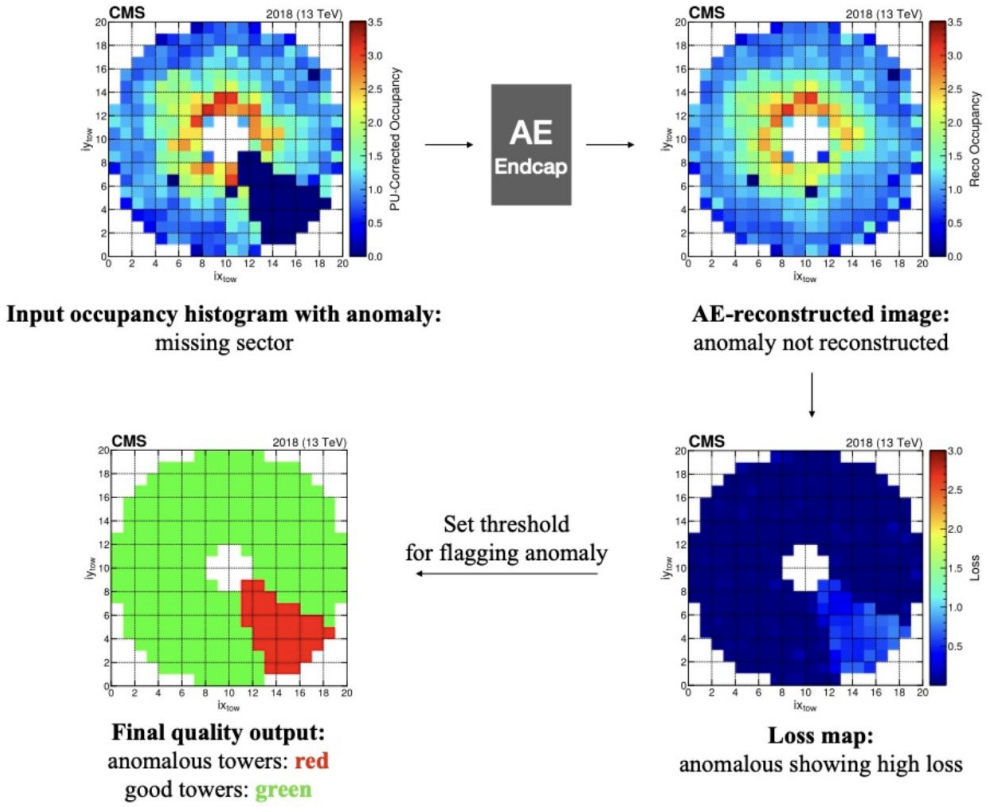
Hardware Max-cut Problem Solver *J. Bae et al (ISSCC'23)*

SLAC CPAD RDC4: AI/ML for Future Readout

- Motivation: facilitate broader application of ML models to address challenges of future collider (and general HEP) readout/DAQ environments
  - High data density/compression, fast front-end feature extraction, front-end programmability, detector monitoring
  - Focus on newer/complex models: anomaly detection, graphs, …
  - Open-source IPs for broad deployment of common ML architectures

- Overlap with RDC5: future anomaly detection trigger infrastructure via fast anomaly classifiers (autoencoders, etc.)
- Objectives (from 2306.13567)
  - Conceptual design for generic AI/ML in ASICs including inference/AD algorithms in both the digital and/or analog space
  - Prototypes for generic AI/ML ASICs respecting expected experimental restrictions on latency, power consumption, granularity, etc.
  - Experiment-specific prototypes?
- Build on overlap with/applications of ongoing SLAC work: 28nm eFPGA, SNL, GPUs on ASICs, …
  - And at other institutes!

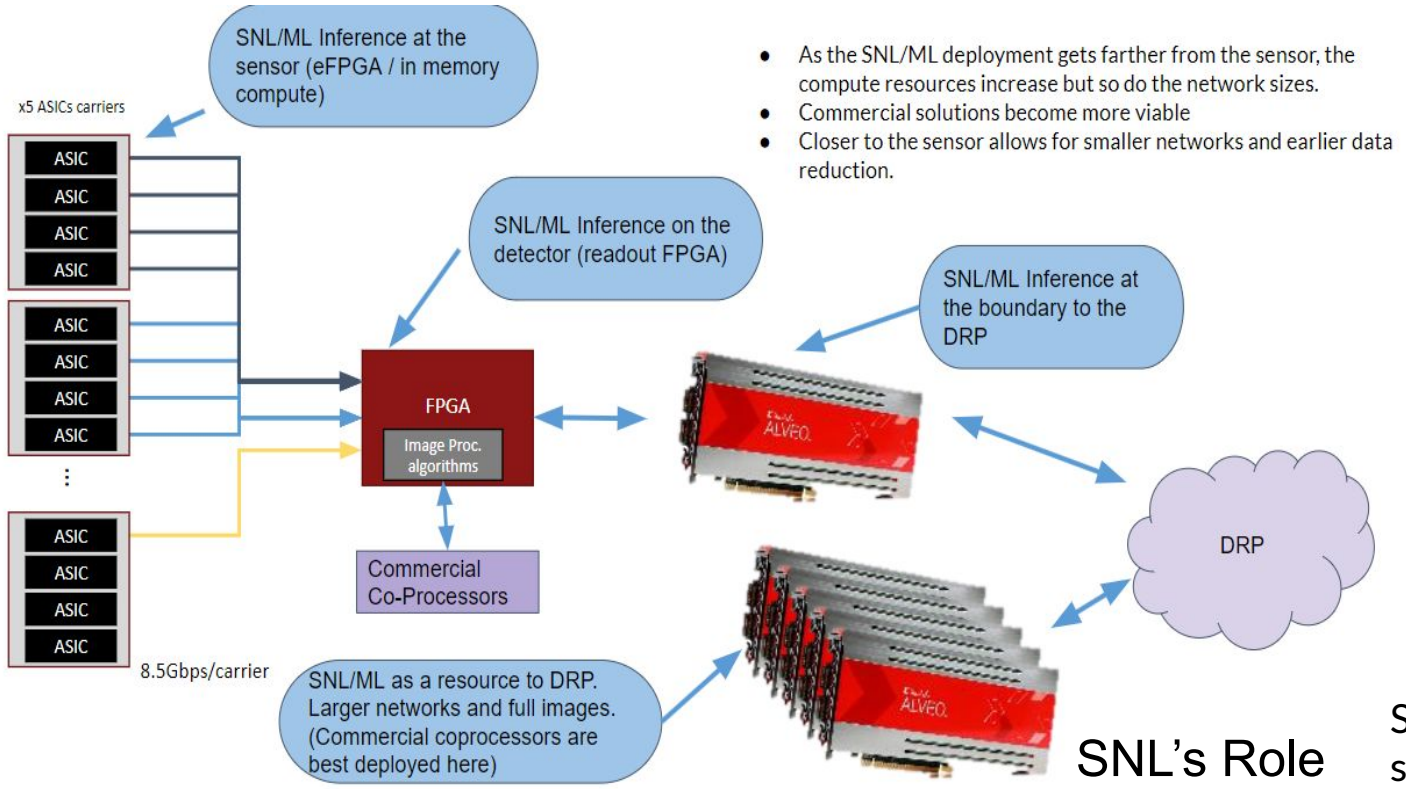
CMS ECal AD Monitoring



SLAC CPAD RDC4: SNL

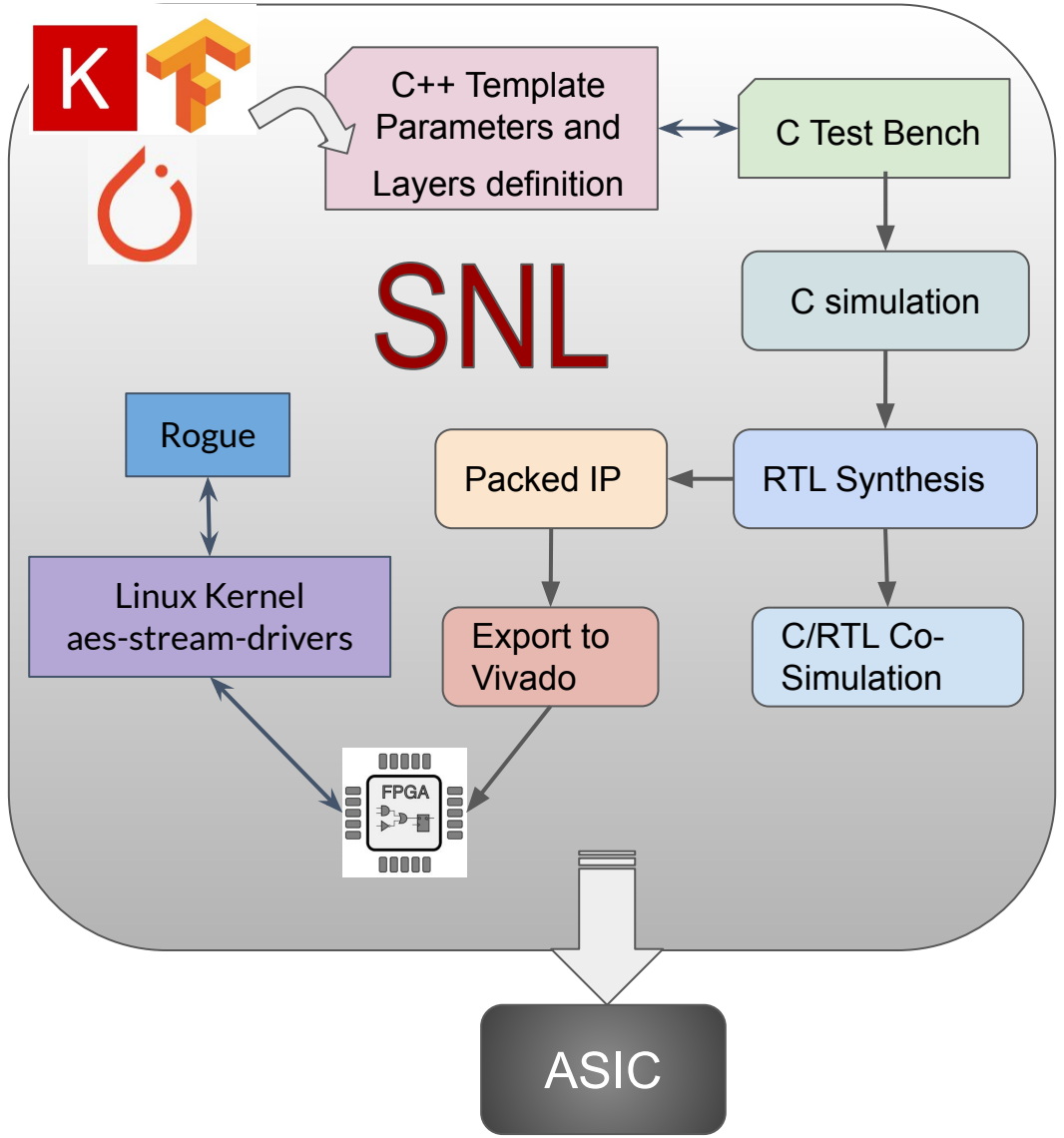
Goals

- Provides specialized set of libraries designed in High-Level Synthesis (HLS) for deploying high-performance, low-latency ML inferences on FPGAs, eFPGAs and ASICs
- Supports Keras like API for layer definition
- Dynamic reloading of weights and biases to avoid re-synthesis
- Supports few thousand of parameters for the inference model
- Total end to end latency of **1uS** to **10ms**



SNL's Role

SNL's Design Flow



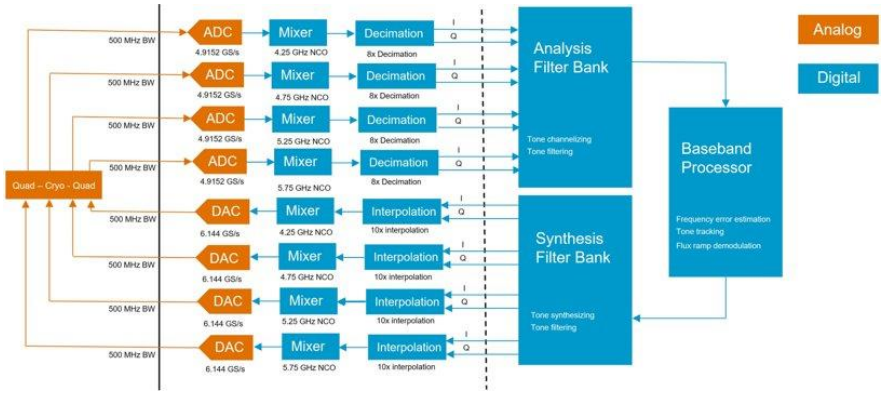
SNL acts as a framework for constructing innovative network structures, setting it apart from HLS4ML, with future consideration given to incorporating ASIC flow.

PIs: Ryan Herbst

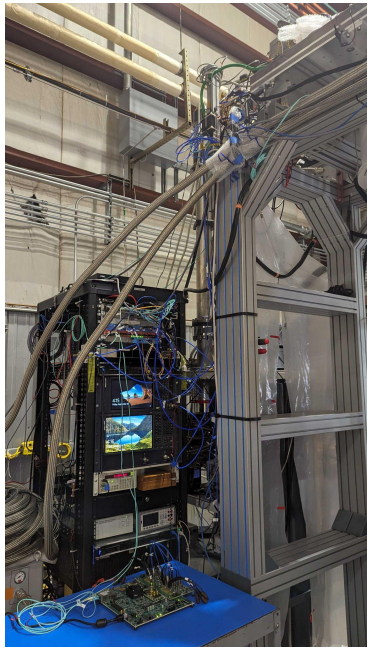
SLAC CPAD RDC4: RFSoC-based Readout Developments

- Motivation: RF system-on-chip (RFSoC) devices have been widely used for instrumentation development at SLAC for various physics experiments hosted by SLAC and other collaborators worldwide.
  - High-speed data converters and integrated up and down conversion
  - Large amount of programmable logic resources and powerful processor integrated
  - RFSoC devices has great potential to reduce the footprint and cost of readouts
- On-going RFSoC-based readout development projects
  - Readout for superconducting detectors of microwave SQUID multiplexers (μmux) or microwave kinetic inductance detectors (MKIDs) for Cosmic Microwave Background (CMB) experiments
  - readout and control platforms using RFSoC devices for axion dark matter detection
  - Readout for quantum device-based sensors targeting meV-Scale energy sensitivity
  - Digital backend for radio astronomy receivers based on heterodyne methods in C band and X band

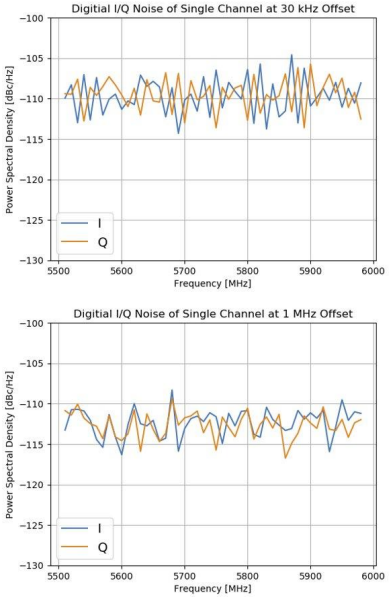
Block diagram of RFSoC-based uMux readout



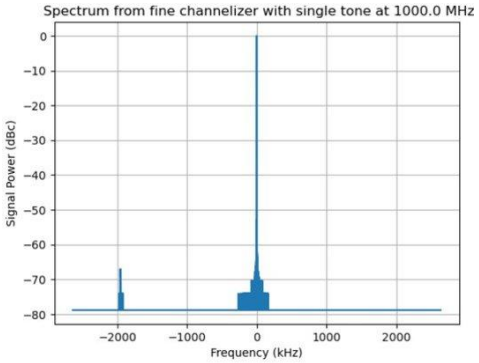
Cryostat test stand



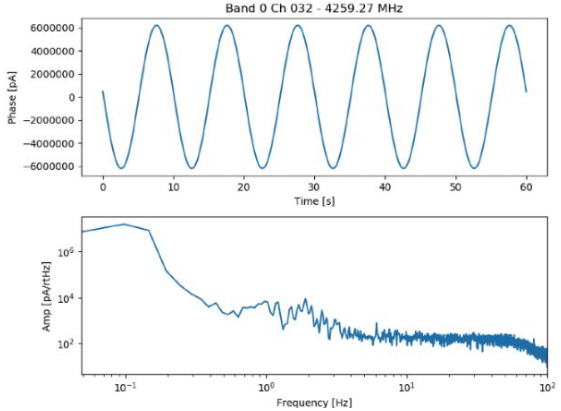
Loopback phase noise as low as -110 dBc/Hz



Channelizer with 200s+ integration time



Injecting sine wave into a superconducting resonator and reading it with our RFSoC-based readout readout!



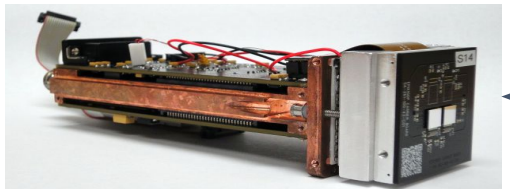
PIs: Chao Liu, Ryan Herbst and Larry Ruckman

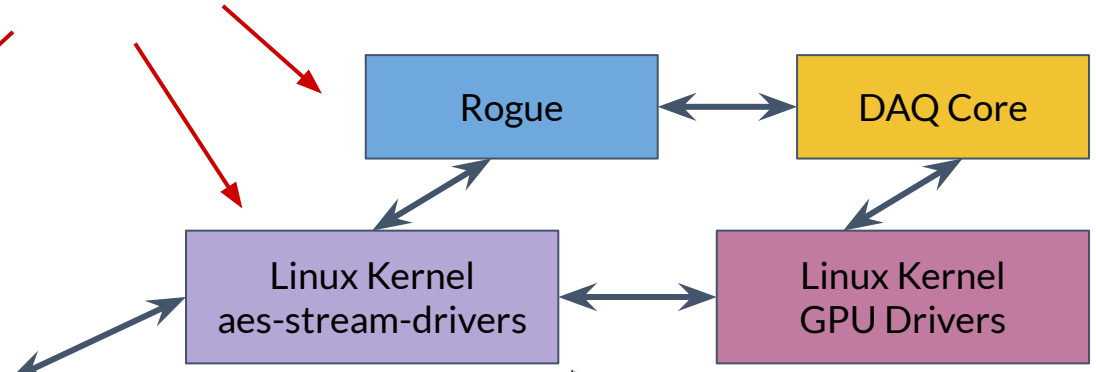
SLAC CPAD RDC4: Open Source Shared Libraries

- Reliable UDP (RUDP) Network offload engine to support network attached devices (NAT)
- High bandwidth synchronous (timing & trigger delivery) & asynchronous fiber protocols for front end readout (PGP2,PGP3)
- SLAC Ultimate RTL Framework (SURF):
  - Open source VHDL/Verilog framework for rapid FPGA/ASIC development using common generic, extensible libraries
  - Ruckus: Open source build system

https://github.com/slaclab/surf
https://github.com/slaclab/ruckus
https://github.com/slaclab/rogue

- Open source DMA engine & associated driver for high bandwidth & high rate DMA transfer
  - Works both in amd64 & Zynq (SOC + RFSOC) platforms
  - Zero copy user space buffer mapping
  - Direct to GPU data transfer support
- Rogue: Open source Python/C++ hardware abstraction software for rapid readout development & test stand support
  - Easily integrated into back end DAQ systems
  - Balanced python (ease of use) and C++ (high bandwidth & high event rate) implementation





Direct to GPU DMA support in open source DMA Engine & Driver

SLAC TECHNOLOGY INNOVATION DIRECTORATE

PIs: R. Herbst, L. Ruckman, B. Reese