CPAD RDC4 BlueSky Initiative from SCIPP

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UNIVERSITY OF CALIFORNIA
SANTA CRUZ

Introduction

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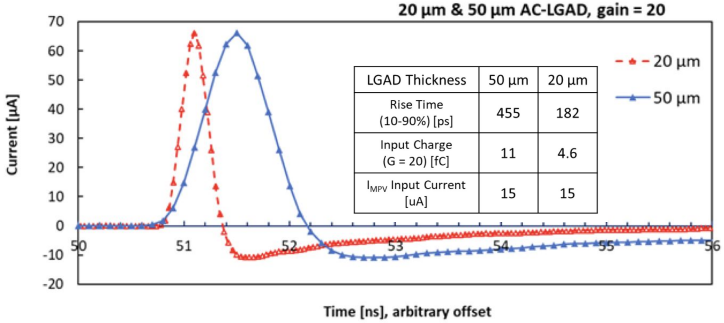
- UC Santa Cruz has been working on ASICs for readout of fast signals generated by AC-LGADs silicon sensors
- Overarching design goals:
  - **Fast timing** (Jitter < 10ps)
  - **Low-power consumption,** (<1mW per channel)



- Recent efforts have targeted applications at the EIC, but design goals are general enough for blue-sky R&D efforts

Institution	Name	Technology	Output	# of Chan	Funding	Specific Goals	Status
INFN Torino	FAST	110 nm CMOS	Waveform & TDC	20	INFN	Large Capacitance TDC	Testing
NALU Scientific	HPSoC*	65 nm CMOS	Waveform	5 (Prototype) > 81 (Final)	DoE SBIR	Digital back-end	**V2 ready**
Anadyne Inc	ASROC**	Si-Ge BiCMOS	Discrim.	16	DoE SBIR	Low Power	**Testing**

Focus of our proposed efforts

HPSoC

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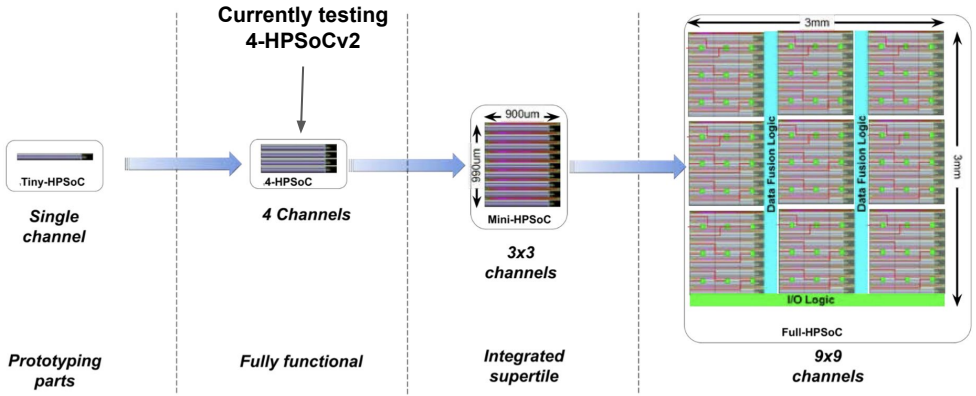
- The HPSoC design implements signal pre-amplification along with **full waveform sampling and digitization** in an ultra-small area package size compatible with small-pitch sensors
- Waveform digitization **promising technique** to reduce the noise from various sources of electronic noise to achieve timing resolution <10ps

Parameter	Specification
Channel no.	miniHPSoC chip (this proposal): 9 Full chip (post FY23): ~100 (pitch ~300µm)
Process	65nm CMOS
Sample rate	10 GSa/s
Bandwidth	2 GHz
No. bits	10
Supply Voltage	1.0V (2.5V for digital I/O)
Timing accuracy	5 ps
Front-End stage	Embedded TIA
Buffer length/channel	256 samples
Power/channel	<2mW



HPSoCv2: Preliminary results

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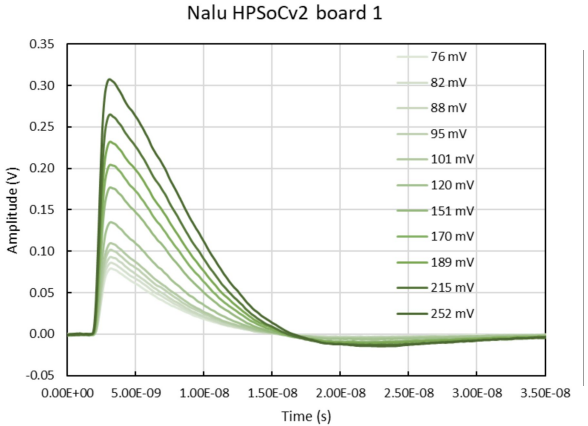
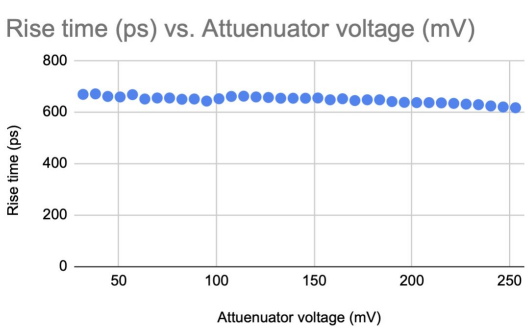
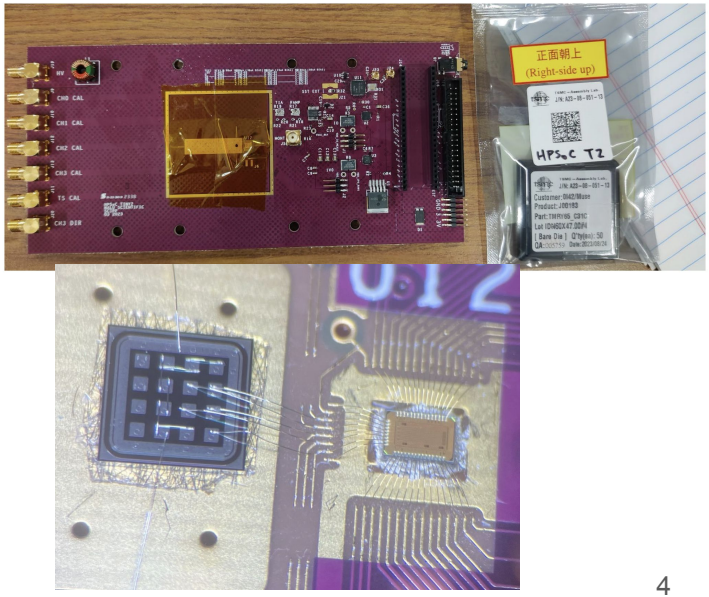
- Status: HPSoCv2 chips in hand, corresponding readout board designed & fabricated, and front-end characterization has started
- Calibration pulses injected to characterize the TIA
  - Observe rise time in the range of 600-700 ps
  - Improved gain compared to v1 chip
- Studies ongoing with ASIC+sensor+betasource

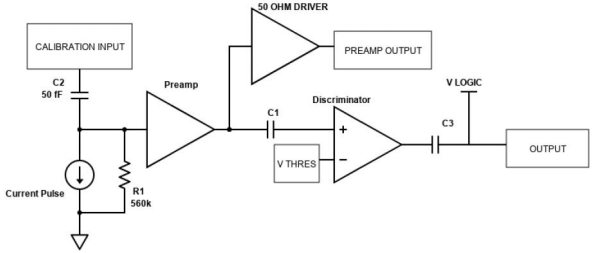


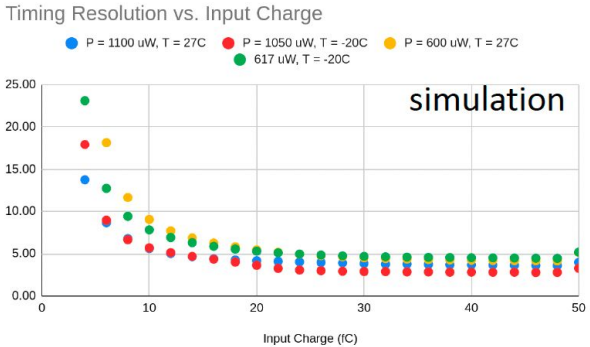




AS-ROC

- Chip developed together with Anadyne Inc. & Joey DeWitt using Tower Semiconductor Silicon Germanium (SiGe) BiCMOS technology
  - Target very low power consumption (<1mW/ch)
  - Current prototype with 16 channels output
  - Both analog and discriminator output
- **Expected jitter <10ps from simulations**
- Readout board developed by SCIPP team





AS-ROS: Status

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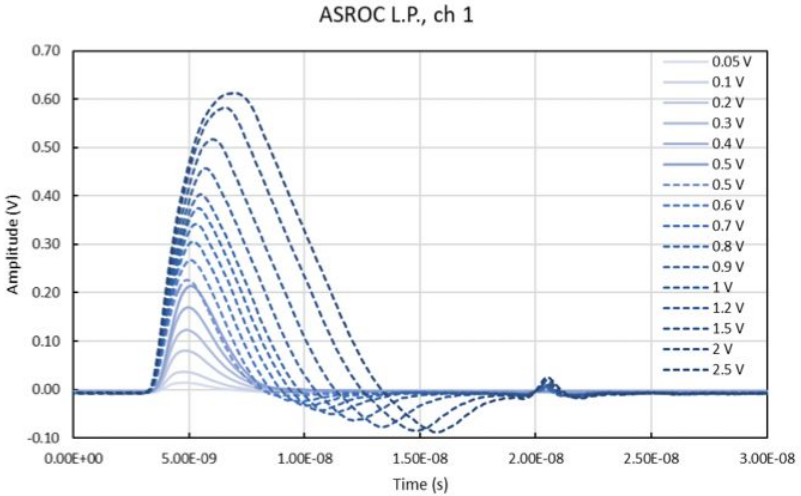
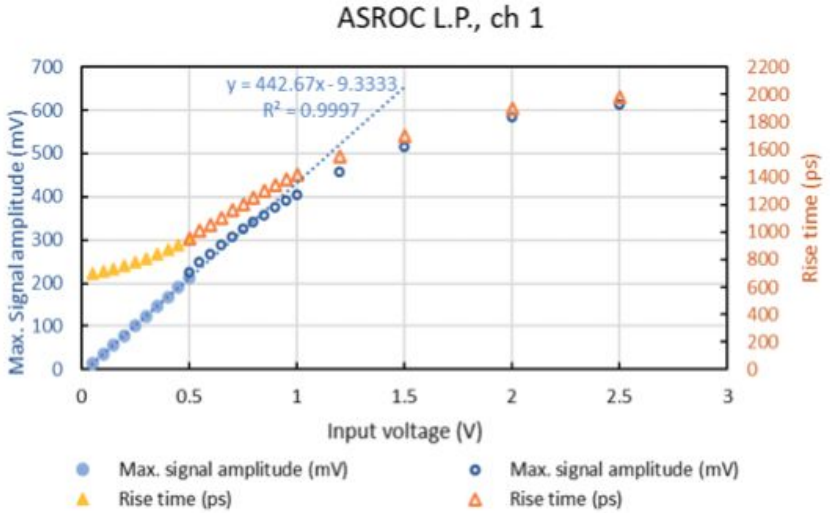
- Characterization of **analog** and digital parts well advanced
  - Good pulse shape and excellent gain for most of the dynamic range
  - Rise time from 700 ps – 2ns at saturation point





AS-ROS: Status

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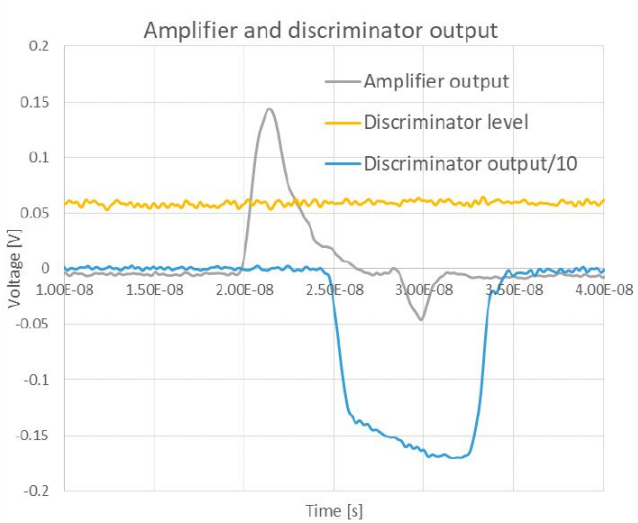
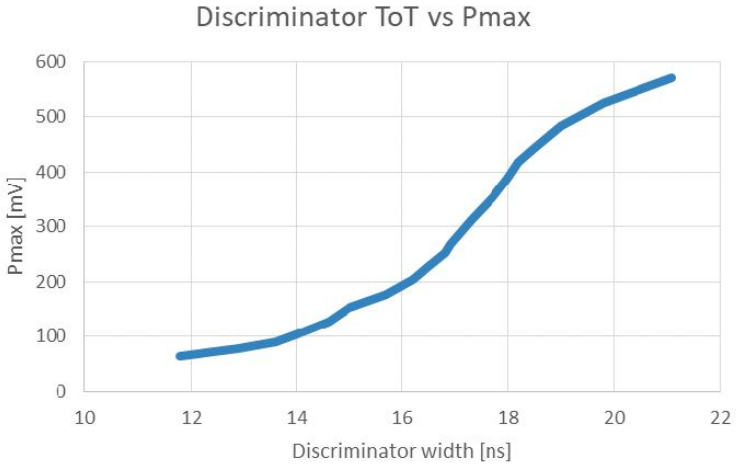
- Characterization of analog and **digital** parts well advanced
- Discriminator output functioning as expected, with jitter < 10ps
  - Discriminator output is a 1.5V step function with rise time < 1ns
  - Width proportional to pulse maximum → can be used to correct time walk





Conclusions

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- The UC Santa Cruz group is interested in continuing R&D on several promising technologies to offer low-power & excellent timing resolution for the readout of ultra-fast silicon detectors
- Two promising chips have been investigated:
  - HPSoC: implemented full waveform digitization, promise to achieve <10ps time resolution
  - AS-ROC: SiGe BiCOMS technology, promise for extremely low power consumption

UCSC ultra-fast sensor group

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