MIT Lincoln Laboratory

KIPAC
KAVLI INSTITUTE FOR PARTICLE ASTROPHYSICS & COSMOLOGY

Massachusetts Institute of Technology

SLAC NATIONAL ACCELERATOR LABORATORY

Stanford University

Single electron Sensitive Readout (SiSeRO) devices: A novel X-ray detector technology for future X-ray missions

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MIT: Mark Bautz, Eric Miller, Gregory Prigozhin

Our lab (KIPAC) and ongoing projects …

Currently focused on X-ray astronomy science (hardware work)

Athena (~2036)

- Next European X-ray flagship mission
- WFI DEPFET detector readout electronics

AXIS X-ray probe (~2032)

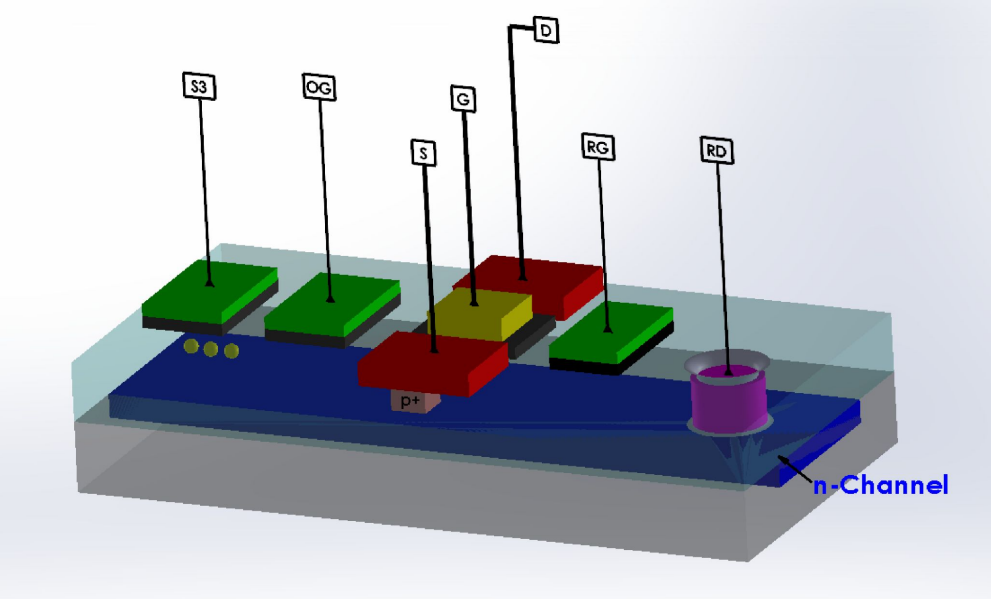
- ~$1B class NASA concept
- Development of focal plane array with MIT
- JFET based CCD detectors

Future missions

- Sub-electron noise (soft X-ray response, absolute calibration),
- very fast (large telescope),
- mega-pixel imagers

SiSeRO detectors

SiSeRO detectors (in CCD form)



Transfer channel under the p-Mosfet. Electrons in the channel modulate the transistor current [1,2]. A trough implants help confining the charge under the mosfet.

- **Higher conversion gain** than conventional CCD technology (better noise)
- Compact layout
- **KTC noise free!**
- Expected Read noise ~1 e- noise at 1 MHz speed for 1500 pA/e sensitivity.

RNDR: Possibility of measuring the same charge multiple time (repetitive Non-Destructive readout)

[1] J. Kemmer and G. Lutz, "New detector concepts," NIM-A 253(3), 365–377 (1987).
[2] Matsunaga, H. Yamashita, and S. Ohsawa, "A highly sensitive on-chip charge detector for ccd area image sensor,"
IEEE Journal of Solid-State Circuits 26(4), 652–656 (1991)

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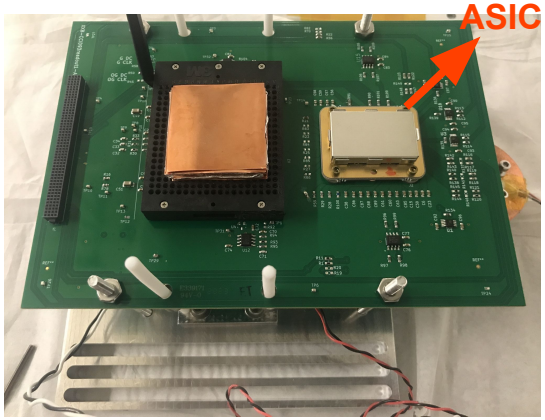
Readout electronics

At SU, we developed a readout module to characterize the SiSeRO devices.

- Drain current readout.
  - Discrete and ASIC readout system
    - An I2V preamp followed by an ADC driver
- Simulations:
  - The bandwidth ~ a few MHz
  - Noise: <1 pA / sq(Hz) current density

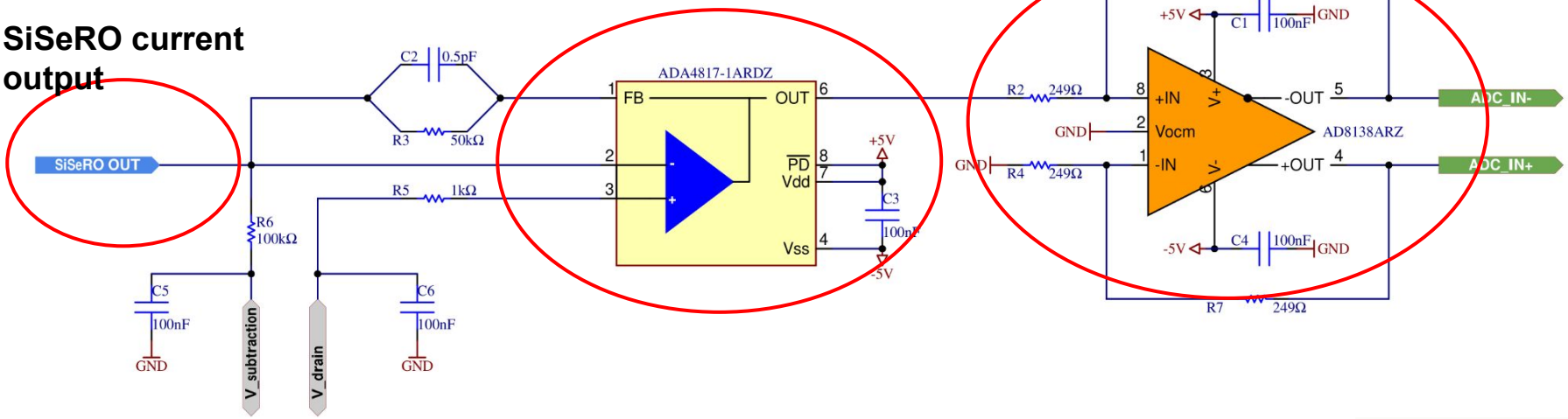


Detector Board carrying an ASIC

Differential Amp to ADC

Current to Voltage

SiSeRO current output



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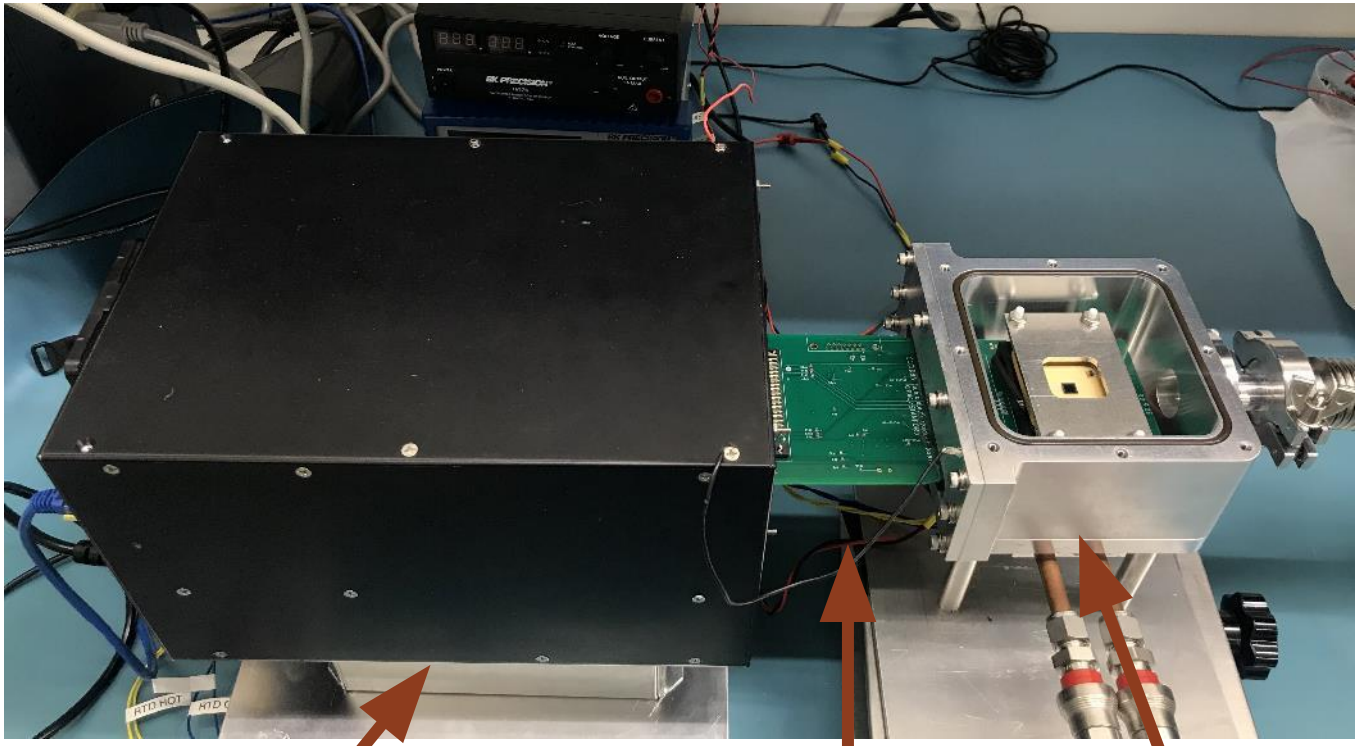
Test Setup ("Tiny box") for SiSeRO



STA Archon controller supports raw data mode for full video waveform capture

PCB with amplifier and support electronics

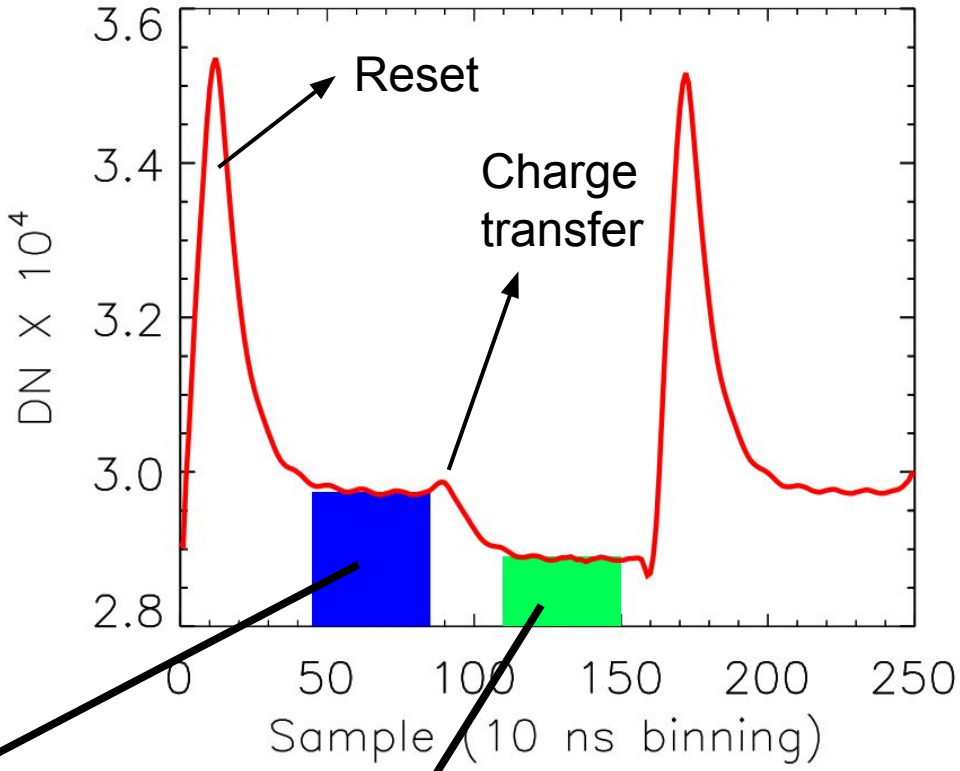
Detector module in vacuum & cooled by TEC (-40 C)

SiSeRO waveform

Parameters to optimize:

- **Rg, RD bias**
- **OG**
- **MOSFET Source, Drain, Gate bias**

625 kHz readout (1.6 us pixel)



Pre-charge transfer

Post-charge transfer

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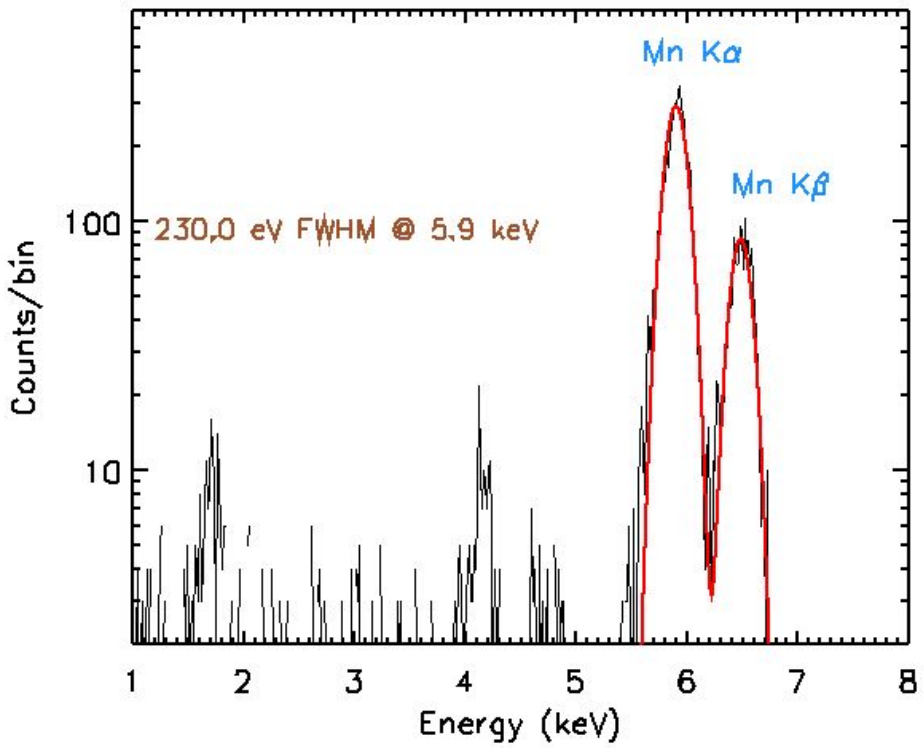
Spectral and noise performance for a SiSeRO prototype (surface channel)



Results

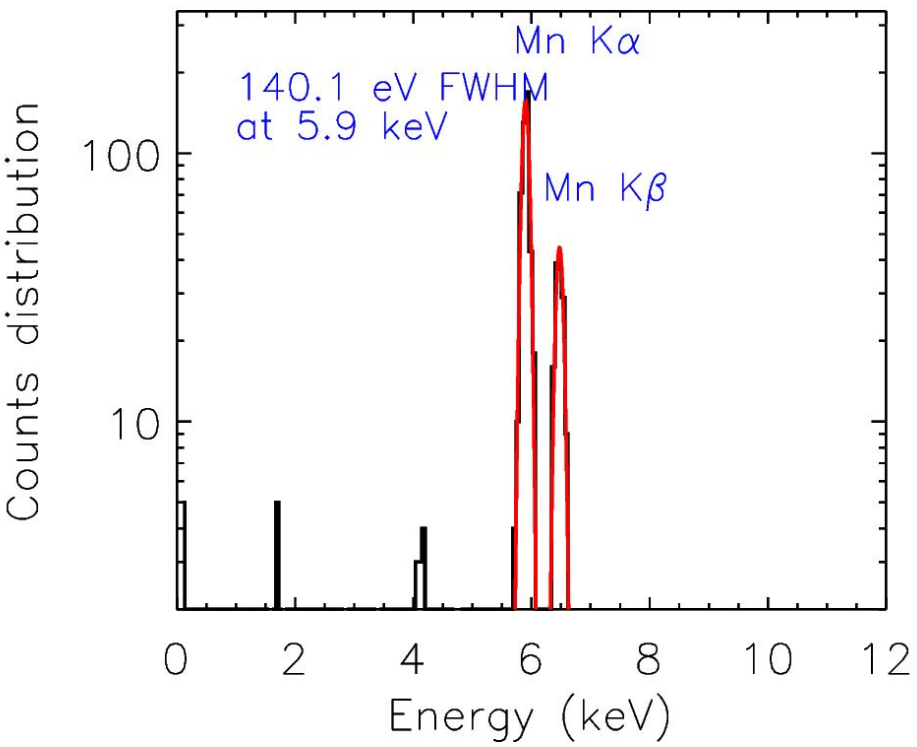
- **Read noise -** 15 electrons RMS
- **Spectrum -** 230 eV FWHM@5.9 keV (centered)
- **Gain** – 700 pA / electron
- **Transconductance -** 20 uS

The prototype uses a surface transistor channel (Higher noise from trapping and detrapping of carriers in the Si interface states)

First results for a SiSeRO device!

(Chattopadhyay et al. 2022, JATIS)

First generation SiSeRO results (buried channel)



(Chattopadhyay et al. 2023, JATIS)

A buried channel SiSeRO

- The transistor channel conduction is below the surface
- No excess noise from trapping and de-trapping of charge carriers from the Si interface states

Results

- **Read noise -** 4.1 electrons RMS
- **Spectrum -** 140 eV FWHM@5.9 keV
- **Gain** – 800 pA / electron
- **Transconductance -** 25 uS

Substantially improved (competitive) performance!

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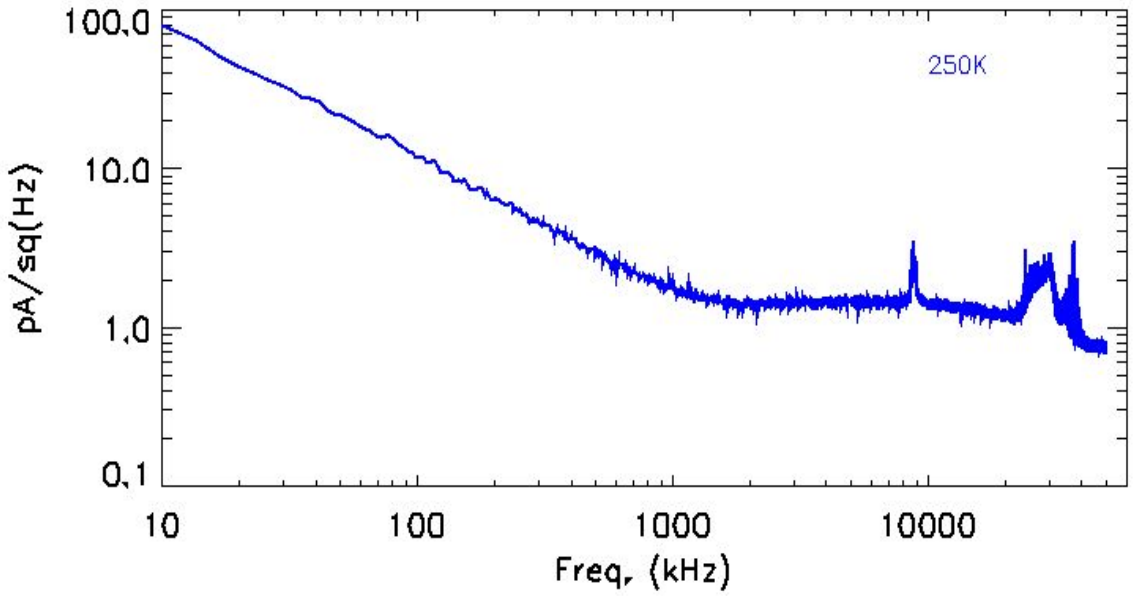
1/f noise in first generation SiSeROs

SiSeRO noise spectral density

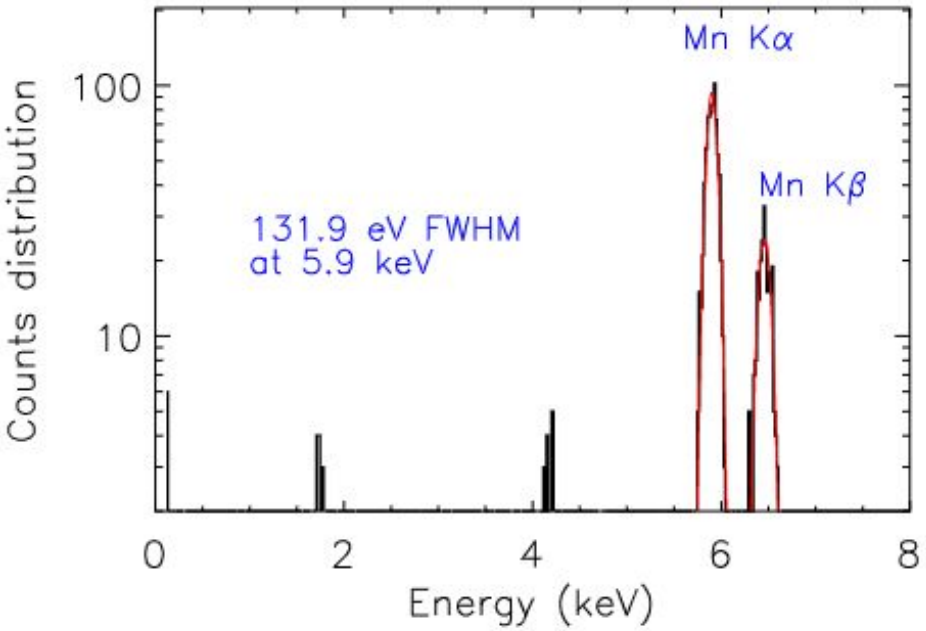


- Thermal noise floor < 2 pA/√Hz current noise density.
- Large 1/f noise with corner frequency ~ 1 MHz

Flexibility of saving raw digital waveforms from the Archon controller

- FFT on the digital waveform (10 ns sample size)

1/f noise in SiSeROs: Digital CDS filtering



Digital filtering

- low frequency correlated noise affects the baseline and signal levels leading to additional noise after CDS.
- Therefore the **default box** filter (sinc response in the frequency domain) is not ideal when noise is dominated by both thermal and 1/f noise
- **FFT filter: An optimized digital CDS filter to suppress the 1/f noise.**

- Noise improved by ~15-20 % to **3.5 e- RMS**
- FWHM improved to **132 eV @ 5.9 keV**

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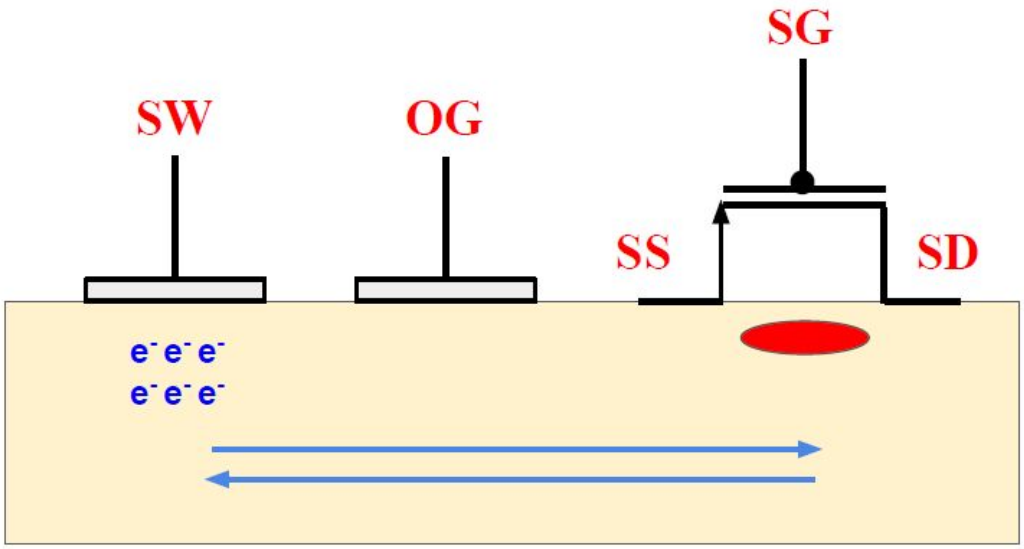
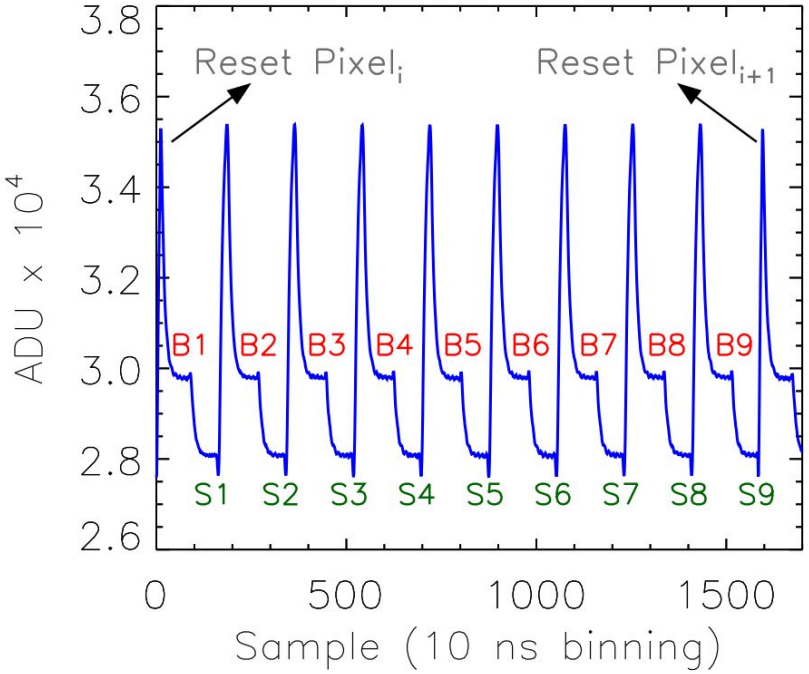
RNDR in SiSeROs



- Charge signal remains unaffected during the readout
- For N measurements, Noise ~ 1/ √N
- Clocked the output gate (OG).



- **9 RNDR cycles: 9 baselines and 9 signals**
- **each pixel is 16 us - readout speed is ~63 kHz**

First demonstration of RNDR on the SiSeRO devices **!**

Chattopadhyay 2022 SPIE, 2024 JATIS

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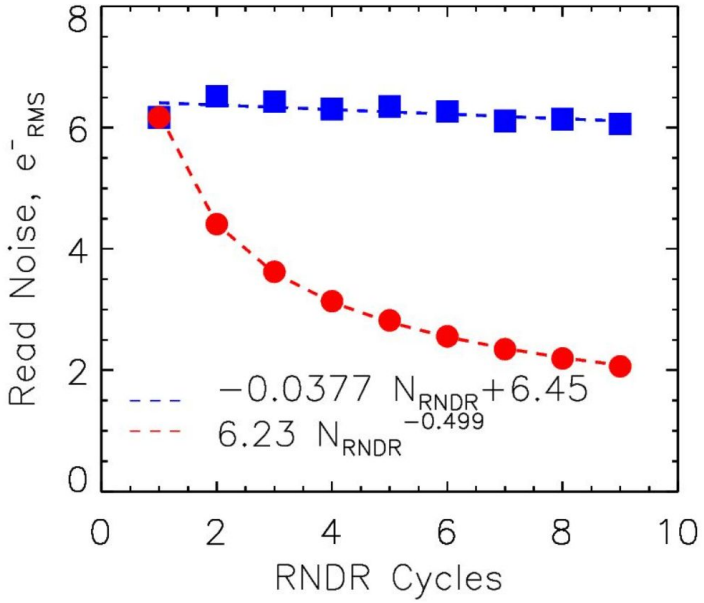
First RNDR results in SiSeROs

- 9 RNDR cycles (each pixel 16 us; 63 kHz readout)
- Read noise for 9 Individual cycles almost constant !
- **Final noise is 2 e- RMS from 6 e- RMS**
- **The final FWHM @ 5.9 keV is 124 eV** ~ close to the Fano limit



Blue: individual measurements.
Red: averaged measurements.

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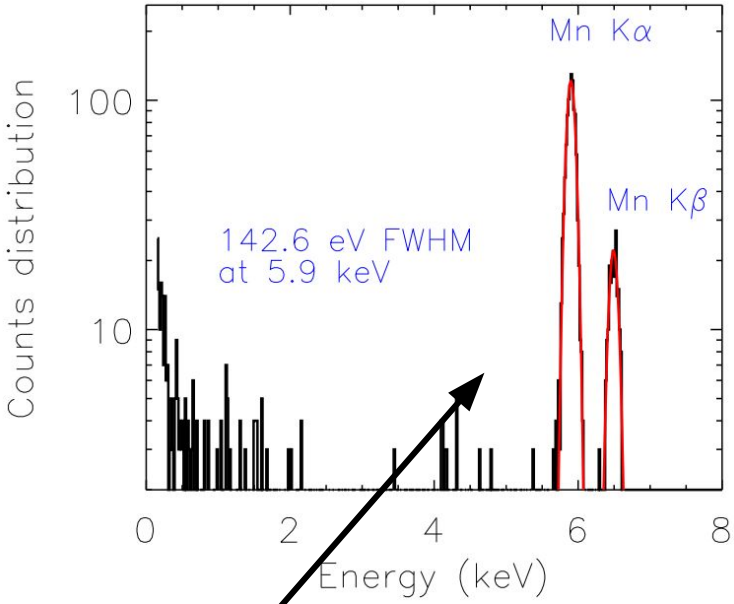

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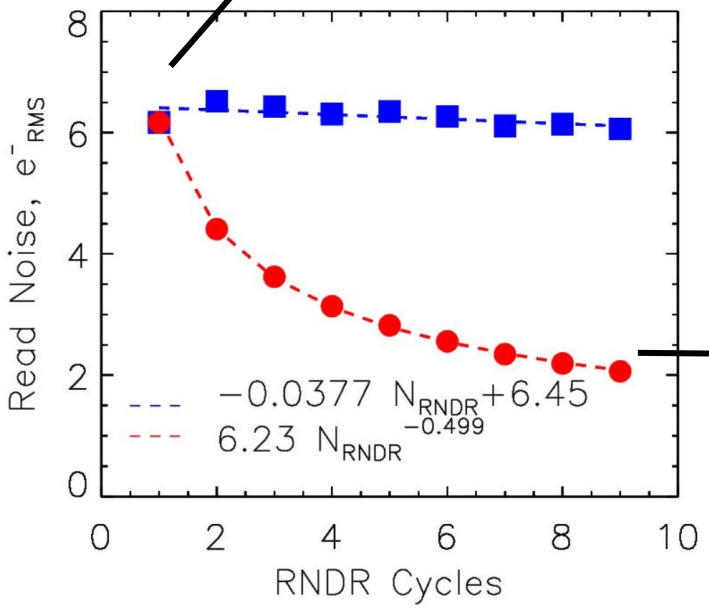

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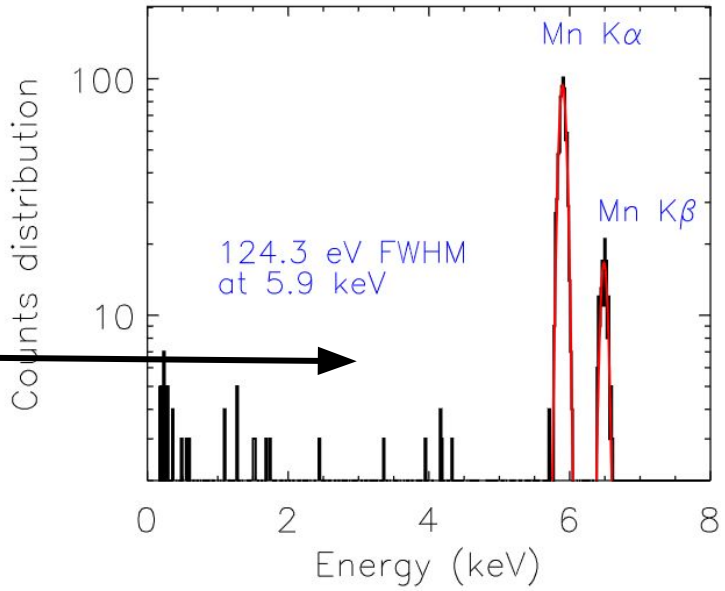

Chattopadhyay 2022 SPIE, 2024 JATIS

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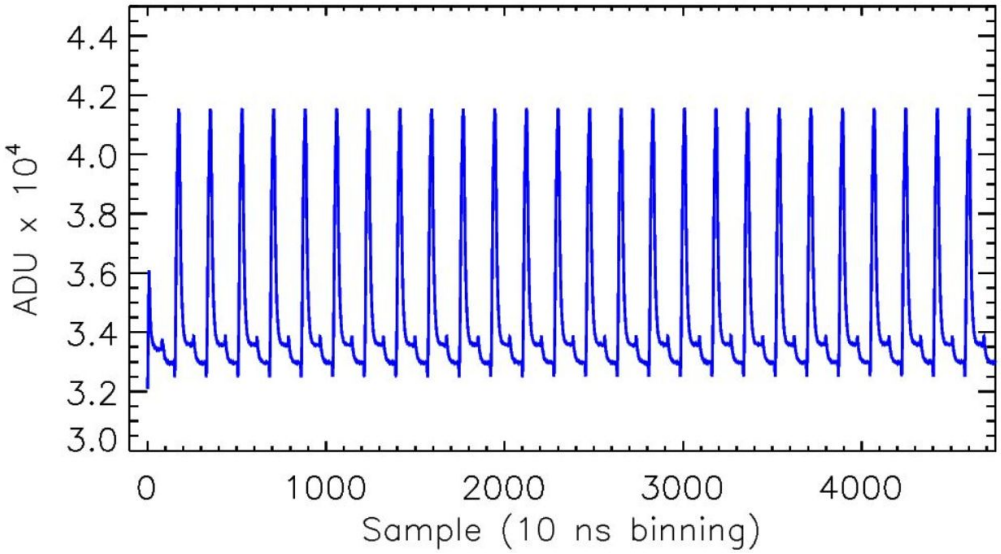
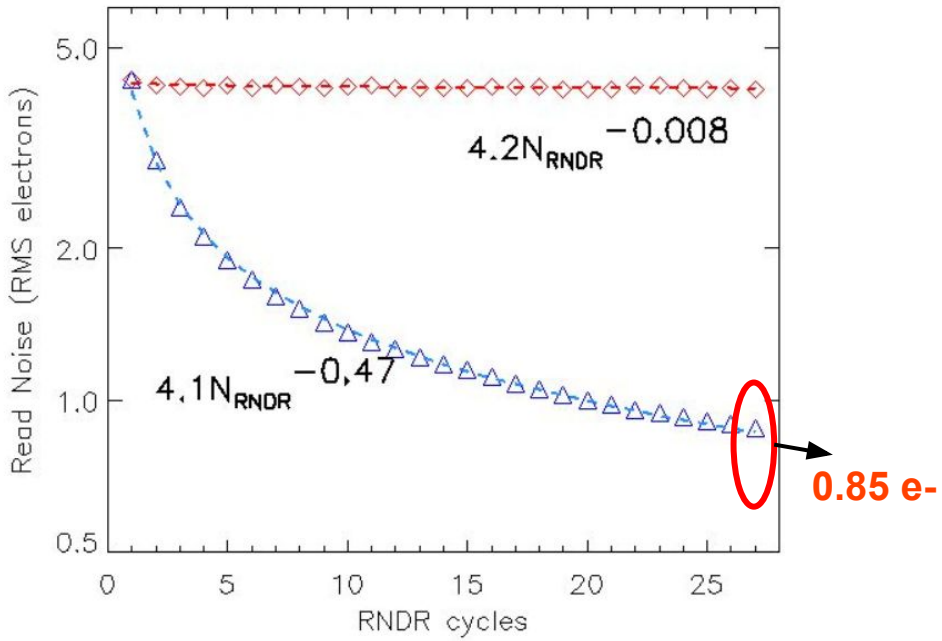
Latest RNDR results: sub-electron noise





Chattopadhyay et al 2024 (in prep)

- **27 RNDR cycles (~50 us pixel, 21 kHz readout)**
- **Read noise and gain for 27 Individual cycles almost constant - no charge loss**
- **The averaged noise follows 1/√N trend**
- **Final noise is 0.85 e- RMS**

Note: FNAL/LBL group have also demonstrated sub-electron noise with n-mosfet SiSeRO variant (hole collecting CCD)

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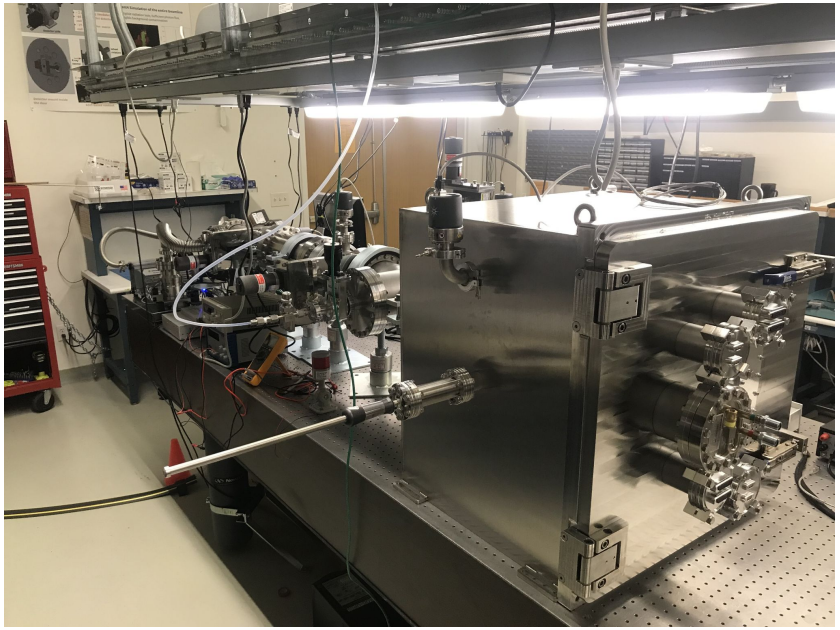
Improved test facilities for RNDR

Experiment in the beamline (-100 C)

- Current tests are done at -40 C, so limited to 27 cycles to control the thermal leakage
- Beamline cryocooler can provide -100 C
- Setup utilizes ASIC readout system.
  - supports up to 16 outputs
- Target ~200 RNDR cycles
- Expected noise ~ 0.3 e-



3 meter long X-ray beamline

- **-100 C cooling**
- **Multiple mono-energy line in 0.67 - 8 keV**

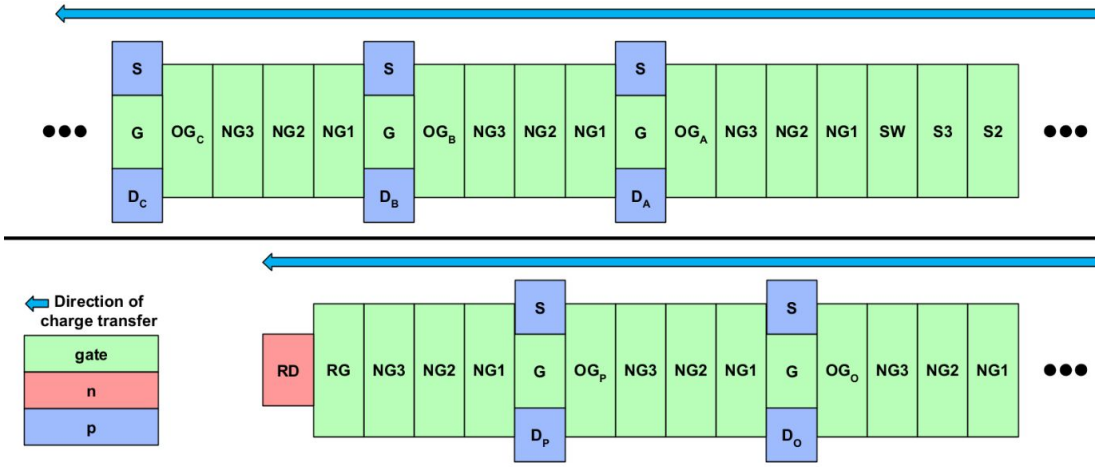
Novel SiSeRO designs under fabrication!

512 x 512 pixel device with 16 SiSeRO outputs

- testing 4 different amplifier variants
  - Improved buried channel design
  - Trough location optimization
  - Better isolation of the MOSFET

Amplifier cluster of 16 SiSeROs in series

- 16 SiSeROs in series at the output
- A factor of 4 improvement in noise at the same readout rate
- Available by the end of 2024! (ASIC based readout)
- FNAL/LBL also exploring similar concept



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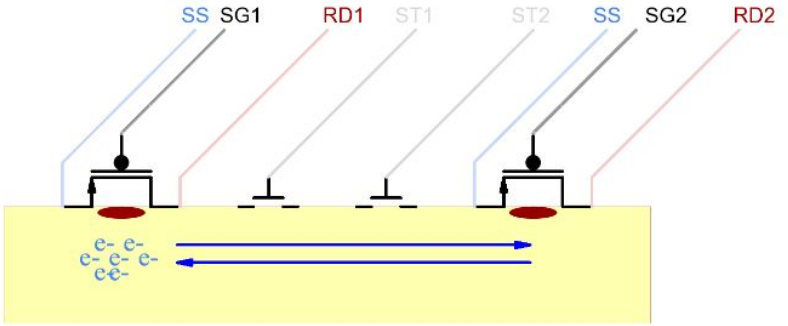
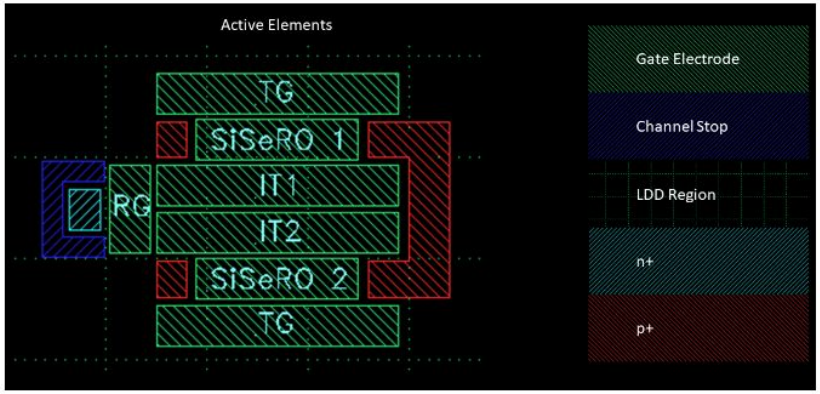
Active Pixel SiSeRO sensor

Preliminary SiSeRO matrix in fabrication

- **Combines the proven X-ray performance of CCDs with the architectural advantages of active pixel sensors**

- 2 adjacent SiSeROs as an unit
- Better charge transfer
- Effectively twice the RNDR cycles for the same integration





Full 64 x 64 SiSeRO matrix in development

- NASA APRA proposal submitted
- Uses Readout ASIC + Switcher ASIC scheme

Summary and Future plans

- **SiSeRO is a novel output stage for CCDs:**
  - Fabricated at MIT-LL using the established MIT-LL CCD process technology.
  - Charge at the back gate of a p-MOSFET modulates the transistor current.
  - Improved gain and responsivity compared to conventional CCD output stages.

- **Characterization of SiSeROs with drain readout at Stanford:**
  - Encouraging results for buried channel SiSeROs ! 3.5 e- read noise, 130 eV FWHM at 5.9 keV for single read measurements.
  - Demonstrated RNDR! Sub-electron noise with 27 RNDR cycles.

- **Development path for SiSeRO technology**
  - Next generation SiSeROs currently in fabrication.
    - Multiple (16) SiSeRO outputs on a single CCD
    - Multiple (16) SiSeROs in series at CCD output
    - First SiSeRO active pixel matrix (APS).

SiSeRO technology opens a path towards fast, sub-electron noise, megapixel spectral-imaging for X-ray (and other) applications!