CPAD Workshop 2023

Tuesday, 7 November 2023

RDC5: Session #1 (Trigger and DAQ) - 51/3-305 - Kavli 3rd Floor (16:00 - 18:00)

-Conveners: Jinlong Zhang; Zeynep Demiragli

time	[id] title	presenter
16:00	[248] Introduction to RDC5	ZHANG, Jinlong DEMIRAGLI, Zeynep
16:20	[92] Empowering AI Implementation: The Versatile SLAC Neural Network Library (SNL) for FPGA, eFPGA , ASIC	DAVE, Abhilasha
16:40	[11] Machine learning based developments for LHC level-1 triggers	DASU, Sridhara
17:00	[250] Future detector readout	PARAMONOV, Alexander
17:20	[264] LuSEE Night Electronics Design	KOTOV, Ivan

Thursday, 9 November 2023

RDC5: Session #2 - 51/3-305 - Kavli 3rd Floor (16:00 - 18:00)

-Conveners: Jinlong Zhang; Zeynep Demiragli

time	[id] title	presenter
16:00	[82] HLS In A DAQ Environment	RUSSELL, J.J.
16:20	[36] hls4ml: deploying deep learning on FPGAs for L1 trigger and Data Acquisition	LIU, Mia
16:35	[73] An Open Source General Purpose DMA Engine For DAQ Systems	HERBST, Ryan
16:50	[266] Portable Acceleration of CMS Mini-AOD Production with Coprocessors as a Service	LIU, Mia
17:05	[156] Yet Another Rapid Readout - For ATLAS Inner Tracker during HL-LHC	RASTOGI, Angira
17:20	[186] An In-Network Event Builder for the Mu2e TDAQ System	CUMMINGS, Sean
17:30	[265] Rogue: Back-End Integration and Future Developments	MORENO, Omar
17:45	[249] Discussion	