CPAD Workshop 2023

Tuesday, 7 November 2023

RDC4: Session #1 - (Readout and ASICs) Circuits and Architectures for 4D Tracking and Calorimetry - 48/1-112C/D - Redwood C/D (13:30 - 15:30)

-Conveners: Mitch Newcomer; Angelo Dragone

time	[id] title	presenter
13:30	[220] Introduction: RDC4 and work planning	DRAGONE, Angelo NEWCOMER, Mitch
13:45	[150] From ETROC to VTROC (Vertically integrated Timing ReadOut)	LIU, Tiehui Ted
14:00	[51] Towards 4D tracking: 28nm sub-10ps TDC ASIC design and characterization setup	RUCKMAN, Larry
14:15	[87] CMS High Granularity Calorimeter ECON-D ASIC overview and radiation testing results	CUMMINGS, Grace
14:30	[63] SiGe integrated chip readout for fast timing	SAFFIER-EWING, Gabriel GALLOWAY, Zachary
14:45	[111] Pebbles: paving the way toward 4D Pixel detectors in 28nm CMOS	HEIM, Timon
15:00	[137] Readout IC R&D for future Phase III High Luminosity Upgrade of the LHC	PARPILLON, Benjamin
15:15	[24] Design, Testing, and Applications of the Fermilab CFD Readout ASIC	XIE, Si

Wednesday, 8 November 2023

RDC4: Session #2 - Big Data Management - 53/1-1350-A - Trinity-A (13:30 - 15:30)

-Conveners: Angelo Dragone; Julia Gonski

time	[id] title	presenter
13:30	[223] ASIC and Electronics Workforce Development	NEWCOMER, Mitch
13:50	[31] Exploration of Resource-efficient Implementations of ML Models Targeting eFPGAs	JOHNSON, Jyothisraj
14:05	[53] Developments of Reconfigurable Digital Logic in the ASIC using 130nm and 28nm CMOS	RUCKMAN, Larry
14:20	[158] Emerging approaches for a flexible and energy-efficient readout	PUROHIT, Prafull
14:35	[93] Front-end neural network filtering implemented in a silicon pixel detector	YOO, Jieun
14:50	[211] Machine-Learning-Based Regression for Edge Data Reduction of Small Pixel, High-Bandwidth Silicon Detectors	BENOIT, Mathieu
15:05	[225] Kicking our Veto Addiction: Accelerating Edge Computing for Tailored Lossy Compression	COFFEE, Ryan
15:20	[226] Work packages planning	

RDC4: Session #3 - Cryogenic and Deep Cryogenics - 53/1-1350-A - Trinity-A (16:00 - 18:00)

-Conveners: Mitch Newcomer

time	[id] title	presenter
16:00	[227] Cold Electronics: Progress and Potential	GRACE, Carl
16:20	[127] CryoCMOS modelling and PDK development for GF 22 FDX	SEIDEL, Olivia
16:35	[144] Scalable SNSPD cryogenic readout	BRAGA, Davide
16:50	[110] RFSoC-based Readout and Characterization Platform Development at SLAC	LIU, Chao
17:05	[130] Front-end Application Specific Integrated Circuits (ASICs) in 65 nm CMOS for Charge and Light Readout	MUKIM, Prashansa
17:20	[42] Frequency Multiplexing of Cryogenic Sensors for the Ricochet Experiment	VAN DE PONTSEELE, Wouter
17:35	[178] Advanced time-division transition-edge sensor readout development for CMB-S4	HENDERSON, Shawn
17:50	[230] Work Packages Planning	

Thursday, 9 November 2023

RDC4: Session #4 - Methodologies, Tools, IC blocks, SoCs and Workforce Development - 48/1-112C/D - Redwood C/D (13:30 - 15:30)

-Conveners: Angelo Dragone; Mitch Newcomer

time	[id] title	presenter
13:30	[228] DRD7 Perspective on R&D for ASIC and Electronics	VASEY, Francois
13:50	[96] 3D Heterogeneous Integration Multi-Project Wafer	FAHIM, Farah
14:05	[81] Rapid Firmware/Software Development with SLAC's Open-Source Tools: SURF, RUCKUS, and ROGUE	HERBST, Ryan
14:20	[219] DC-DC Converters Using New Materials and Architectures	Mr NIKOLICA, Adrian
14:35	[191] Design Updates for HPSoC: A very high Channel Density Waveform Digitizer with sub-10ps resolution	OTT, Jennifer
14:50	[77] CRYO ASIC: A System-on-Chip (SoC) for Charge Readout in the nEXO Experiment	PENA PEREZ, Aldo
15:05	[135] An input buffer for PSEC5 – a waveform sampling ASIC – in 65nm CMOS Technology with a 5GHz analog bandwidth	YEUNG, Richmond
15:20	[229] Work Packages Planing	