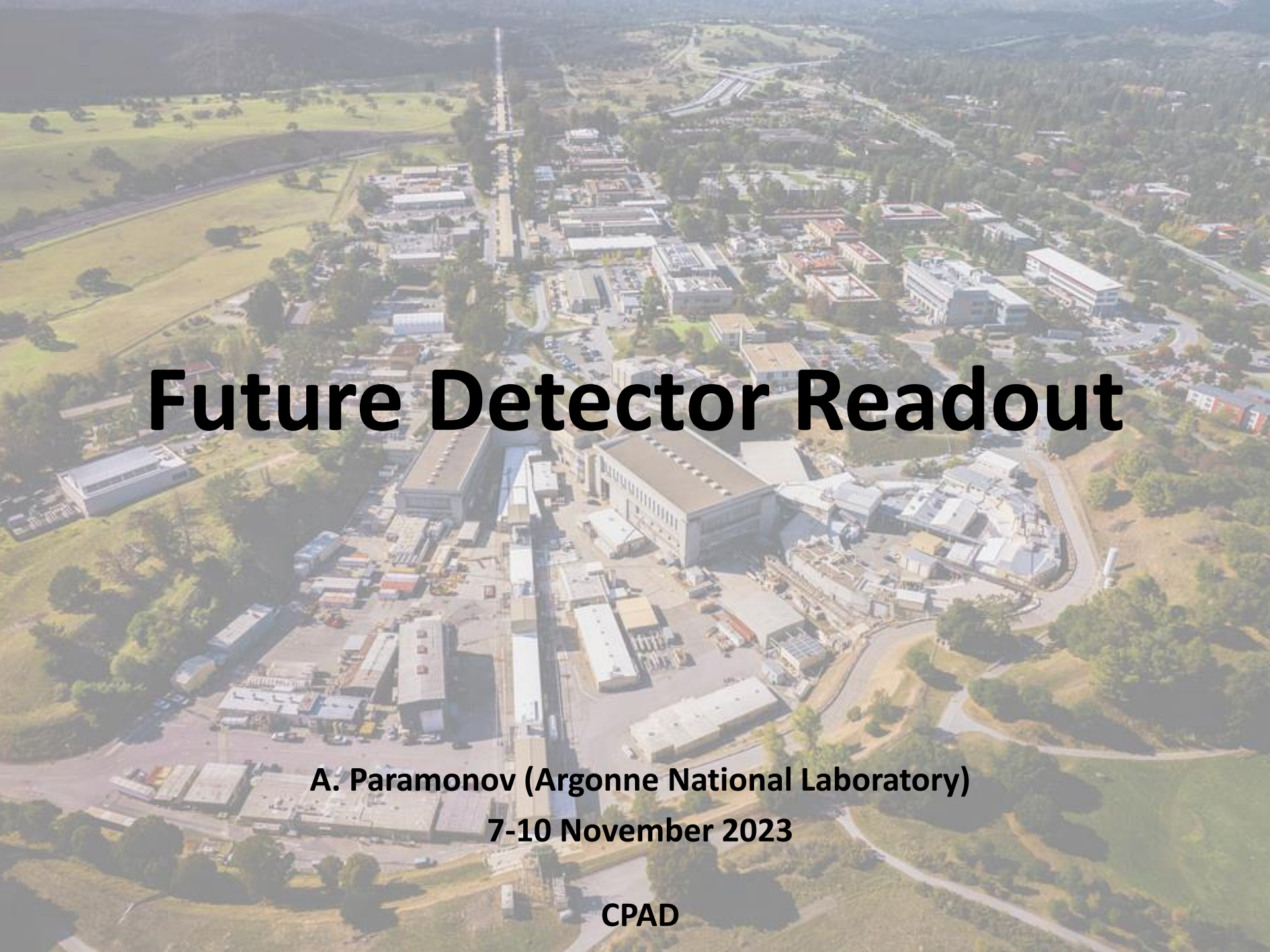

Future Detector Readout

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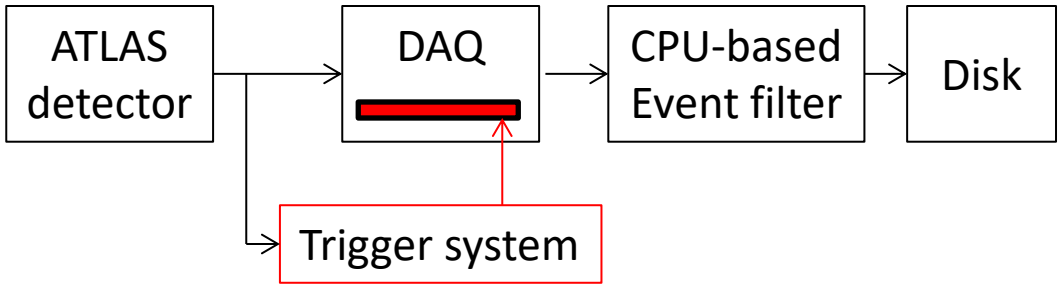
7-10 November 2023

CPAD

Vision

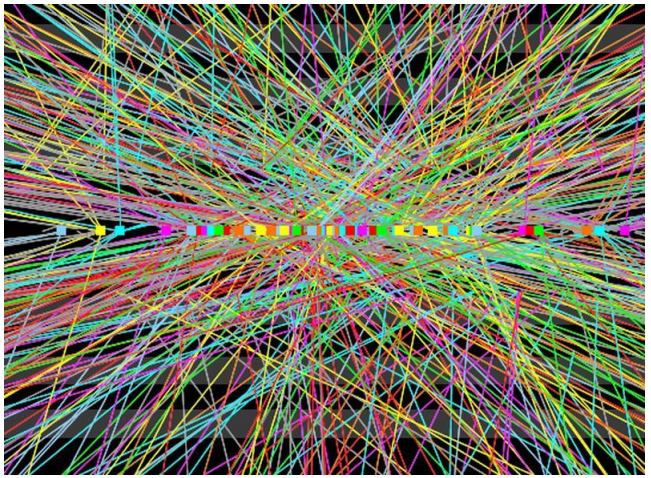
- **Future collider experiments will be capable of triggerless detector readout (all data for each bunch crossing**)
- Why triggerless?
  - Utmost discovery potential.
  - Simplicity of the whole detector design (fewer custom boards, no on-detector buffering)
  - Effort and design cycle (design and support of boards, firmware, & algorithms).
- Why ATLAS and CMS are not triggerless already?
  - Readout of the tracking (inner) detectors is the major challenge because of the high data rate and radiation environment.
- However, the emerging link technologies and advances in on-detector data processing can enable the future collider experiments to be triggerles.



From-detector data links

- As an example, let's take a look what would be needed to make the ATLAS experiment triggerles.
- Readout of the tracking detector is the show-stopper. The data links need to be faster and more radiation-hard.
- The innermost layer of the ITk pixel detector is the hardest case because of the large data volume.
- There are two handles to read it out for every bunch collision:

1. **Brute force (bandwidth).** One ITkPIx ASIC outputs 5.12 Gb/s of data for a MHz trigger rate. Naively scaling by 40 gives 200 Gb/s per ASIC.
2. **Intelligence**. Can we reduce data volume that needs to be transmitted off-detector? This can be done via data processing or compression.

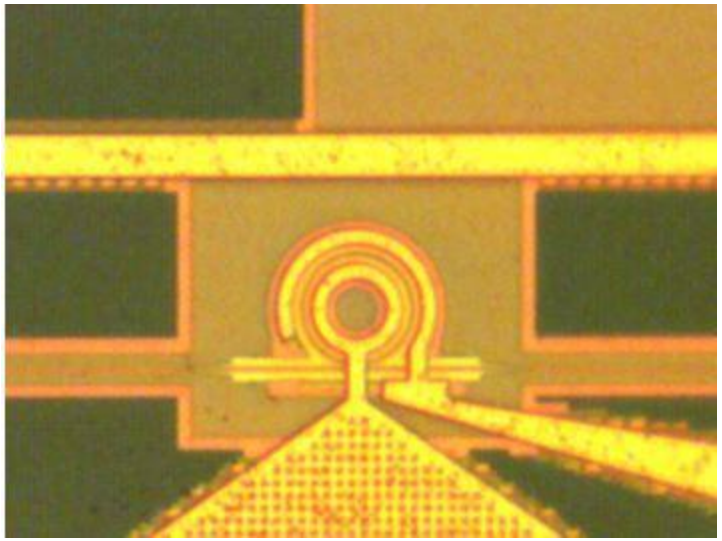


To-detector Links

- Transmission of data to detector (configuration and calibrations) is not a challenge.
- However, clock distribution for 1-psec timing detectors is harder.
  - For example, the propagation delay from USA 15 to ATLAS changes by ~100 psec for a degree C change in the ambient temperature. Electrical cables are affected too. → **The downlink needs time compensation** (correction for the propagation delay).
- The link data format should offer robust clock recovery. DC balance of scrambled data (e.g. in GBT and lpGBT) has largu fluctuations. 8b/10b offers much better DC balance and, therefore, robust clock recovery.
- The uplink may use the recovered clock from the downlink to allow measurements of the propagation delays.

Link technologies

- What are the requirements besides data rate and radiation tolerance (does not need for be as high for ee colliders)?
  - The links should not compromise detector performance due to dead material or power consumption.
  - Some HEP experiments (e.g. DUNE) need cryogenic-capable links.
  - High reliability (long service life and low failure rate).
  - Affordable
- Si-photonics technology checks all these boxes.
- Wireless data links are also interesting.
- Si photonics is highly customizable and affordable but close partnership with industry is needed for manufacturing and integration of photonic chips.
- Selected elements of the Si-pho PDK need to be revised for radiation tolerance.



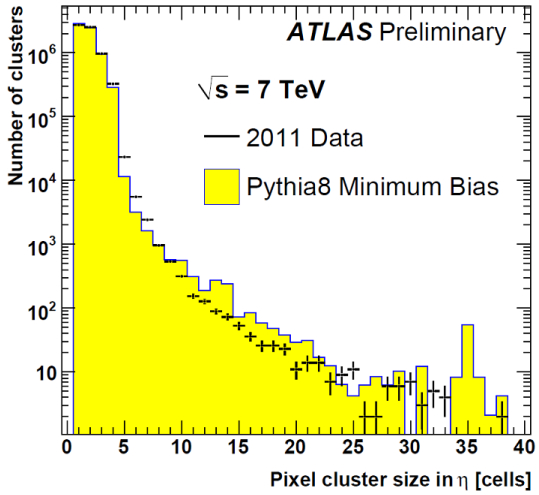
https://ep-news.web.cern.ch/content/silicon-photonics-high-energy-physics-experiments

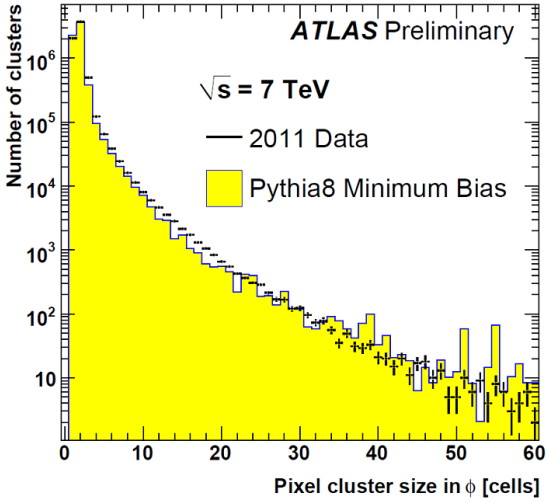
On-detector intelligence

- There are strong incentives to reduce the data volume.
- Again, on-detector data processing should not compromise detector performance because of the power consumption, extra material, or single event upsets. It requires balance.
- In some cases intelligent data processing may allow reduction of power consumption (fewer signals to digitize, smaller clock fan-out network, less data to move across ASIC).
- R&D for on-detector intelligences (AI/ML) is ongoing at many institutions. They are exploring different kinds of architectures ranging from conventional CNs (all digital) to analog and neuromorphic.

Intelligence for imaging detectors

- As a simple example. we can train AI to combine neighboring pixels into groups (aka clusters) so that the ASIC would output cluster parameters instead of individual pixels. A cluster corresponds to a particle crossing of the sensor.

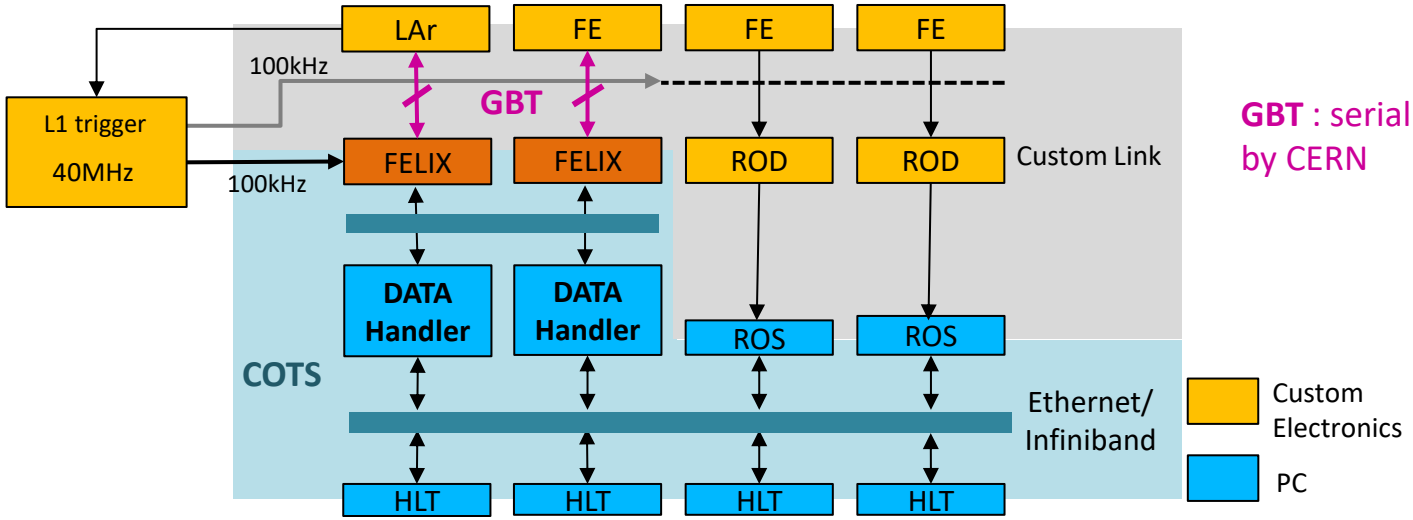




- Further, we can filter out noise and clusters consistent with low-momentum particles. Filtering of clusters from soft particles works best for the outer layers.
- There are other ideas that go beyond single ASIC.

What's happening off-detector?

- The rapid evolution of commodity switched networks and CPUs allowed us to reduce complexity of the ATLAS DAQ system. It uses FPGAs only on the custom-commodity boundary.

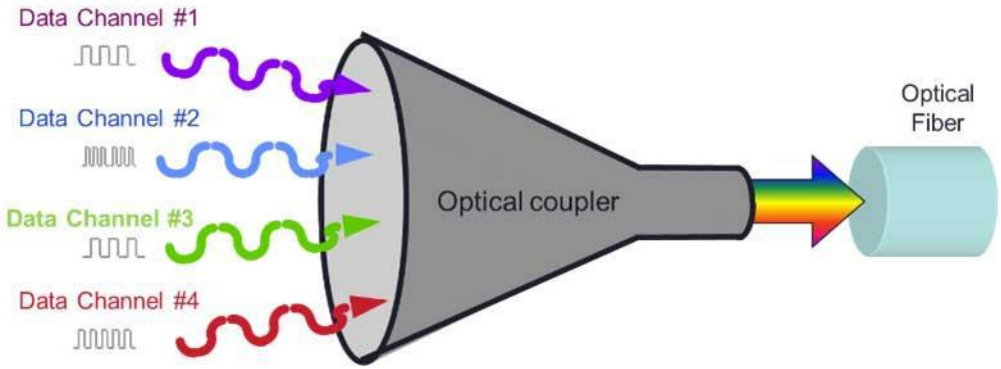


GBT : serial protocol designed by CERN

- The future detectors will likely rely on the same approach as the on-detector systems need to be synchronous to the collider beam structure.
- Future FPGAs and commodity computing should easily handle triggerless DAQ when for the future experiments are build.
- In some cases commodity (Ethernet) links can go directly to detector.

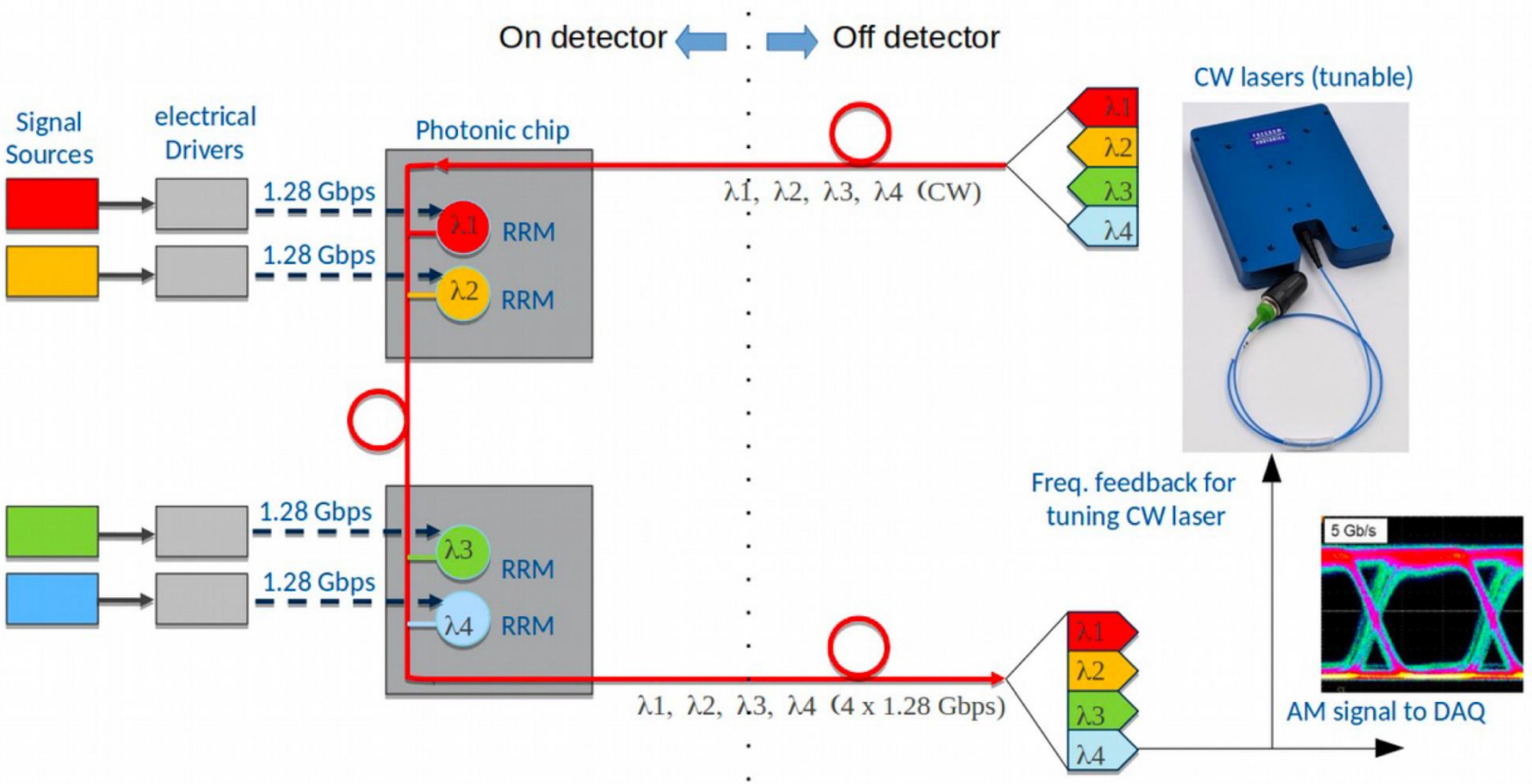
Data aggregation

- Output per pixel ASIC gets lower about 16 times for the outermost ITk pixel layer of ATLAS. It gets even slower for ITk Strip detector.
- Therefore, we should be able to aggregate sloer links to keep the number of long fibers (between the detector and the counting room) low.
- Fiber needs to go directy to the pixel ASIC for the innermost layer.
- Fiber also needs to go to timing layers unless there is some time compensation for electrical links.
- For outer layers, where the link speed is low. Data can be distributed via electrical links to an aggregation point.
- Data aggregation can be via WDM as discussed in arXiv:2203.14894



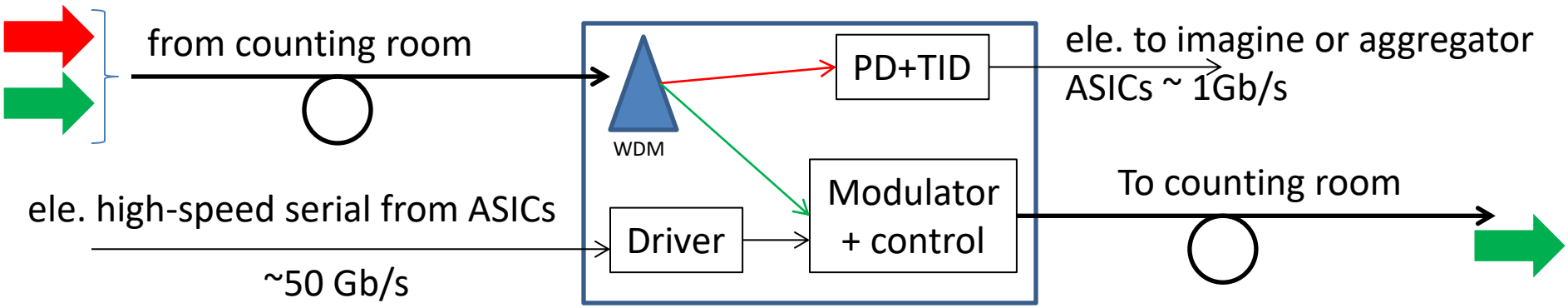
Rad-hard Si-pho WDM link

- SBIR with Freedom photonics.
- Data aggregation and modulation happens on the same wafer. One fiber in and one fiber out. Ring resonators have small footprint.



Photonic chip+

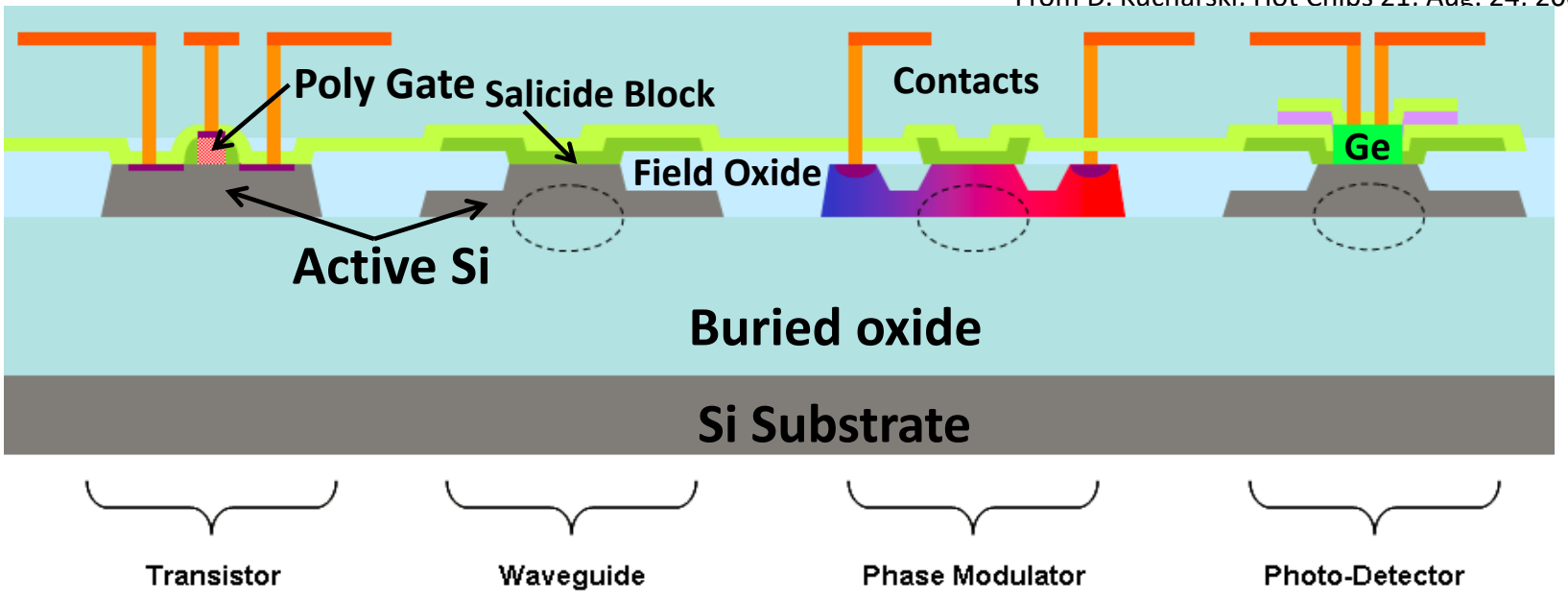
- Si-photonic waveguides and the other element (lenses, modulators/resonators, polarisers, etc) can be manufactured with larger feature size Si-on-insulator processes (CMOS) than conventional circuits. The waveguide dimensions are fixed by the wavelength of light.
- The slower circuitry (e.g. for the downlink and recovered clock) can be packaged into the same chip.
- The high-speed serialiser (and perhaps the resonator driver) needs to be external.
- The light source (laser) needs to be external (not rad-hard).
- The downlink fiber is shared by data and the light source (for the uplink).



Si photonics technology uses a commercial CMOS SOI process (see 10.1109/JSSC.2007.908713 or 10.1109/OFC.2008.4528356). The optical elements are:

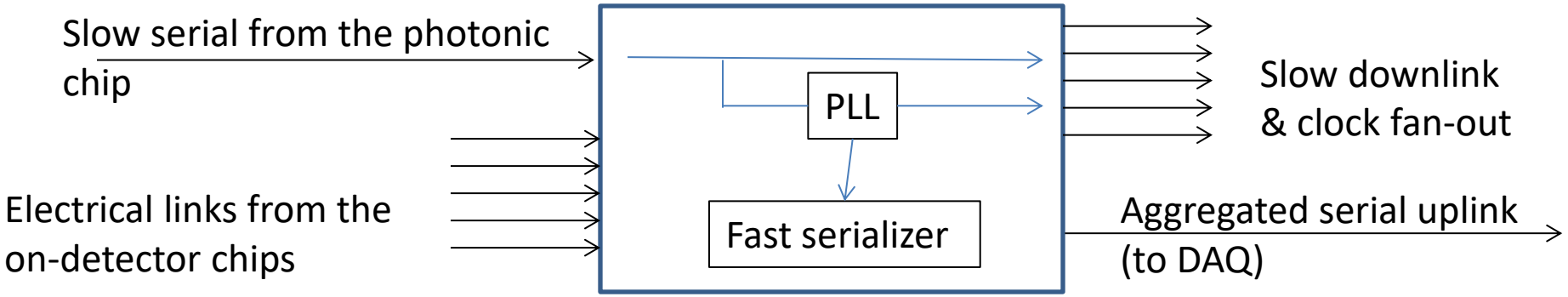
- Passive waveguides (losses<0.1 dB/cm) → interconnects between other optical devices.
  - Utilize the high index of refraction between Si and SiO_2.
- Phase modulators → Used in the MZI-based amplitude modulators
  - The refractive index of Si depends on the free carrier density (electrons and holes)
  - Implemented as a PN diode structure by using implants
  - Bias the PN diode to change the phase
- High-speed photo detectors
  - Selective growth of Ge on top of the Si waveguide.
- Low-loss grating couplers, holographic lens (efficiency ~ 95%)
  - Used to couple light in and out of the Si die
  - Redirect light from horizontal direction (die) to vertical (fiber)

From D. Kucharski, Hot Chips 21, Aug. 24, 2009



Electrical (aggregator) chip

- The electrical chip is needed to
  - recover clock,
  - fan-out the electrical down-links, and
  - Aggregate electrical links
- The electrical downlink can be shared by a group of imagine ASICs. The downlink data format should allow addressing them individually in broadcast.
- Can the uplinks be aggregated without decoding them (e.g. just with a multiplexer-serializer)? Can we chain these aggregation ASICs?
- We can assume that the links are all using the same clock source to simplify sampling.



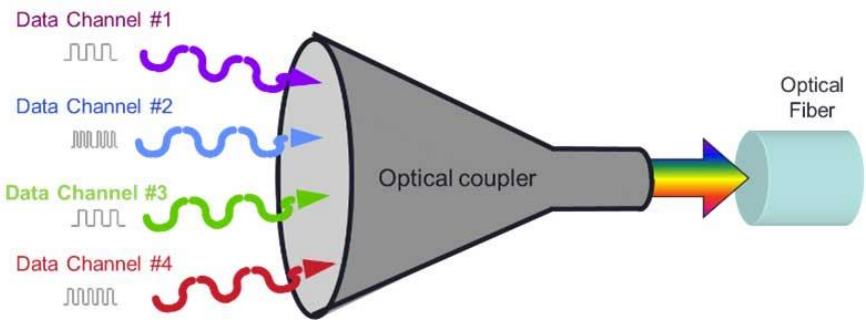
Outlook

- Design of triggerless collider experiments is on the horizon.
- This requires R&D for on-detector electronics
- Intelligent data processing at the source (AI/ML)
- Faster optical links
- Photonics ASICs
- New aggregation ASICs.
- The proposed aggregation infrastructure is different from the lpGBT-VTRX+ approach.
- Unification of the downlinks
- Major focus on fiber-to-chip and reduction in copper interconnects.
- Requires further investment in domestic ASIC expertise (photonics, analog compute, neuromorphic, spiking NNs, etc).

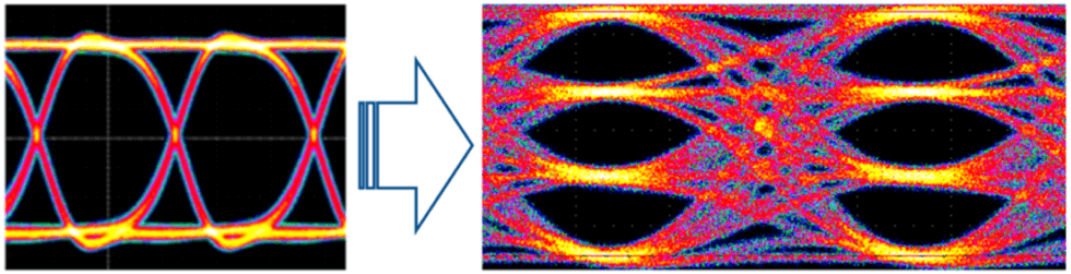
BACKUP

Industry trends

- All the data links for 100m range are fiber-optical. We can not use copper cables because of the high power consumption.
- VCSEL-based 400 Gb/s QSFP transceivers operate at 50 Gb/s per fiber.
- Si-photonics offers 400 Gb/s QSFP modules operate at 100 Gb/s per fiber.
  - Si photonics offers slightly lower power consumption than VCSELs.
- WDM (wavelength division multiplexing) reduces the number of fibers



- PAM (pulse amplitude modulation) instead of NRZ (non-return to zero)



R&D

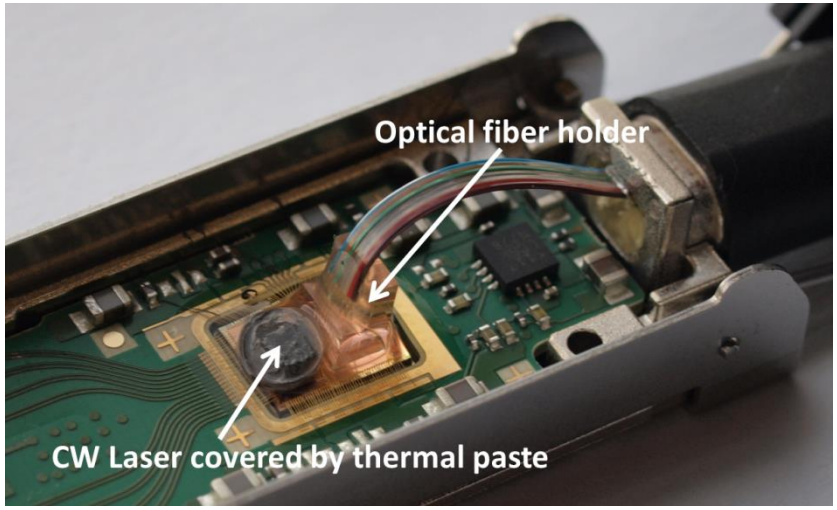
- Alas, industry does not need rad-hard or cryo-capable data links.
- So far we have been using VCSEL-base links (e.g. VL+) and Si-photonic links are in development.
- Wireless data transmission is also interesting. It allows broadcasting for control and configuration of detectors and does not need bulky copper cables.
- The off-detector systems are likely to continue using FPGAs since the on-detector electronics is synchronous to the beam and custom data transmission protocols are used to control the detectors.
- However, the connectivity between the FPGAs and commodity computing will need to go beyond PCIe gen5 (or TCP/IP).
  - There are CPU-FPGA hybrids but it is not clear if we can use them for detector readout. The serial links are not customizable and we also need to supply user-defined clock signals.
- The majority of the design effort is spent on testing and verification of FPGA firmware. Complexity of the future detectors is likely to be higher. Novel design approaches may significantly reduce the effort.

Rad-hard optical links

- R&D for rad-hard VCSEL-based and Si-photonic links is ongoing.
- VCSELs is still the mainstream technology.
- The HEP community can not develop VCSELs for radiation tolerance so we select commercial products most suitable for our needs.
- For VCSELs we develop rad-tolerant drivers and circuits for reading out the photo-diodes.
- Si-photonic transceivers are fully customizable for rad-tolerance. However, we do not have a lot of expertize in the community.
- For the VCSEL-based links the data aggregation is typically done logically (a data frame is assembled of smaller pieces). This is done by an on-detector IC (e.g. GBTx or lpGBTx).
- Si-pho links can also use native optical data aggregation via WDM.

Si-photonics links

- Argonne has characterized radiation tolerance of commercial Si-photonics optical transceivers for the ATLAS experiment at the LHC. Other institutions (e.g. CERN) have also looked at the technology.
  - The optical components were found to be highly radiation tolerant.
- Target: TID~ 3 Mrad, NIEL~ 1e17 n/cm^2.



- The Si-photonics approach allows fabrication high-speed, low-cost, low-power, high-reliability, and low-BER fiber-optical transceivers
- Si-photonics utilizes fabrication of optical circuits in the same wafer as electrical circuits using conventional CMOS processes. →"Fiber to chip" instead of copper cable
- E.G. The technology could significantly reduce the mass, complexity, and power consumption of the FCC-hh inner tracker while also improving its performance.
- <u>The HEP community could benefit from further adopting the technology</u> through partnership with commercial companies or by developing our own devices and expertise. The Si-phonics device libraries are widely available.

Wireless Microwave Technology

- Data rates of several Gb/s.
- 60 GHz band
- 1x1 cm antenna and 2.5x2.5 mm IC.
- Lowe power consumption (<0.3W)
- Error rate at 4 Gb/s over 1m distance is 1e-11.
- The cross-talk is reduced because the signal does not penetrate the tracker sensors.

Free-space optics

- 2.5 Gb/s over 2m at 1e-12 BER.
- mid-IR wavelength