Yet Another Rapid Readout – For ATLAS Inner Tracker during HL-LHC

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RDC5: Trigger and DAQ session
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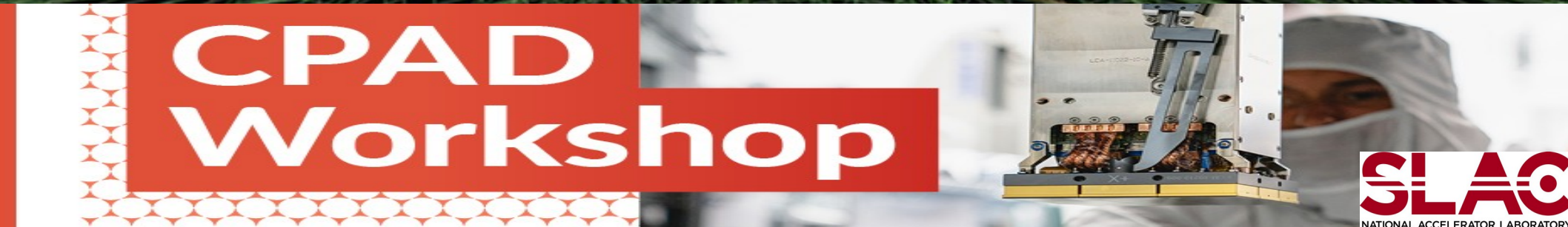
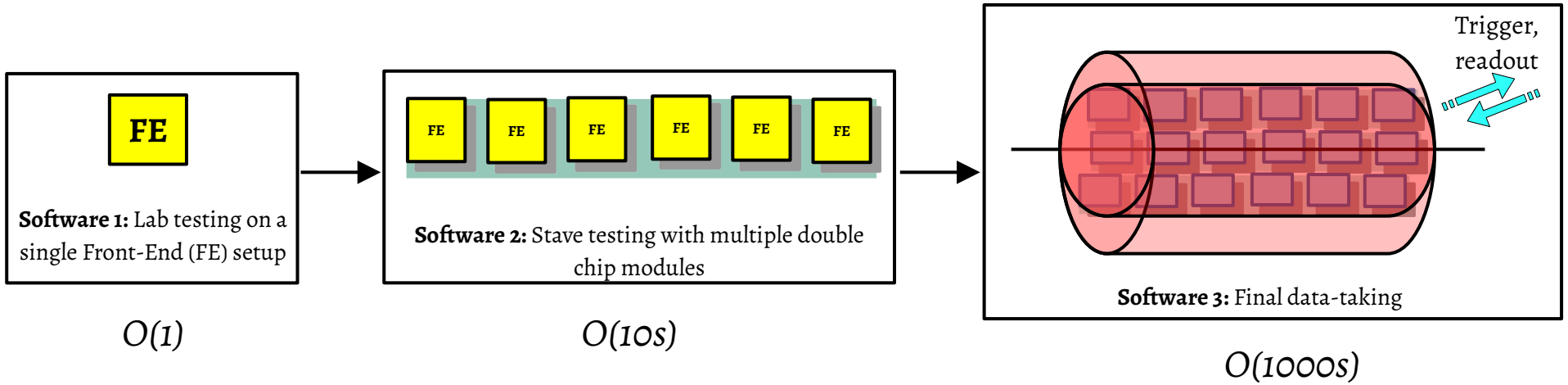


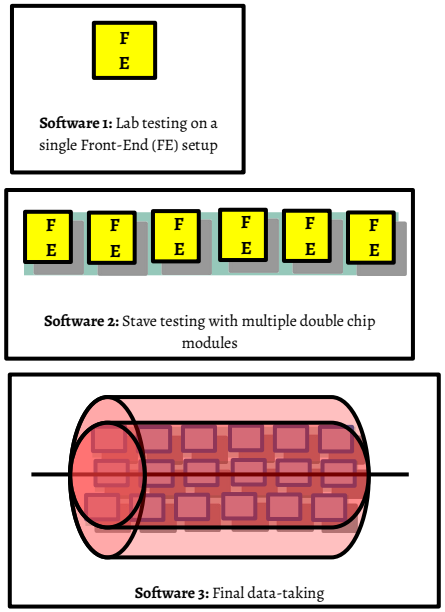
Historical context

- There have been many Trigger and Data AcQuistion (TDAQ) software in the past in ATLAS. These were used in different stages of testing and operation.
- For example, for the new Insertible B-Layer upgrade in 2014, three different software were used for:



The main reason behind three different software was the hardware which scaled up. Not a single software was able to handle all three different stages.

Caveats



- Hardware (HW) setup scaled up at different stages of testing and operations.
- Different software (SW) and firmware (FW) design for each stage.
- SW and FW intertwined with each other for smoother operations.
  Hence, even more difficult to migrate to different hardware setup with the same SW & FW.

- At the same time, harder to maintain different code bases for future usage.

- Often expert knowledge and maturity of software is either lost or not available for future upgrades.
- Had a huge impact on DAQ for operation and how many developers were needed to get it running.

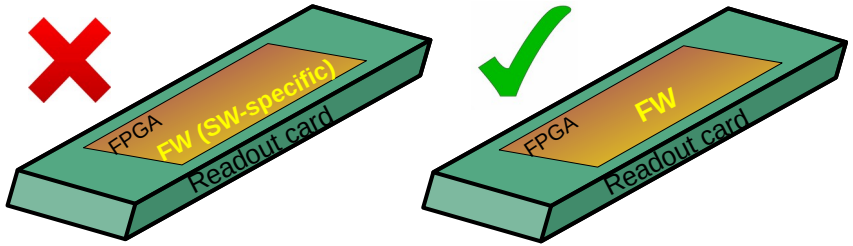
Another DAQ software, why??

Want to maintain a mature software and have experts be able to apply their knowledge over a broad spectrum of test scales.

Best case: should be possible to become expert before going to CERN without having a full system scale setup at home institute.

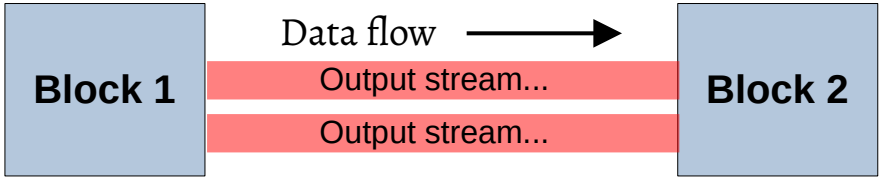
Design philosophy

- **Simple firmware, smart software.**



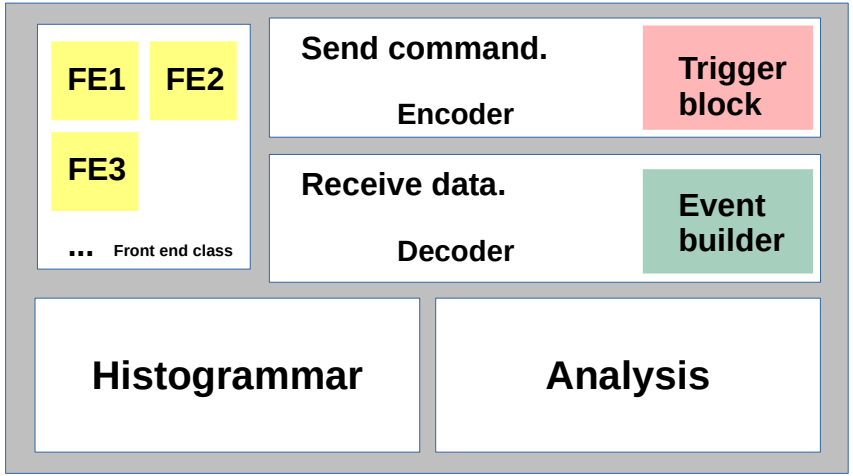
+ SW (Hardware-aware) + SW (Hardware-agnostic)

- Balance of simplicity in software and high performance.



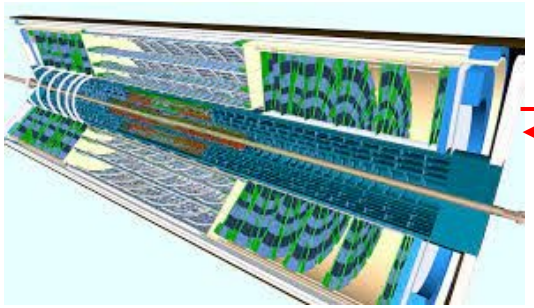
Process independency. Pipeline data in between so that scaling up is easy.

- **Modular software.**



- Good documentation.
- Maintenance and preservation for future.

A new readout software: YARR



ATLAS Inner Tracker (Itk)

Upgraded inner detector for High Luminosity LHC. Two implementations of all silicon-based FE chips – pixels and strips.

YARR = Yet Another Rapid Readout

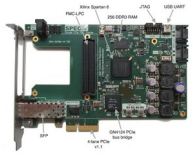
Documentation

A software to interact with the on-detector electronics for:

- Setting up FE configuration.
- Performing calibrations.
- Running online diagnostics.
- Actual operations.
- …

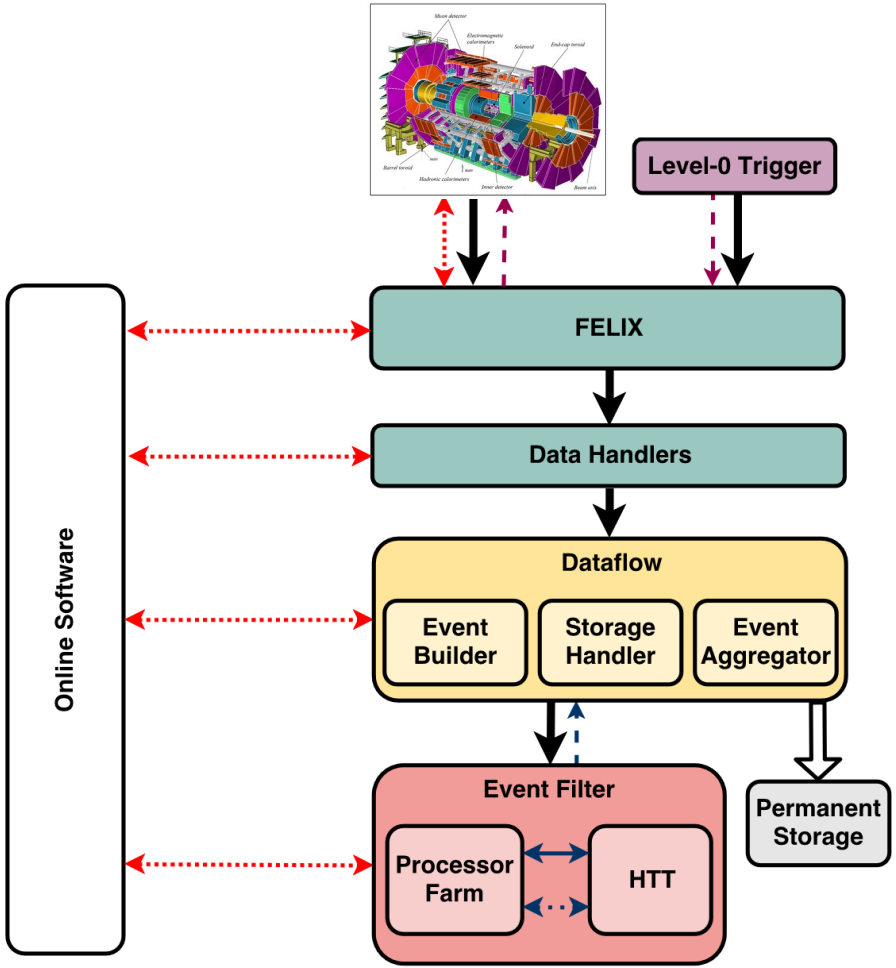
Interfaces with the rest of the ATLAS DAQ system, common to other subdetectors.

For small scale lab testings with YARR, CERN Simple PCIe Carrier (SPEC) board with Xilinx Spartan 6 FPGA (and a few others) is the chosen HW with a custom firmware.



Hence, very generic software with hardware implementation to develop or fix bugs on small-scale lab systems before deploying on the detector, thereby training new experts !

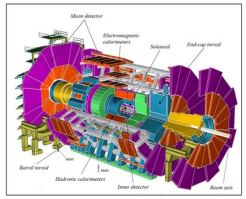
ATLAS TDAQ architecture: HL-LHC



O(800) FELIX cards to be installed on O(400) dedicated FELIX servers.

Source:
ATLAS Phase-II TDR

ATLAS TDAQ with YARR



Level-0 Trigger

Readout

FELIX

Data Handlers

Online Software

Dataflow

Event Builder

Storage Handler

Event Aggregator

ITk

Calo

Muon

YARR

Event Builder

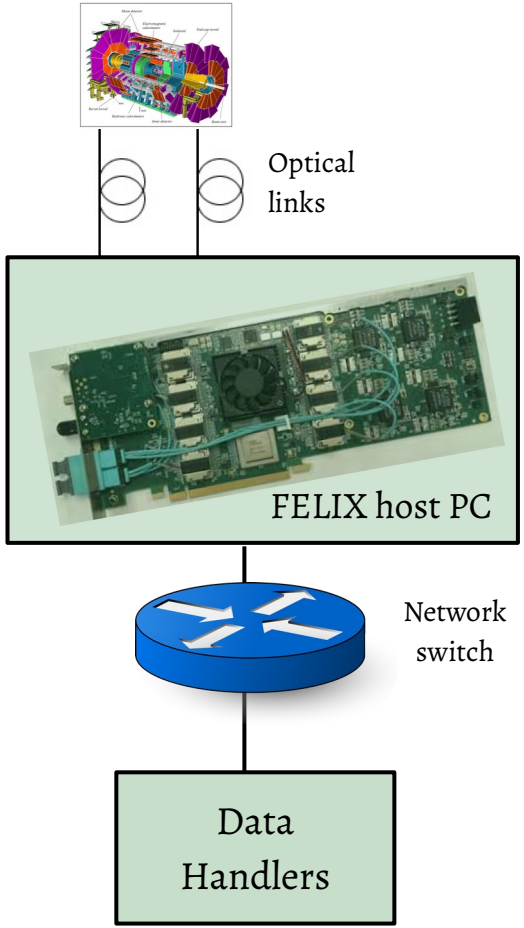
Event Filter

Processor Farm

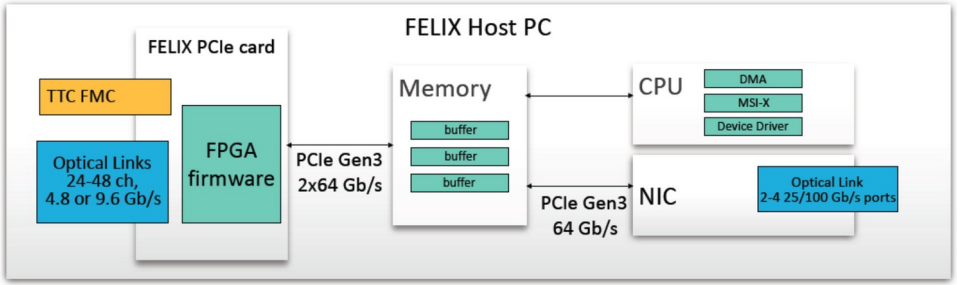
HTT

Permanent Storage

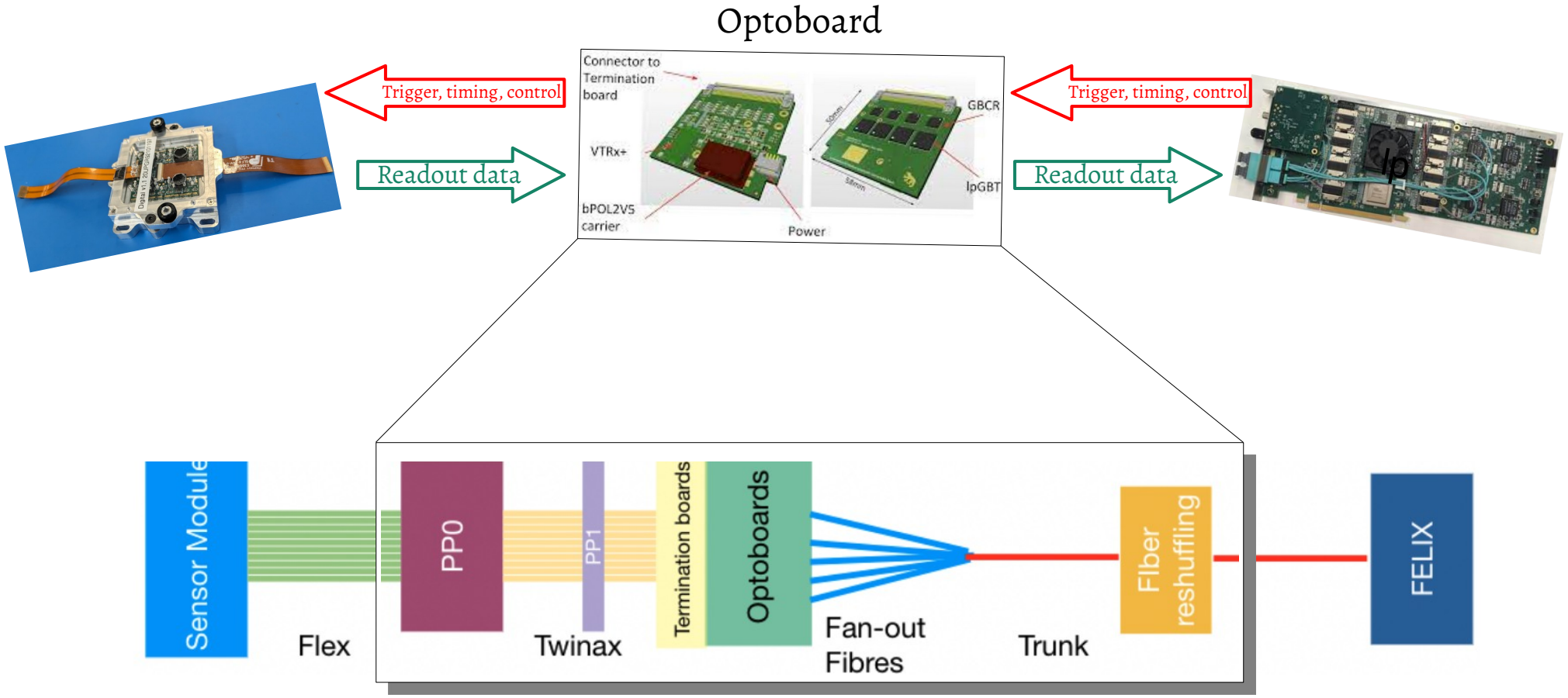
The new hardware platform for HL-LHC



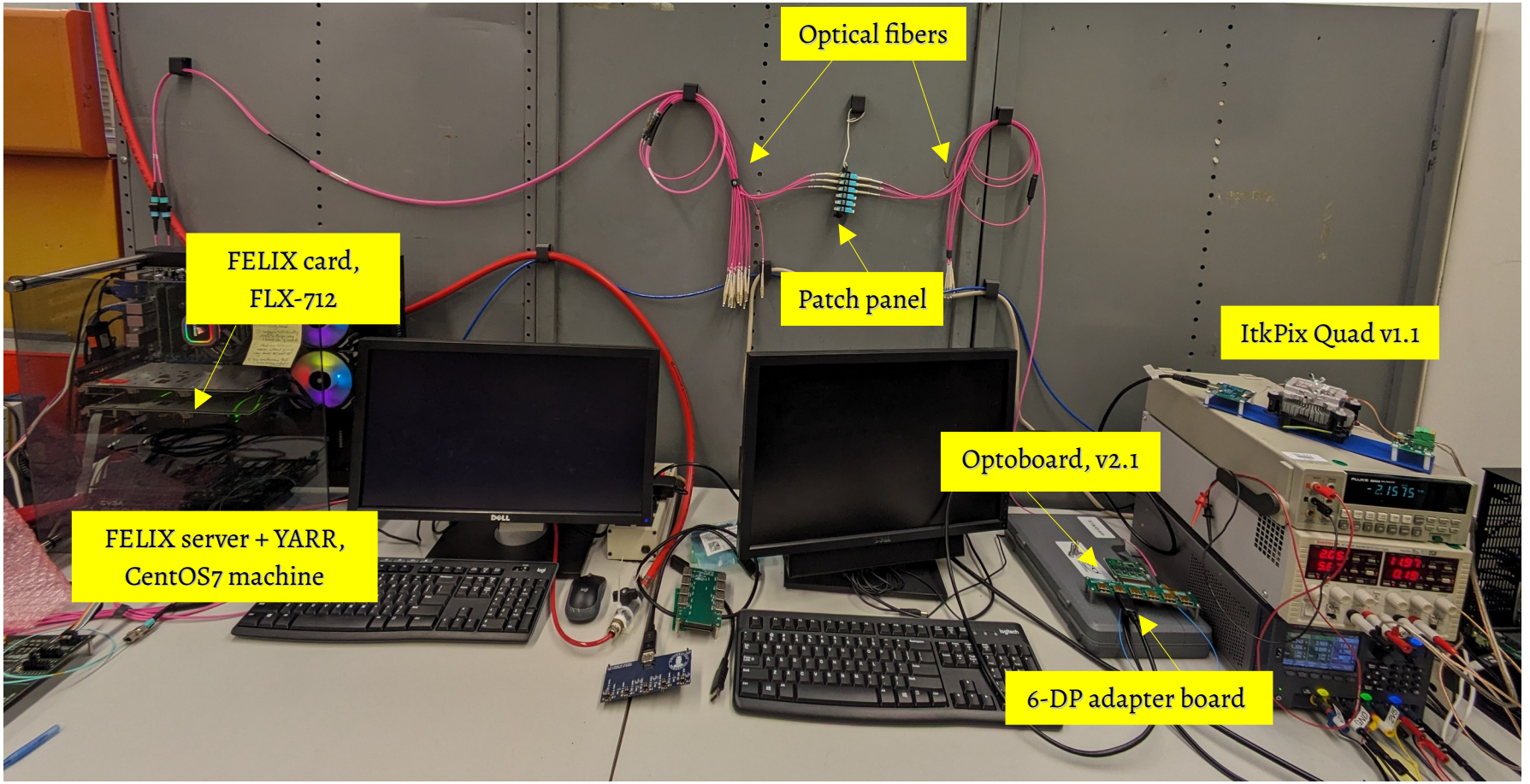
- Front End LInk eXchange (FELIX).
- A router between FE serial links and commercial network.
- Separates data transport from data processing.
- Routes detector control, configuration, calibration, monitoring and detector event data.
- Fed by TTC (Timing, Trigger and Control), a CERN protocol to distribute the 40 MHz LHC clock and L1 trigger information.
- FELIX features configurable E-links in GigaBit Transceiver (GBT) mode, which is a variable-width logical link that can be used to separate different streams on a single physical link.
- FELIX HW & FW* is detector independent (with some detector-specific FW features).



A lab setup: ATLAS ITk with FELIX



Test stand at LBNL



Adapting YARR for FELIX

FELIX server on host PC

- ToHost: data from felix card routed to clients via DMA into PC memory
- FromHost: data from clients copied to felix card via DMA

NetIO

- A software network library, based on libFabric API for backend.
- Low-latency sockets for sending/receiving detector control, configuration and calibration.
- High throughput sending/receiving physics data.
- Publish/subscribe model for clients on the network.

YARR (NetIO client)

To optoboard → FE

Firmware design: Maximum PCIe throughput to the host PC, relying on DMA

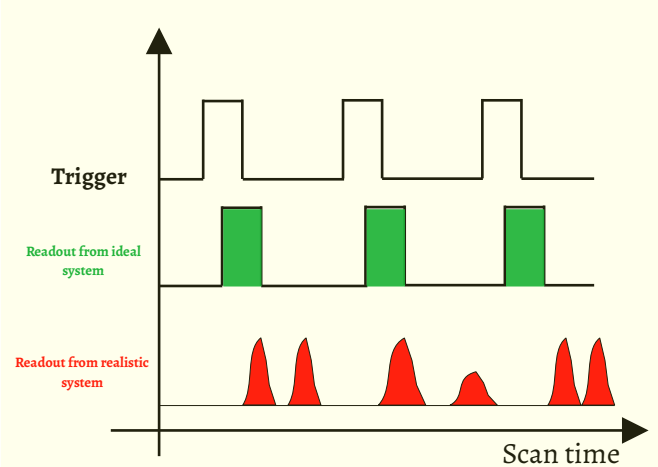
Firmware design: Central router to handle all elinks, data multiplexing/demultiplexing protocol for ATLAS

Firmware design: Fixed latency transmission to FE

Readout from ideal vs real systems

- Data arrival from SPEC-based systems is very deterministic, since it is a direct readout.
- FELIX-based systems has a layer of network before YARR (NetIO), hence the readout can be slow or delayed.
- As a result, the exchange of packets (both commands and data) can suffer from erroneous measurements.
- This is particularly worse during the calibrations where a lot of intricate commands needs to be send for multiple injections, trigger and change of FE configuration.
- At the same time, the arrival of data is expected within a certain time window in between every parameter scans.
- Hence, the timing of data packets has to be synchronized to utmost precision for sensible calibrations.

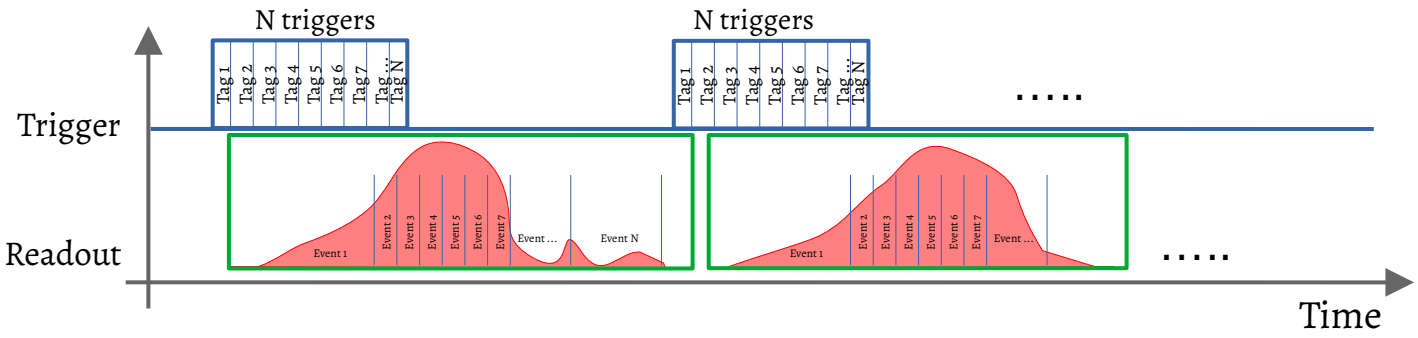
For ideal systems, the wait time is roughly the hardware controller latency. While for realistic systems, wait time is not easily deterministic due to network traffic and/or data buffering.



Loss-less readout for real systems

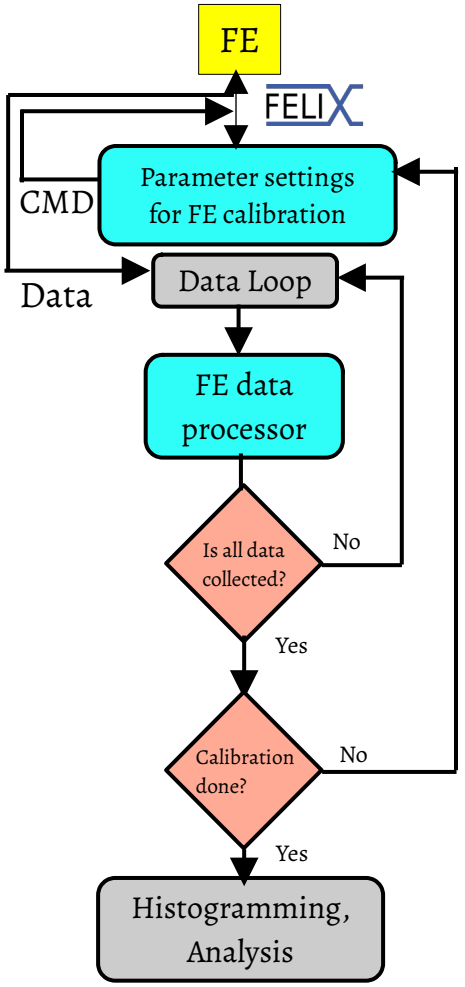
Feedback mechanism (the concept)

Continue reading data until all expected data is received, within a pre-decided time interval.



- YARR collects data from the NetIO socket and passes it on to the data gatherer class.
- Data gatherer orchestrates the data further to various FE-specific classes to decode the streams and create the events.
- With the feedback mechanism, the data gatherer class now will keep listening to more data based on the response received from the FE-specific decoder class.
- The parameter scan for any given settings continues until the data corresponding to all the sent triggers is received back or a maximum timeout is reached.
- This makes the calibrations immune from the uncertainty of data arrival and universal to variability of different setups.

Calibration-specific example

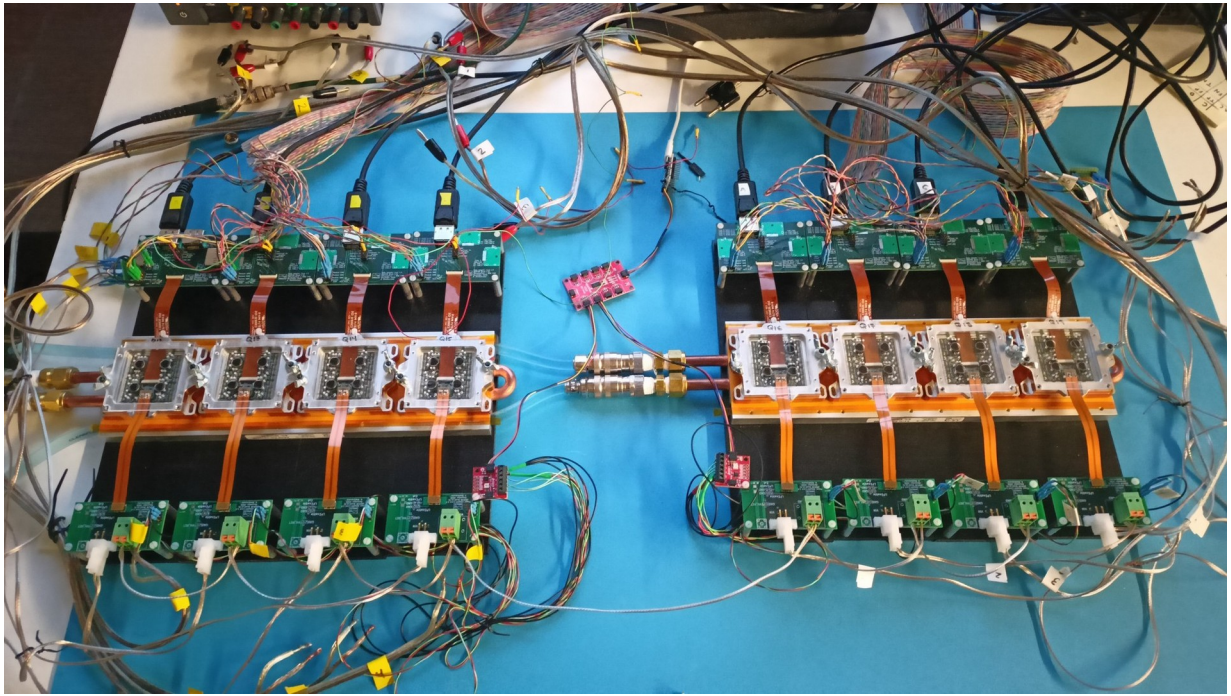


Conclusion

- ATLAS will deploy new all-silicon inner tracker (ITk) to replace current inner detector to meet the extreme conditions during HL-LHC operation.
- ITk Pixel detector fueled by newly designed ITkPix readout chip, by the RD53 Collaboration for both ATLAS and CMS upgrades.
- ITk will need a new DAQ system to deal with the more than 5 billion channels.

- YARR is a potential software solution for operation with FELIX and is already been successfully used for many years during testing and QC with different hardware.
- Currently, YARR is being deployed at many system test cites while still undergoing continuous developments and integration for usage with FELIX.

Future developments



(At LBNL)

- Test on larger scale systems, more realistic to detector scenario. For example, a serial power chain of multiple front-end modules (left).
- Perform readout with YARR using FELIX hardware, with external triggers in test beam studies.
- Readout performance of YARR with FELIX for external triggering with charge injections at the same time – to emulate the high pileup conditions.