CPAD Workshop 2023



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HLS In A DAQ Environment

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The use of High-Level Synthesis Languages (HLS) instead of VHDL or Verilog for FPGA code development is no longer a novelty. HLS allows for greater abstraction, enabling the handling of increasingly complex problems. The rapid prototyping and exploration of various ideas made possible by HLS would be respectively impossible and too time-consuming when using an FPGA hardware language. HLS has proven to be especially useful in the real-time environment of embedded Data Acquisition (DAQ) systems, helping FPGAs become omnipresent, providing highly coveted low-latency, high throughput, and deterministic behavior.

A particularly valuable and potent combination is HLS coupled with C++ meta-programming techniques. This offers two advantages: a) many operations and concepts can be accomplished at compile time, and b) the development of generic frameworks where data types, array sizes, and even algorithmic choices are selected at compile time. This leverages the strengths of FPGAs, where specifying as much as possible at compile-time results in both performance and resource usage advantages, while simultaneously allowing the code to be flexible and adaptive.

Two cases that illustrate these techniques in HLS are presented. Arithmetic Probability Encoding is a data compression method previously used in the protoDUNE project, which will be adapted for nEXO, a neutrinoless double-beta decay experiment. In Mathusla, a proposed experiment for searching for long-lived particles (LLP) emanating from CMS at CERN, HLS is being used to develop a complex trigger. This involves employing 100 FPGAs for local track-finding and then aggregating the found tracks into a central FPGA to locate a possible vertex of the decaying LLP. All of these tasks must adhere to a 2.5-microsecond time budget.

Early Career

No

Primary author: RUSSELL, J.J. (SLAC)
Co-authors: RUCKMAN, Larry (SLAC); HERBST, Ryan (SLAC)
Presenter: RUSSELL, J.J. (SLAC)
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