Skipper CCD-in-CMOS active pixel sensor: status and first characterization results

Speaker: G. Fernandez Moroni
SLAC: L. Rota, A. Gupta, A. Dragone
Centro Atomico Bariloche: F. Alcade, M. S. Haro
Tower Semiconductor: A. Birman, A. Fenigstein
UNS: A. Lapi, F. Chierchie
Skipper CCD

3x3 operation cartoon


~6 Mpixel CCD

Output stages
Thanks Brenda for the slide! (from )

Fast-readout technologies with single-electron resolution

First prototypes are currently being tested showing great results!

G. Fernandez (FNAL)

- standard Skipper CCD
- MAS CCD
- Sisero CCD
- Skipper CMOS
- DESI sensors*

CCDs with n-Sisero stage
[arXiv:2310.13644]

Skipper-in-CMOS
[B. Parpillon @ CPAD 2022]

Multi-Amplifier Sensing (MAS) CCDs, 16-ch Skipper-CCD
[arXiv:2308.09822] *doi.org/10.1002/asna.20230072

See Wednesday's talk by Kenneth Lin and Thursday's talk by Blas Irigoyen for latest results on MAS!
and Thursday's talk by Guillermo Fernandez for latest results on skipper-in-CMOS
Overview

- **Project:** Skipper CCD in CMOS Sensor with Non-Destructive Readout Co-Design
- **Support:** Work supported by the DOE Office of Science under the Microelectronics Co-Design Research Project “Hybrid Cryogenic Detector Architectures for Sensing and Edge Computing enabled by new Fabrication Processes” (LAB 21-2491)
- **Goal:** Design and Fabricate Single-Photon Image Sensor Prototype
- **Innovation:**
  - Sensor with Pinned PhotoDiode (PPD) for conversion
    - Much higher Conversion Gain than CCD (100uV/e- vs 3uV/e-)
    - Low leakage
    - Lower noise per measurement than CCD
  - Skipper CCD for charge manipulation
    - High charge transfer efficiency
    - Enables Non-Destructive Readout (NDR) capability
    - Enables noise averaging feature
  - Co-integrated CMOS process
    - Readout parallelization capabilities
    - Much faster readout time than CCD*
    - Finer feature size
    - High-Volume capability

Top-Level Overview

- MPW with front-side illumination
- Size: 5x5 mm$^2$
- Active area: 3x3 mm$^2$
- Pixel design compatible with Back-Side Illumination
- n-type channel detector
Top-Level Overview

- MPW with front-side illumination
- Size: 5x5 mm²
- Active area: 3x3 mm²
- Pixel design compatible with Back-Side Illumination
- n-type channel detector

Collaboration Landscape:
1. Tower Semi: CMOS and Pixel Technology
2. Centro Atómico Bariloche: Pixel and Matrix testing
3. Fermilab: Front End Readout Design
4. SLAC: Digital blocks and top-level implementation
5. Fermilab, UNS: testing

Physics Applications
1. Low mass dark matter searches
2. Single electron trackers for dark sector searches
3. Soft x-ray spectroscopy
4. Astrophysics: deep measurements of dark energy and dark matter signatures
5. Single-photon quantum sensing
**Architecture Selected:**

1. **Small, Fast, Low noise**
2. Gain tunable with Cin/Cfb capacitance ratio → High gain desirable in low light condition to improve SNR
3. Skipper operation effective up to the track & hold
4. Other noise sources (ie: KTC noise from track & hold, or sources from differential driver) are made insignificant due to the PGA gain

---

**To off-chip test board**
Will perform readout, CDS and skipper operations

---

### Specifications

<table>
<thead>
<tr>
<th>Spec</th>
<th>min</th>
<th>typ</th>
<th>max</th>
<th>unit</th>
<th>condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>IDC</td>
<td>24</td>
<td></td>
<td></td>
<td>mA</td>
<td>Nominal corner</td>
</tr>
<tr>
<td>Power</td>
<td>120</td>
<td></td>
<td></td>
<td>mW</td>
<td>Nominal corner</td>
</tr>
<tr>
<td>Output referred noise</td>
<td>188</td>
<td></td>
<td></td>
<td>uV</td>
<td>Noise tran, 0e-, cds=4pF, gain=1</td>
</tr>
<tr>
<td>ENC</td>
<td>1.6</td>
<td></td>
<td></td>
<td>e−</td>
<td>Noise tran, 0e-, cds=4pF, gain=1</td>
</tr>
<tr>
<td>ENC</td>
<td>&lt;1</td>
<td></td>
<td></td>
<td>e−</td>
<td>Noise tran, 0e-, cds=4pF, gain=35</td>
</tr>
<tr>
<td>linearity: 1-R^2</td>
<td>9.8E-08</td>
<td>NA</td>
<td></td>
<td>NA</td>
<td>gain =1, from 0e- to 11Ke-</td>
</tr>
<tr>
<td>Dynamic Range</td>
<td>1</td>
<td>11000</td>
<td>e−</td>
<td></td>
<td>Gain =1 and 2</td>
</tr>
<tr>
<td>Gain</td>
<td>1</td>
<td>35</td>
<td></td>
<td>V/V</td>
<td></td>
</tr>
</tbody>
</table>
AFE Specification

- Achieve single-electron CMOS Imaging
- High dynamic range
- Microsecond readout time

Pixel

<table>
<thead>
<tr>
<th>Variable</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conversion Gain</td>
<td>115</td>
<td>µV/e⁻</td>
</tr>
<tr>
<td>Dynamic range</td>
<td>11000</td>
<td>e⁻</td>
</tr>
<tr>
<td>White Noise</td>
<td>&lt;10e-9</td>
<td>V/√Hz</td>
</tr>
<tr>
<td>Fnc</td>
<td>&gt;100</td>
<td>MHz</td>
</tr>
<tr>
<td>ENC (single Meas)</td>
<td>&lt;1</td>
<td>e⁻</td>
</tr>
</tbody>
</table>

Analog Readout

<table>
<thead>
<tr>
<th>Variable</th>
<th>Min</th>
<th>Target</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Amplitude</td>
<td>1</td>
<td></td>
<td>11000</td>
<td>e⁻</td>
</tr>
<tr>
<td>Input Amplitude</td>
<td>0.125</td>
<td></td>
<td>1375</td>
<td>mV</td>
</tr>
<tr>
<td>PGA gain (trimmable: 4-bit)</td>
<td>1</td>
<td></td>
<td>64</td>
<td>V/V</td>
</tr>
<tr>
<td>measurement time</td>
<td>1</td>
<td>10</td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>Temperature</td>
<td>-40</td>
<td>27</td>
<td></td>
<td>C</td>
</tr>
<tr>
<td>ENC (single measurement)</td>
<td>&lt;2</td>
<td></td>
<td></td>
<td>e⁻</td>
</tr>
</tbody>
</table>
Testing setup

- Focused in the proof of concept operation of the pixel structure.
- Agustin Lapi, Claudio Chavez in charge of its characterization.
- Test at Different temperatures
- Results presented here at 130K
- Characterization of the pixel structure by individual tests.
Understanding the operation of the output stage

- Output stage characterization
- Decouple the noise from charge production
- Each point has 3000 skipping samples
- The performance should improve in the full matrix using on chip electronics

~170 s
Understanding the operation of the output stage

- Output stage characterization
- Decouple the noise from charge production
- Each point has 3000 skipping samples
- The performance should improve in the full matrix using on chip electronics
Understanding the operation of the output stage

- Output stage characterization
- Demonstration of noise reduction
- Single sample noise $s$
- Measurements from the SF showing much lower noise. Some extra LF noise.
Understanding the operation of the output stage

- Output stage characterization
- Demonstration of noise reduction
- Single sample noise

Measurements from the SF showing much lower noise. Some extra LF noise.

- 2e-equivalent
- Room temp. Test
- Still some LF noise presence
Charge transport from the usage using light

- Important to characterization the charge transfer from the PPD.
- Single poly layer for the gates
- Evaluate the possibility of charge production that is not correlated with exposure time.
Single photon counting

- Sensitivity of the output node ~5 times larger than the Skipper CCD.
- The mean/variance ratio is compatible with the Poisson distribution of the photons arriving to the PPD.

Additional comments

- 9 months one person full time to resolve single photons
- Many Lessons learned: It took us ~8 years to understand how to operate in single photon mode with the Skipper CCD
Instrumentation of the full matrix

- New adaptor board sent for fabrication to instrument the full matrix
- Instrument the full matrix
- The full matrix has 20 different pixel architectures with small modifications in the pixel architecture
- Architecture: 20 variants – 5 Splits: 400 pixel flavors
Skipper-in-CMOS: phase II

Goal of Skipper-in-CMOS phase II:
• Increase frame-rate to 1 kfps

Novel architecture with 3D integration:
• Increase parallelism of the system: x16 pixel cluster connected to an ADC
• Skipper-in-CMOS with back-side illumination (BSI) bonded to readout ASIC (SPROCKET) on CMOS 65nm

Conceptual design of camera based on tiled, full-reticle Skipper-in-CMOS sensors
SPROCKET (Skipper-CCD Parallel Read-Out Circuit) readout ASIC

Readout ASIC for hybrid bonding with image sensor.
In-pixel readout front end includes a preamplifier, correlated double-sampling circuit, and 10b SAR ADC in ~30×30μm (60x60 μm including digital)

• SPROCKET1 (Sep '22): 64 x 32 pixel array with in-pixel ADC
• SPROCKET2 (Dec '22): second version including analog pile-up capability
• SPROCKET3A (May '23): Prototype of digital control + pattern generation
• SPROCKET3 (Nov '23): 320 x 64 pixel array, includes full functionality to be bump-bonded to CMOS image sensor
• SPROCKET3-FR (Summer '24): Full-reticle SPROCKET
SPROCKET3

- **SPROCKET3** is the final SPROCKET prototype before a full-reticle ROIC is developed, including:
  - **20,480 ADC pixels** (bump bond to **327,680 CIS pixels**)
  - In-pixel readout front end including in-pixel analog pileup and at 10b SAR ADC w/ 60 μm pitch.
  - Completely integrated pattern generator + control circuitry to drive both ADCs and Skipper-CCD-in-CMOS logic.
  - **20.48 GHz transmitter** with 10 GHz VCO co-designed with integrated photonic readout in collaboration with the University of Washington.
Conclusions

- The single photon counting capability of the pixel unit has been demonstrated.
- Extra optimization is required to get the best performance of the device.
- Most of this optimization will come from the instrumentation of the full matrix. Different pixels architectures.
- Test of the full matrix will start soon.
- A second version of BSI device is being designed.
- A fast readout ASIC for bump bonding to the sensor is being developed.
What is Skipper CCD?

- Originally developed for CCD readout technique
- Allow to perform Non-Destructive Readout of the charge
- Signal is correlated, noise is not; improve SNR by $\sqrt{N}$
- Integrated noise $< 1$ e- is possible!
  ➔ Allow to do single photon imaging
Final pixel value is $\text{pix} = \text{avg}(\text{signal} - \text{pedestal})$, noise scales as $\sqrt{\#\text{samples}}$

Skipper readout is NOT the same as Correlated Multiple Sampling (CMS)

Thanks to the non-destructive read-out, pedestal and signal are sampled close to each other $\rightarrow$ filter low frequency noise too
Top-Level Overview: why a rolling-shutter architecture

- **Goal of 1st prototype:** demonstrate low-noise readout based on Skipper operation

- Implemented **rolling-shutter** architecture:
  - Control signals are common to all pixels in a row
  - Only one row is active, readout signals are gated in non-active rows (pixel under RST)
  - Avoid redundant charge transfer across PD/gates in non-active rows
  - Reduce digital activity, minimize noise coupling

- Read-out is not fully-parallel: 20 columns are multiplexed to 1 readout channel
  → In non-active columns, redundant charge transfer is still happening
Skipper-in-CMOS: phase II

Goal of Skipper-in-CMOS phase II:
• Increase frame-rate to 1 kfps

Novel architecture with 3D integration:
• Increase parallelism of the system: x16 pixel cluster connected to an ADC
• Skipper-in-CMOS with back-side illumination (BSI) bonded to readout ASIC (SPROCKET) on CMOS 65nm
SPROCKET (Skipper-CCD Parallel Read-Out Circuit) readout ASIC

Readout ASIC for hybrid bonding with image sensor.
In-pixel readout front end includes a preamplifier, correlated double-sampling circuit, and 10b SAR ADC in ~30×30μm (60x60 μm including digital)

- SPROCKET1 (Sep '22): 64 x 32 pixel array with in-pixel ADC
- SPROCKET2 (Dec '22): second version including analog pile-up capability
- SPROCKET3A (May '23): Prototype of digital control + pattern generation
- SPROCKET3 (Nov '23): 320 x 64 pixel array, includes full functionality to be bump-bonded to CMOS image sensor
- SPROCKET3-FR (Summer '24): Full-reticle SPROCKET
SPROCKET3

- **SPROCKET3** is the final SPROCKET prototype before a full-reticle ROIC is developed, including:
- **20,480 ADC pixels** (bump bond to 327,680 CIS pixels)
- In-pixel readout front end including in-pixel analog pileup and at 10b SAR ADC w/ 60 μm pitch.
- Completely integrated pattern generator + control circuitry to drive both ADCs and Skipper-CCD-in-CMOS logic.
- **20.48 GHz transmitter** with 10 GHz VCO co-designed with integrated photonic readout in collaboration with the University of Washington.

SPROCKET3 ROIC integrated with a CMOS Image Sensor (CIS) and Photonic IC (PIC) Readout

SPROCKET3 Layout Capture