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Simulated Performance of the SiD Digital ECal Based on Monolithic Active Pixel Sensors

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The SiD Collaboration has had a long interest in the potential for improved granularity in the tracker and ECal; a study of MAPS in the SiD ECal was described in the 2013 ILC TDR . Work is progressing on the MAPS application in an upgraded SiD design, both for the ECal and tracking. A prototyping design effort is underway for a common SiD tracker/ECal design based on stitched reticles to achieve 5 x 25 cm^2 sensors with 25 x 100 (or 50) $micron^2$ pixels for a linear collider application (C^3 or ILC). Application of large area MAPS in these systems would eliminate delicate and expensive bump-bonding, provide possibilities for better timing, and should be significantly cheaper due to being a more conventional CMOS foundry process. The small pixels significantly improve shower separation. Simulation studies confirm previous results, indicating electromagnetic energy resolution based on digital hit cluster counting provides better performance than the SiD TDR analog design based on 13 mm^2 pixels. Furthermore, the two-particle separation in the ECal is excellent down to the millimeter scale. Geant4 simulation results with optimized analysis based on machine learning will be presented demonstrating optimization of these expectations.

Early Career

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