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Cryo-CMOS at SLAC: Present and Future

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SLAC is pursuing a central role in advancing cryogenic-CMOS development across a spectrum of High-Energy Physics (HEP) experiments. These endeavors encompass diverse domains, including neutrino science through projects like DUNE and nEXO, as well as investigations in quantum computing and Cosmic Frontier research efforts. The latter involves Cosmic Microwave Background surveys, searches for axions or light dark matter, gamma-ray detection in space, and exploration of gravitational wave observatories. Presently, the readout of cryogenic sensors and detectors utilized in these experiments encounters challenges stemming from the segregation of readout electronics, conventionally designed for higher operating temperatures. This necessitates extensive cabling and introduces limitations on analog readout bandwidth, hindering scalability for experiments with large channel counts. Cryogenic ASICs offer a remedy, facilitating cost-effective sensor multiplexing schemes, supplying low-noise amplification along with waveform digitization, and delivering lower noise currents and voltages for sensitive circuits. The appeal of cryogenic ASICs lies in their potential to simplify complexity, reduce costs, and enhance performance margins for ambitious scientific undertakings across the HEP landscape.

This work will showcase a brief overview of SLAC's commitment to advancing specialized cryo-CMOS electronics aimed to support these experiments. We explore their applications in liquid-argon (LAr) and liquid-xenon (LXe) detectors, featuring System-on-Chip (SoC) implementations like CRYO ASIC for nEXO and ongoing endeavors in GAMPix. The latter is a high-granularity charge readout system designed for a LAr-based Gamma-ray detection instrument and holds the potential for application in future DUNE modules 3rd and 4th. Expanding into the realm of High-Energy Physics (HEP) applications, particularly in the extreme cold environments encountered in projects like CMB-S4, we will outline the significant challenges posed by this project. Additionally, we will provide insights into our recent R&D initiative program, dedicated to the development of cutting-edge cryo-CMOS circuit techniques. The program leverages the state-of-the-art 22nm FDSOI ultra-low-power, rad-hard technology, capable of reliable operation down to 4K as the primary technology node. Furthermore, this R&D initiative will serve as the foundation and risk mitigation strategy for the future development of SoC ASICs tailored explicitly for cryogenic experiments and will also yield valuable advantages for forthcoming liquid noble gas experiments.

Early Career

No

Primary author: PENA PEREZ, Aldo (SLAC)

Co-authors: HALLER, Gunther; YANG, Liang; ROTA, Lorenzo; CONVERY, Mark; BREUR, Sander; HENDERSON, Shawn; SHUTT, Tom; AHMED, Zeeshan

Presenter: PENA PEREZ, Aldo (SLAC)

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