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An input buffer for PSEC5 –a waveform sampling ASIC –in 65nm CMOS Technology with a 5GHz analog bandwidth

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PSEC4 [1] has been utilized for waveform sampling in the PhD theses of E. Angelico[2] and E. Oberla[3] ,the Fermilab Test Beam, and the Accelerator Neutrino Neutron Interaction Experiment. PSEC5 aims to improve on its predecessor by raising the number of channels from 6 to 16, the sampling rate from 10 GSa/s to 40 GSa/s, and most importantly, achieving a timing resolution of 1 picosecond.

A buffer of high input and impedance and low output impedance is required to prevent any loading and disruption to the signal source, while driving the waveform to subsequent stages with minimal loss in signal quality.

We present an input buffer of said ASIC in the TSMC 65nm process, which provides an analog bandwidth of 5GHz, unitary gain, a significant DC offset to prevent a cutoff at 0V, and no AC phase difference using 2.5V nMOSFETs. The described input buffer is situated at the front end of the ASIC, feeding into three followers of a similar design. We will also discuss the larger scheme of the front end signal transmission.

We have simulated the buffer with a capacitive load of itself under a three times multiplier in order to account for the capacitance of the followers succeeding the input buffer using Cadence® Virtuoso® System Design Platform.

References
[1] Eric Oberla PSEC4 waveform sampler and Large-Area Picosecond PhotoDetectors readout electronics; Workshop on Picosecond Photon Sensors, Clermont-Ferrand
[2] Evan Angelico; Development of Large-area MCP-PMT Photo-Detectors for a precision
time-of-flight system at the Fermilab Test Beam Facility; Doctoral Dissertation, Department of Physics, University of Chicago
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[3] Eric Oberla; Charged Particle Tracking in an Optical Time Projection Chamber; Doctoral Dissertation, Department of Physics, University of Chicago

Early Career

Yes

Primary authors: YEUNG, Richmond (University of Chicago); FRISCH, Henry (Enrico Fermi Institute, University of Chicago); PARK, Jinseo (University of Chicago); OBERLA, Eric (University of Chicago); ANGELICO, Evan (Stanford University); RICO-ANILES, Hector (North Central College); PASTIKA, Nathaniel (FNAL); RUBINOV, Paul (Fermilab); ENGLAND, Troy (Fermi National Accelerator Laboratory)

Presenter: YEUNG, Richmond (University of Chicago)

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