Contribution ID: **137** Type: **Oral**

Readout IC R&D for future Phase III High Luminosity Upgrade of the LHC

Tuesday, 7 November 2023 15:00 (15 minutes)

We introduce an Application Specific Integrated Circuit (ASIC) readout integrated circuit (ROIC) prototype designed using the CMOS 28 nm bulk process. This chip serves as a smart pixel concept test chip for the Phase III high luminosity upgrade of the large Hadron collider.
Our design demonstrates a synchronous 40MSPS analog-to-digital converter (ADC) at the frontend, enabling data conversion within a single bunch crossing.
The prototype contains a 32x16 pixel matrix. Each pixel measuring 25×25 μm² and fully integrated with a charge-sensitive preamplifier with leakage current compensation and three auto-zero comparators for a 2-bit flash-type ADC. The power consumption is approximately 4 μW per pixel for an equivalent noise charge of 90 electrons at the output of all the hit comparators across the ROIC allowing an in-time threshold of approximatively 450 electrons.

Early Career

No

Primary author: PARPILLON, Benjamin

Co-authors: Dr TRIVEDI, Amit (UIC); FAHIM, Farah (Fermilab)

Presenter: PARPILLON, Benjamin

Session Classification: RDC4

Track Classification: RDC Parallel Sessions: RDC4: Readout and ASICs