Readout IC for future Phase III high luminosity upgrade of the large Hadron collider

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We introduce an Application Specific Integrated Circuit (ASIC) readout integrated circuit (ROIC) prototype designed using the CMOS 28 nm bulk process. This chip serves as a smart pixel concept test chip for the Phase III high luminosity upgrade of the large Hadron collider.

Our design demonstrates a synchronous 40MSPS analog-to-digital converter (ADC) at the frontend, enabling data conversion within a single bunch crossing.

The prototype contains a 32x16 pixel matrix. Each pixel measuring 25×25 µm² and fully integrated with a charge-sensitive preamplifier with leakage current compensation and three auto-zero comparators for a 2-bit flash-type ADC. The power consumption is approximately 4 µW per pixel for an equivalent noise charge of 90 electrons at the output of all the hit comparators across the ROIC allowing an in-time threshold of approximatively 450 electrons.

Early Career

No

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