Readout IC R&D for future Phase III High Luminosity Upgrade of the LHC

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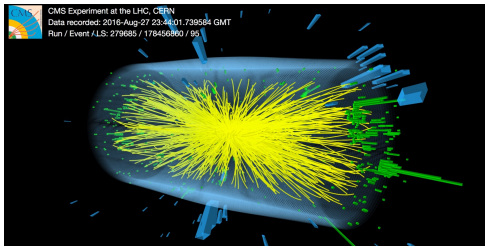
Background

Phase II upgrade HL-LHC CMS

- 5 times improved luminosity (radiation)
- 7 times higher interaction rate (~3Ghit/cm2)
- Raw data generation of 40ZB/yr



Pixel detector R&D effort for replacement for Phase III

Technology	65nm CMOS	28 nm CMOS
Pixel size	**50x50 µm²**	**25x25 µm²**
Pixels	394x400 = 157.6k	788x800 = 0.63M
Detection threshold	**~1000e-**	**~500e-**
Hit rate	**< 3GHz/cm²**	**< 3GHz/cm²**
Trigger rate	**1MHz**	**40MHz (?)**
Digital buffer	**12.5 µs**	**(?)**
Readout data rate	1-4 links @ 1.28Gbps	Photonic link @ 30-100 Gbps
Radiation tolerance	**500Mrad at -15°C**	**1Grad at -15°C**
Power	**1 W /cm²**	**1 W /cm²**

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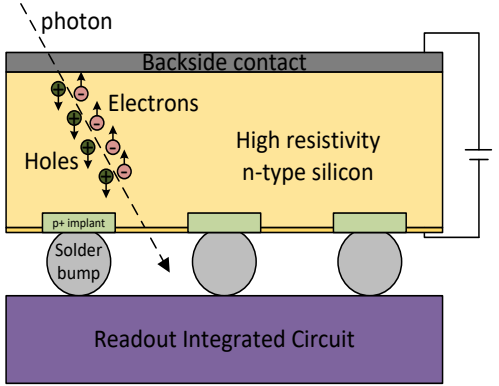
Prototype ROIC for our R&D proof of concept

ROIC Implementation end goal:

- → Low power, low noise preamplifier with a leakage compensation technique (for radiation)
- → A low power 40MSPS synchronous comparator architecture with auto-zero capability to create an in-pixel ADC
- → On chip data reduction capability using AI/ML techniques



First Prototype implementation:

- Analog frontend without ML/AI backend
- The pixel prototype is designed in HPC+ 28nm
- It contains an array of 16x32 pixels
- Pixel size are 25µm x 25µm each
- The ASIC is 1.5mm^2

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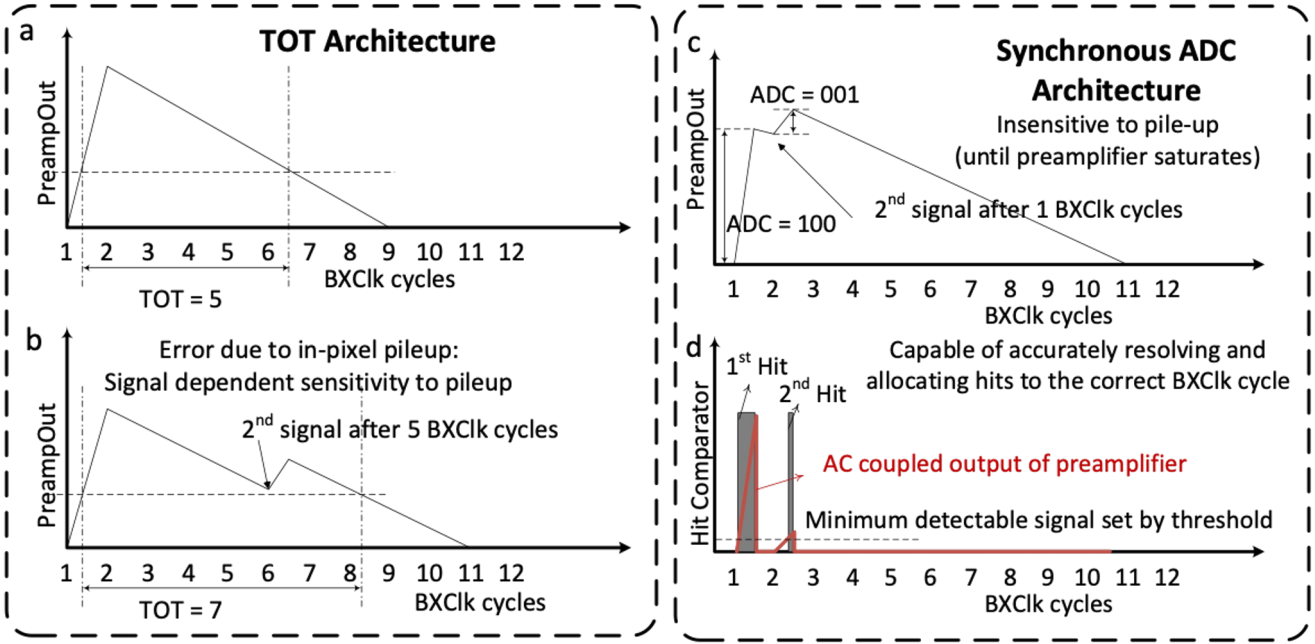
TOT vs. Synchronous



- Insensitive to pile up
- Capable of accurately resolving hits in subsequent bunch crossing
- Synchronous approach ensure simple ML algorithm
- Enables low power combinatorial approach for digital implementation

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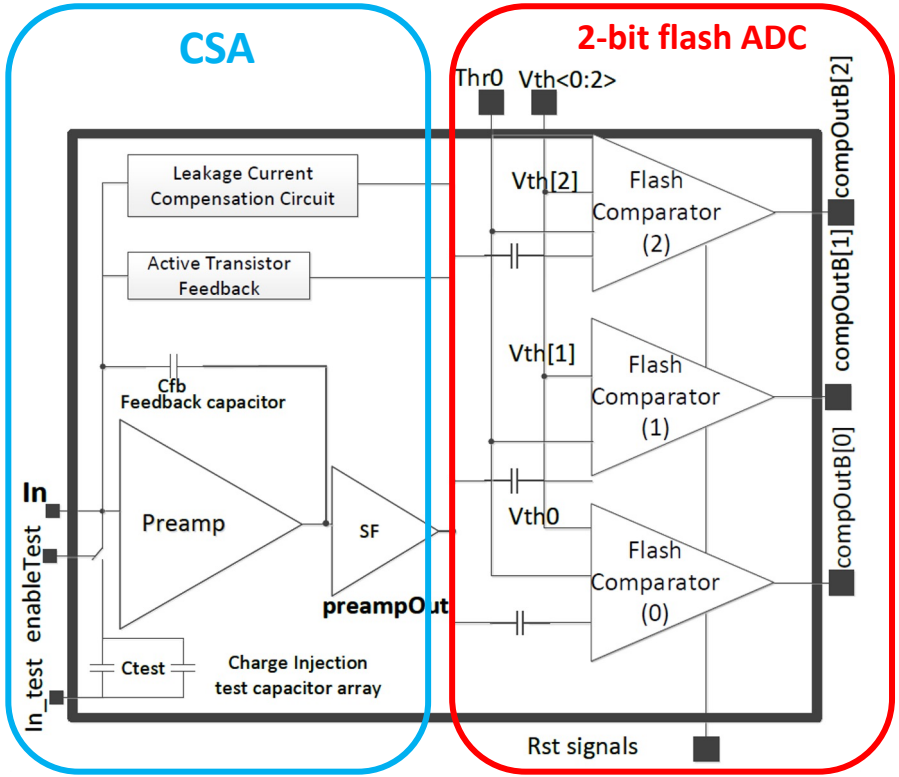
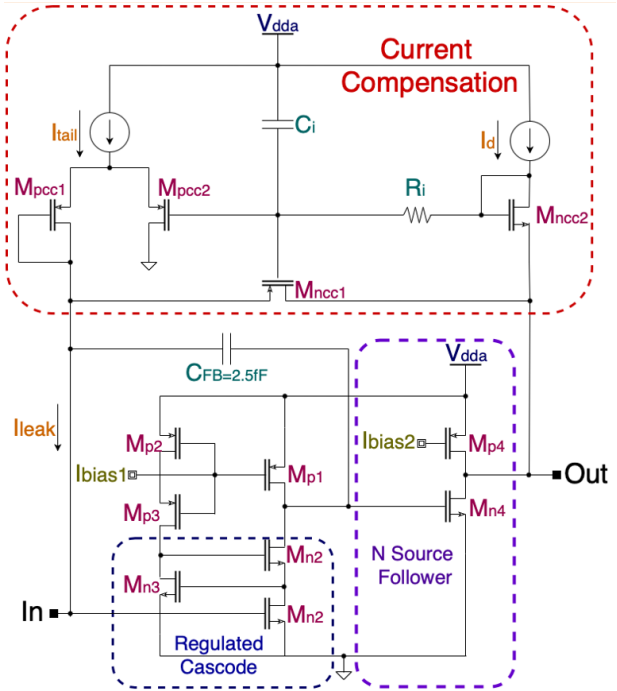
Front-end pixel architecture



- 25μm × 25μm pixel sizes
- Power about ~6.25uW [majority of it used at the front-end]
- AC coupled 40MSPS in-pixel 2-bit flash ADC
  -> insensitive to pile-up
- 2-bit ADC:
  → version 1: Single ended
  → version 2: Differential
- Charge injection cap array (2 or more) for injecting different signals across the pixel matrix for testing Neural network performance
- Auto zero in every pixel for threshold correction
- Also exploring Non-AZ options

Charge Sensitive Amplifier (1)



- Dynamic range 64aC – 2.5fC

400e- to 13Ke-

- Regulated Cascode core amplifier design
- Active transistor feedback resistor (Mncc1)

→ Large signals behaves as a constant current source

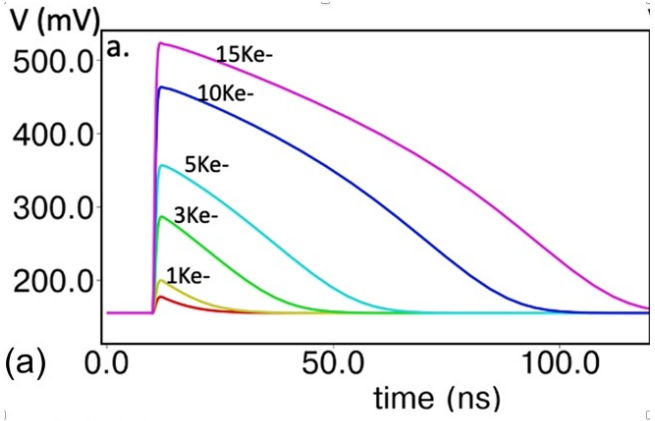
→ Small signals R_F = 1/gm

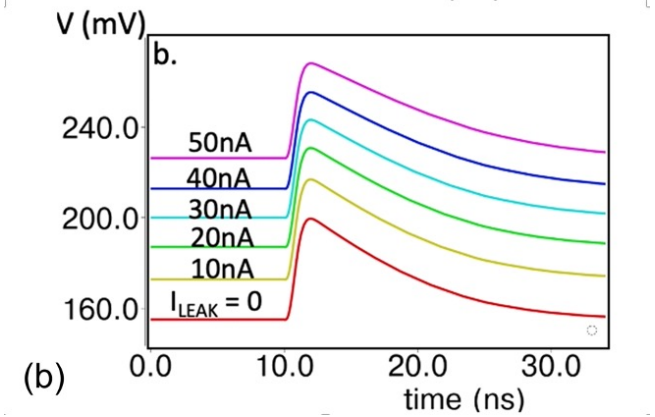
- Leakage current compensation structure

inspired by IFCP65

→ compensation up to 50nA

Uses a differential amplifier Mpcc1 and Mpcc2 with a tail current greater than the sum of detector leakage current and the bias current of Mncc2 (Id)





L. Gaioni, D. Braga, D. C. Christian, G. Deptuch, F. Fahim, B. Nodari, L. Ratti, V. Re, and T. Zimmerman,
"**A 65 nm cmos analog processor with zero dead time for future pixel detectors,**"
Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, vol. 845, pp. 595–598, 2017.

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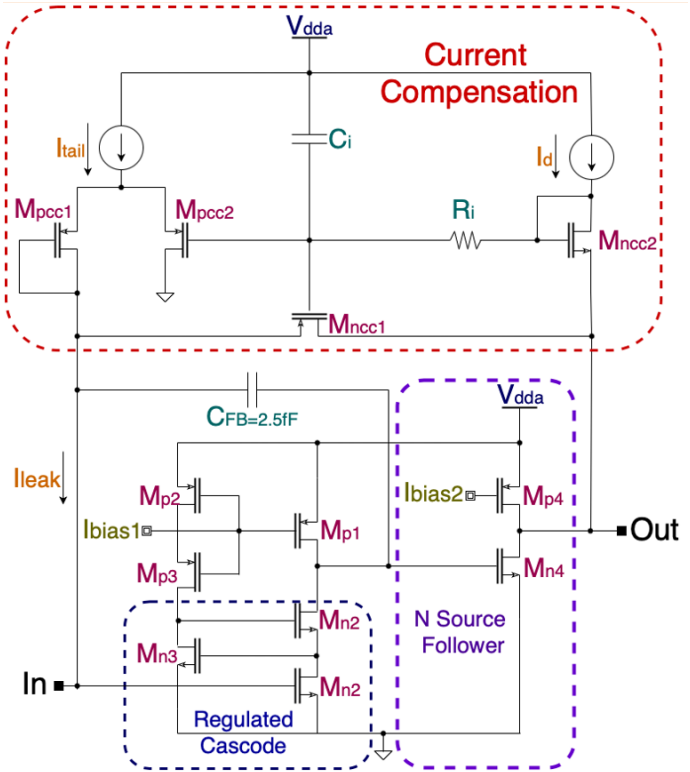
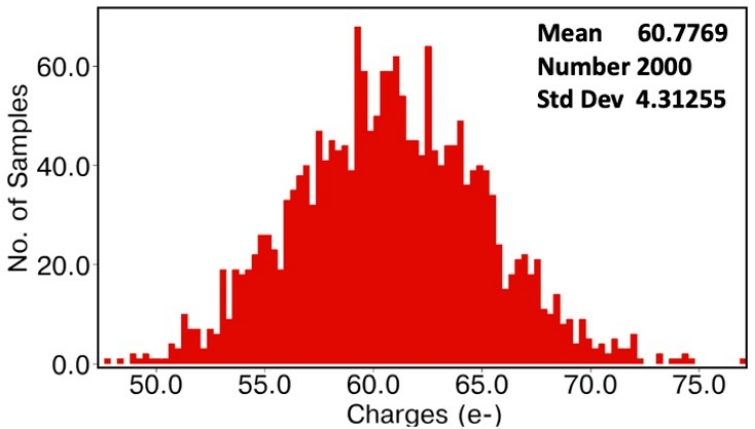
Charge Sensitive Amplifier (2)



Parameters	value	unit
Power	3	μW
ENC	61	e-
Charge sensitivity	40.85	μV/e-
Phase Margin	65	degree
Dynamic Range	13	ke-
Q_{BF}	12	e-



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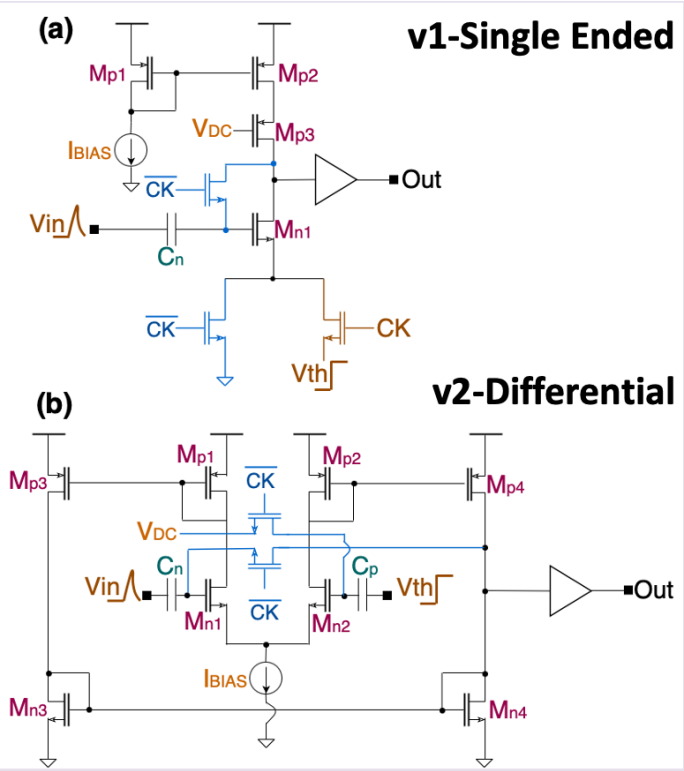
ADC Comparator (1)



Two architectures implemented for comparison:

Reset Phase:

Blue path activates during the first 12.5ns of the period. The circuit is configured as a voltage follower to sample and store DC operating point, offset and noise.

Comparison Phase:

Brown path activates during the second half of the period. The circuit is configured as a high voltage gain structure, the threshold and signal are injected and compared.

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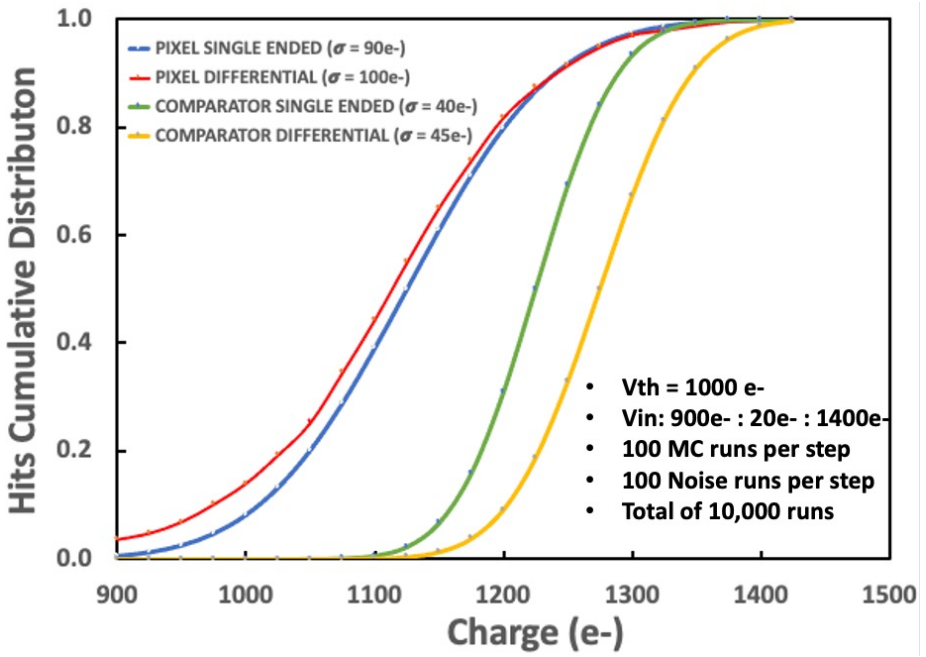
Comparator (2)

Result	v1	v2	unit
Power	**0.5**	1	μW
Threshold Dispersion	**40**	45	e-
Area	**17.5**	30	μm^2
Auto-zero	yes	yes	
Dead time	250	**0**	ps



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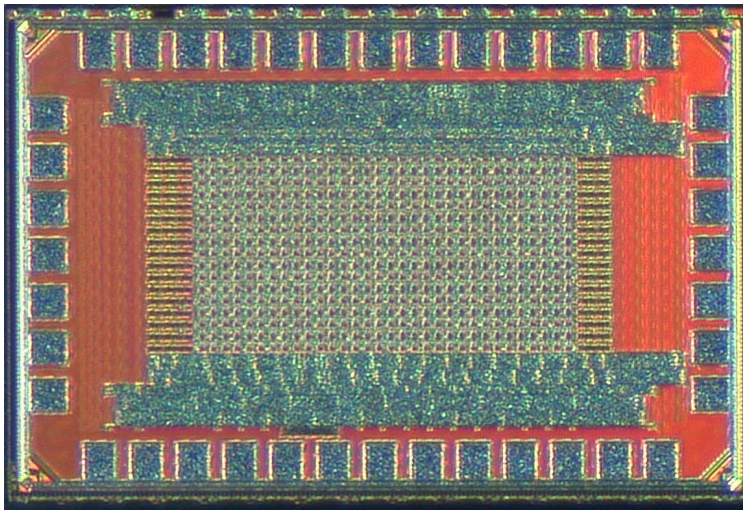
Pixel Performance



Result	v1	v2	unit	comments
Power	3.7	5.2	μW	Per pixel
Total Equivalent Charge Dispersion	90	100	e-	Includes: • ENC • Qth • Baseline fluctuation • kickback
Min Threshold	430	475	e-	4.75 σ
Analog Area	169	211	μm^2	

- 4x improved granularity
- 2.5x power reduction
- 2.5x improvement in threshold detection
- Insensitive to pile-up

Includes:

Equivalent Noise Charge: **ENC**

Static Offset: $\mathbf{Q_{TH}}$

Dynamic Offset Fluctuation: $\mathbf{Q_{BF}}$

$$\sqrt{ENC^2 + Q_{TH}^2 + Q_{BF}^2}$$

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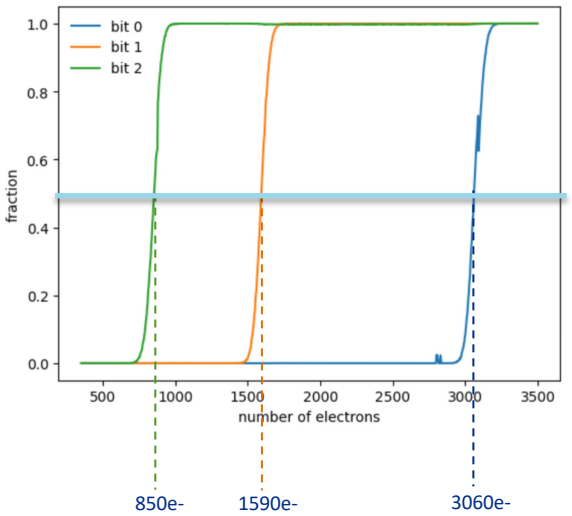
Early measurement results



S-curve extracted for 3-bit on single pixel

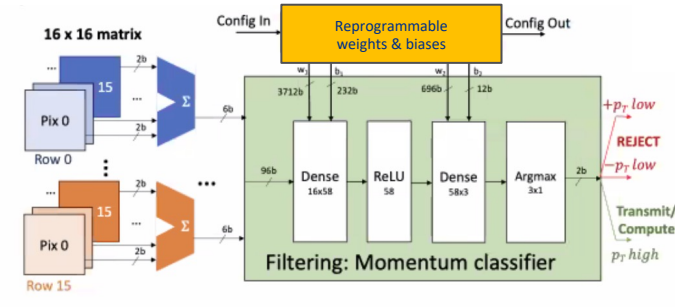
- *single ended version*
- *200 measurement by steps of 2e-*
- *No sensor capacitance connected to the ROIC*
- *Sampling threshold at 850e-, 1590e- and 3060e-*

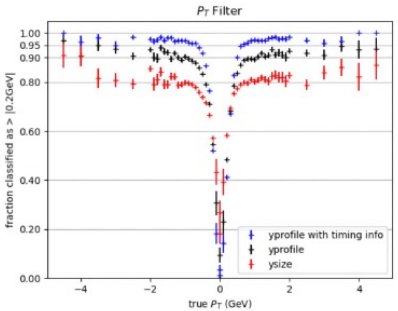
	Single ended	Diff
Charge sensitivity	50uV/e-	50uV/e-
Standard deviation	25-30e-	NA
Threshold dispersion	NA	NA

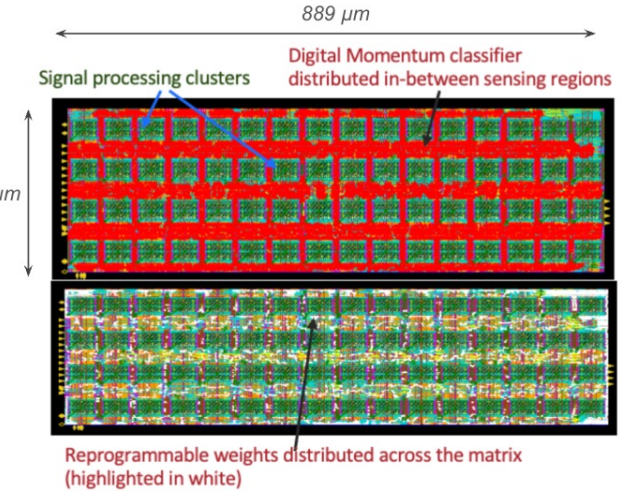
S-curve extraction for differential structure ongoing
Threshold dispersion characterization ongoing

Ongoing Effort : Smart Pixel ROIC Implementation

- We are taping out two 8x32 smart pixel matrices **soon**
- Analog frontend pixels tightly connected to a fully combinatorial digital classifier
  - → Only draws power when a charge cluster is created
  - → 300uW of power for 256 pixels
  - → ~1uW/pixel to ensure our goal of 1W/cm2
- Classifier allows to reject 75% of the clusters
  - → Reducing power required for data transfer







Co-design of digital classifier:

→ Jieun Yoo talk (11/8/23 2.35PM)

[Front-end neural network filtering implemented in a silicon pixel detector]

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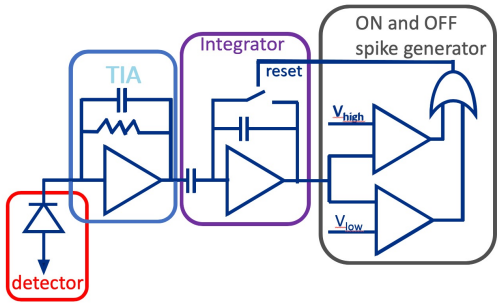
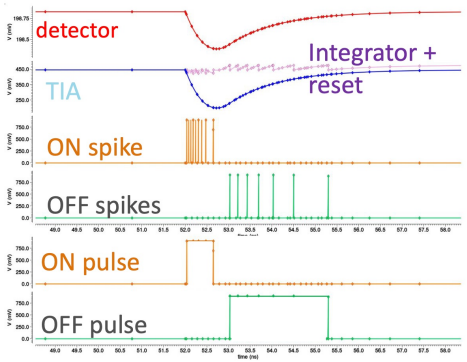
(1) Future Effort : ASIC Development Roadmap for Smart Pixel

Neuromorphic Front-End Solution

- Event-driven front-end (ongoing)
- Algorithm development of digital SNN for a cluster of pixels (completed by ORNL)
- Implementation of the SNN into digital hardware (Fermilab)
- Implementation of the SNN into analog hardware (Sandia)



- Pulse shape encoded in spike train
- Ultra-fast signal processing ~ 100ps
- Digital processing – power constraints
- Analog processing – device constraints (speed)



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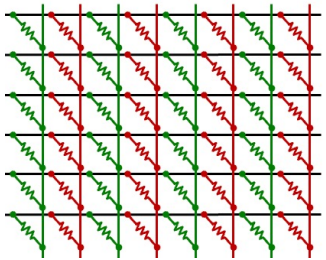
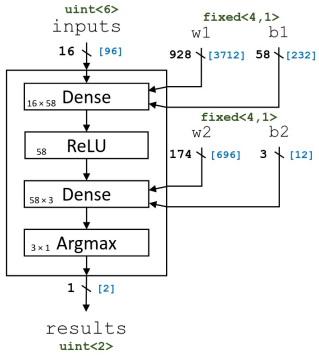
(2) Future Effort : ASIC Development Roadmap for Smart Pixel

Analog AI implementation

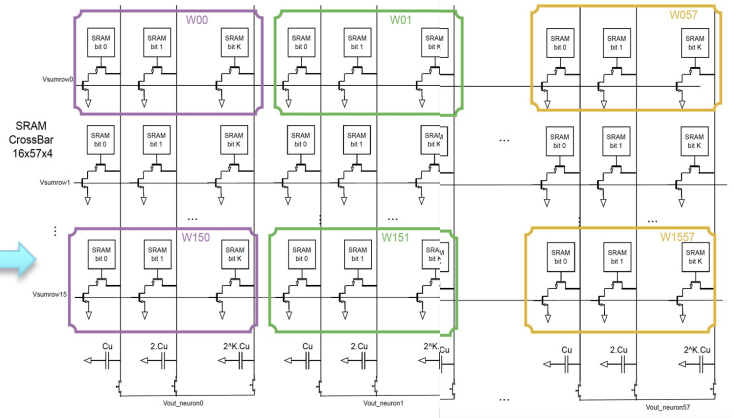
- Implement analog classifier counterpart for a cluster of pixels
- Characterize power/area efficiency gain
- Develop ROIC prototypes:
  - SRAM based solution
  - Floating Gate based solution
  - Beyond CMOS ReRAM based solution



Analog NN model with ReRAM



NN model



Analog NN model with SRAM

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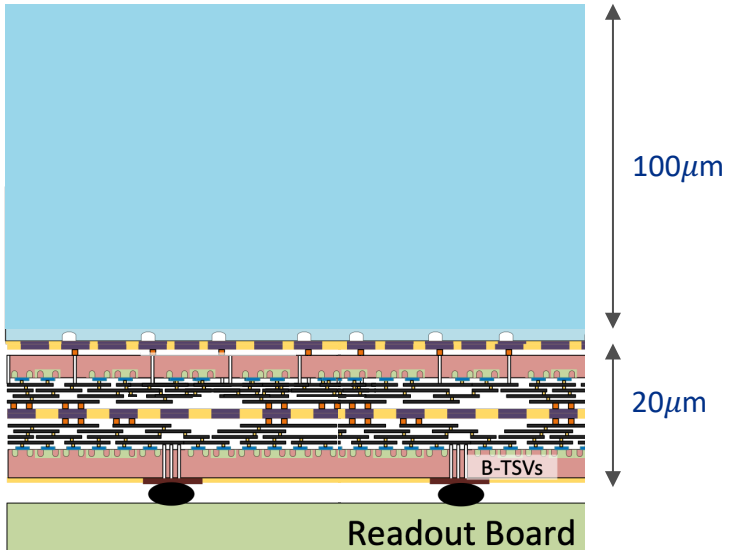
(3) Future Effort : ASIC Development Roadmap for Smart Pixel

Investigate 3D integration –

pixelated layer for data filtering; 2nd layer for featurization

- Highly parallel processing enabled by vertical integration
- Low power data transfer
- Reduced clock speed

Enabling real time determination of physics information (x,y,θ,ϕ and uncertainty)



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