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Design Updates for HPSoC: A very high Channel Density Waveform Digitizer with sub-10ps resolution

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We present the architectural design, prototype fabrication and first results for the High Pitch digitizer System-on-Chip (HPSoC). The HPSoC is a high channel density and scalable waveform digitization ASIC with an embedded interface to advanced high-speed sensor arrays such as e.g. AC-LGADs. The chip is being fabricated in 65nm technology and targets the following features: picosecond-level timing resolution; 10 Gs/s waveform digitization rate to allow pulse shape discrimination; moderate data buffering (256 samples/chnl); autonomous chip triggering, readout control, calibration and storage virtualization; on-chip feature extraction and multi-channel data fusion.

Early Career

Yes

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