Design Updates for HP-SoC: A very high Channel Density Waveform Digitizer with sub-10 ps resolution

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CPAD Workshop

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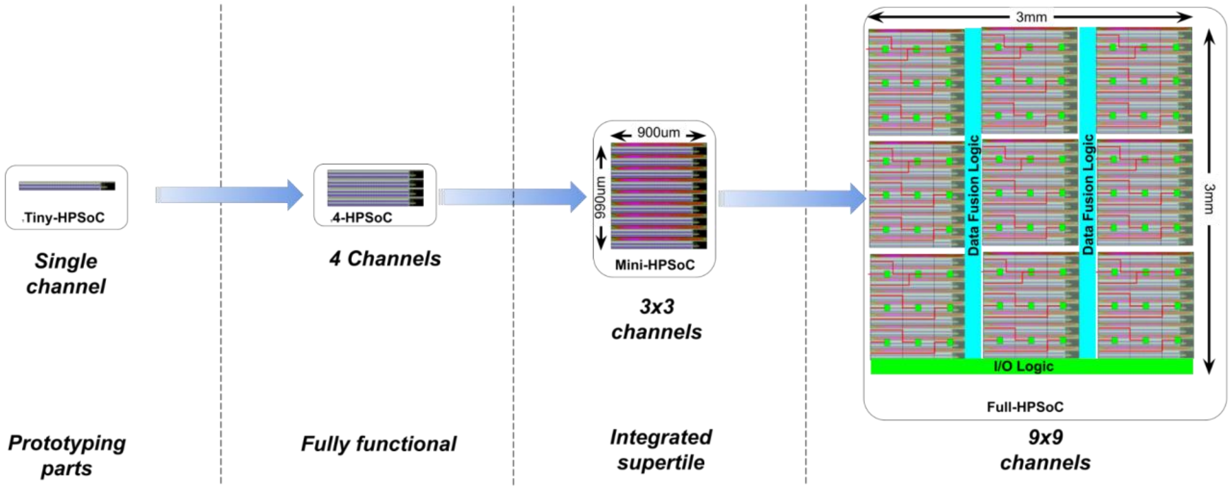
Motivation

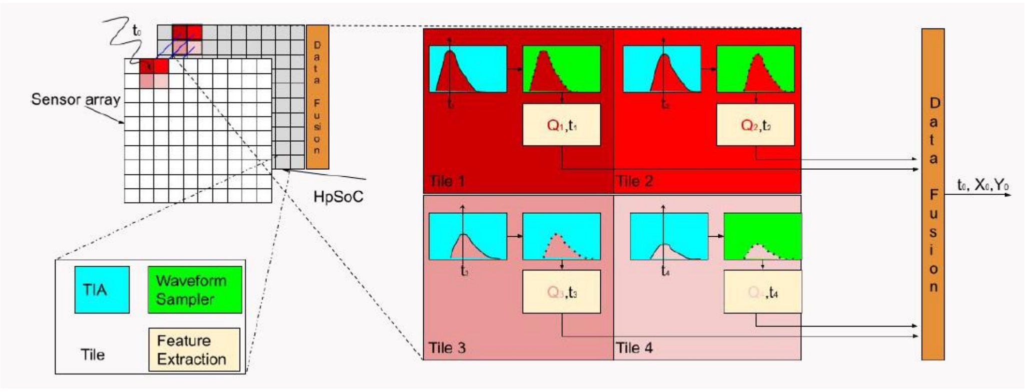
- Precision timing – and 4D tracking – is increasingly important for high-energy and nuclear physics experiments
- Large-scale detector applications require large numbers of segments: depending on the experiment and detector layout, the density of readout channels is high
- Design of fast readout electronics with an acceptable power consumption and cost level is an ongoing challenge
- Time-to-Digital Converter (TDC) and time-over-threshold solutions provide only an indirect estimate of integrated charge and are adversely impacted by effects such as time walk, baseline wander, which need to be corrected

➢ **Implementation of on-chip waveform digitization at the GSample level could address these concerns**

HP-SoC: specifications and targets

- 65 nm TSMC CMOS
- Input preamplification handling fast current-based sensors (~100 ps rise times)
- Very large integration (100+ channels) with modular tileable, scalable structure
- Timing resolution (jitter) better than 10 ps, down to 5ps
- Waveform digitization of at least 10 Gs/s, allowing for pulse shape discrimination
- Autonomous chip triggering and storage virtualization
- On-chip feature extraction and multi-channel data fusion

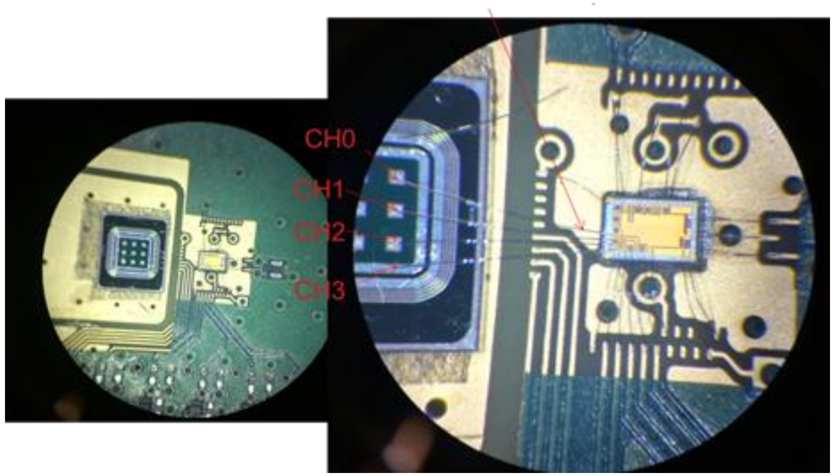


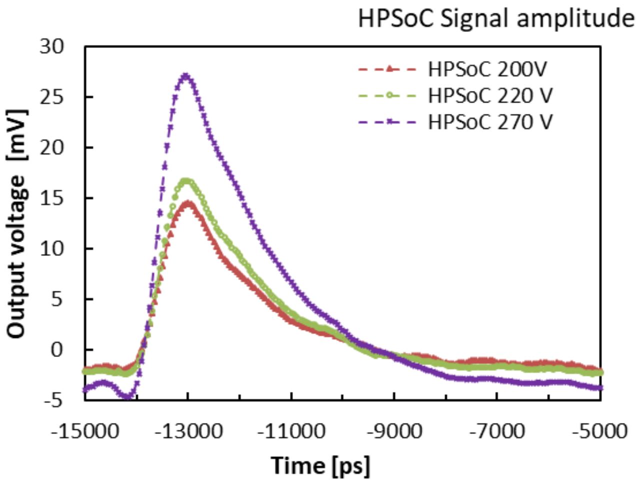


HP-SoC v1

- First prototype developed, fabricated and tested through SBIR Phase-1 funding (DOE-SC0021755)
- 4 channels, sampling array and conversion logic, digital control but limited functionality
- Focus on characterization on 1-ch transimpedance amplifier and gain stage with LGAD sensor

- Reached 600 ps rise time and ~45 ps jitter: main issue was the lower than expected output signal amplitude = front-end gain





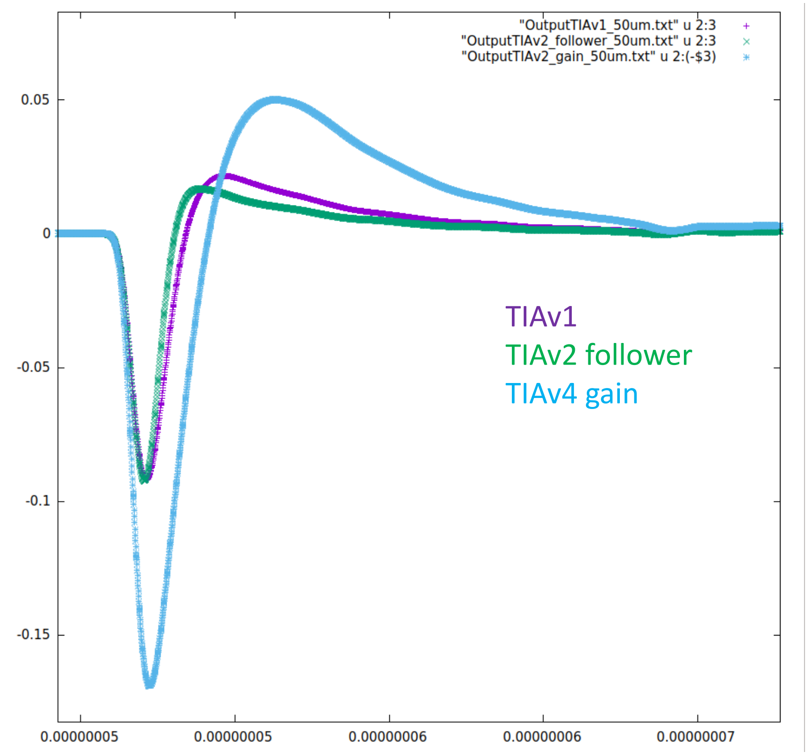
TWEPP 2022: https://indico.cern.ch/event/1127562/contributions/4904727/ https://arxiv.org/abs/2210.09555v2

HP-SoC v2

- Co-funded by FY23 EIC/Jefferson Lab Generic R&D grant
- Optimized front-end design informed by the testing results from the initial prototype chiplet
    - Improved TIA and gain stage: higher signal amplitude
- Independent front-end amplifier to permit separate evaluation of the analog performance

- Full digitizer
- New internal discriminator
- On-chip autonomous operation via self-triggering

- Chip submitted in May, received in September 2023



Key developments to v2

- Assuming 0.4 pF input capacitance
- Simulation before any parasitics
- In order to achieve timing resolution below 30 ps, it is likely necessary to go to thinner sensors (Landau distribution of charge deposition can only be reduced in this way)

	TIAv1+Gain v1	TIAv2 + follower	TIAv2 + Gain
Gain (signal/ freq=0)	6.48/13 (kOhm)	6.50/9.9(kOhm)	11.9/43(kOhm)
Rin (signal/freq=0)	872/1.4k (Ohm)	177/246 (Ohm)	63/254 (ohm)
Bandwidth	228Mhz	356MHz	129MHz
Rise time	649ps	627ps	691ps
Output bias	357mV	359mV	249mV
Noise (5 GHz)	0.093mV	0.162mV	0.14mV
Current	1.63mA	2.4mA	3.15mA (2.24mA final)
Vpeak (from Base)	92mV	92.3mV	169mV
Estimated jitter (assuming 1 mV total noise)	8.8ps	8.5ps	5.1ps

50 µm (~10 fC signal)

	TIAv1+Gain v1	TIAv2 + follower	TIAv2 + Gain
Gain (signal/ freq=0)	3.05/13 (kOhm)	3.16/9.9(kOhm)	5.15/43(kOhm)
Rin (signal/freq=0)	503/1.4k (Ohm)	117/246 (Ohm)	29.5/254 (ohm)
Bandwidth	228Mhz	356MHz	129MHz
Rise time	348ps	332ps	368ps
Output bias	357mV	359mV	249mV
Noise (5 GHz)	0.093mV	0.162mV	0.14mV
Current	1.63mA	2.4mA	3.15mA (2.24mA final)
Vpeak (from Base)	43.3mV	44.9mV	73.6mV
Estimated jitter (assuming 1 mV total noise)	10ps	9.24ps	6.24ps

20 µm (~4 fC signal)

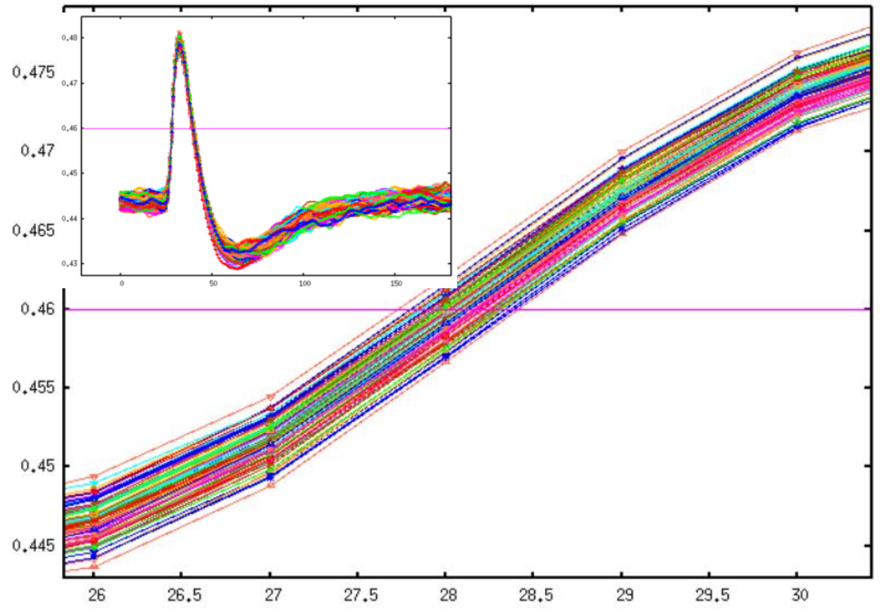
Power consumption estimate

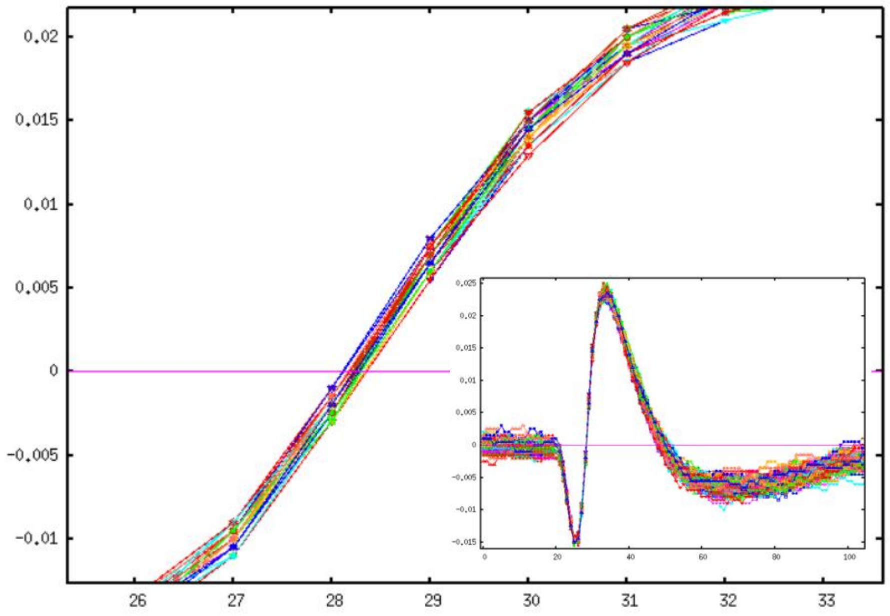
- TIA (with gain): 2.24 mA
- Trigger: 0.720 mA
- Ramp: ~30 µA
- Comparator: 256x1 µA = 0.256 mA
- Total w/out clock and counter distribution: 3.25 mA
  - Ca. 3.3 mW (1 V op)

Waveform digitization

J. Ott et al, HP-SoC Update

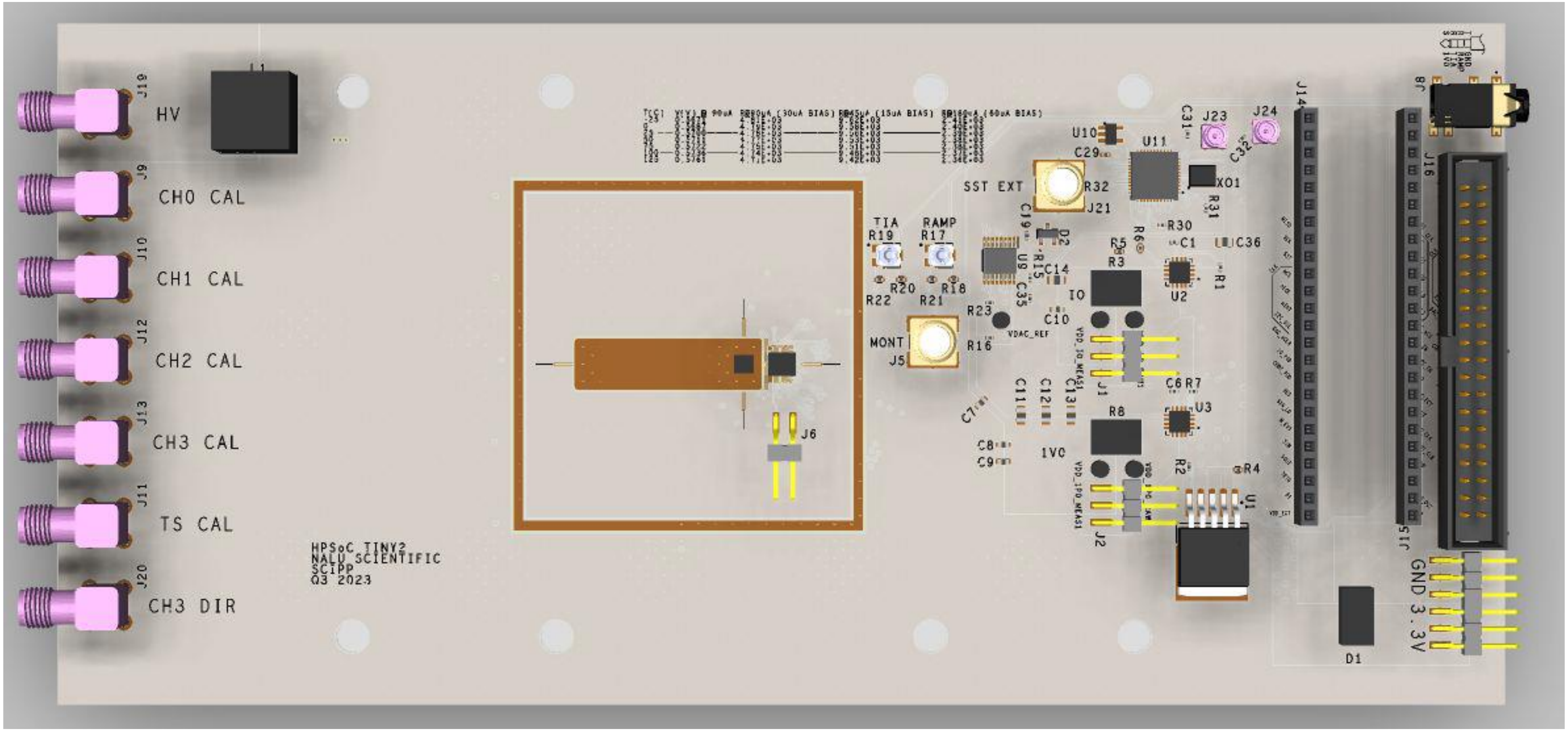
- Waveform digitization at 10 GS/s (10-bit): allows digital baseline correction, constant fraction discrimination and other algorithms for improving jitter component of the timing resolution
- Simulated HP-SoC v2 output digitized waveforms with noise: estimated reduction from 13.7 ps (leading edge) to 5 ps





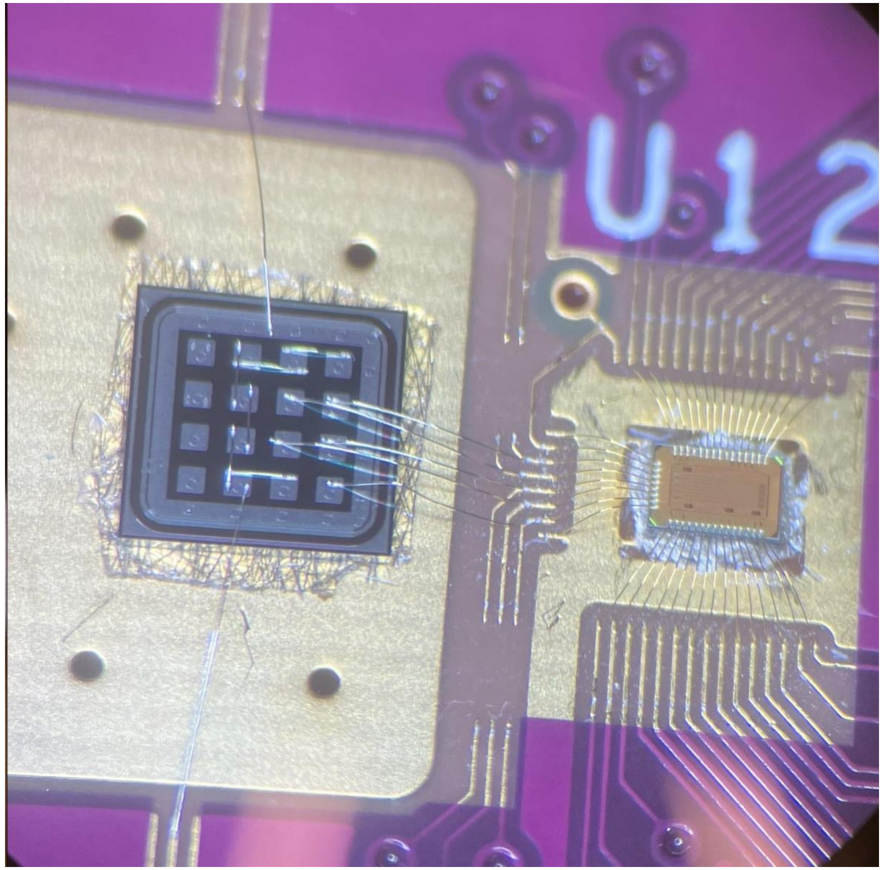
➢Classification of digitized waveforms with machine learning ?

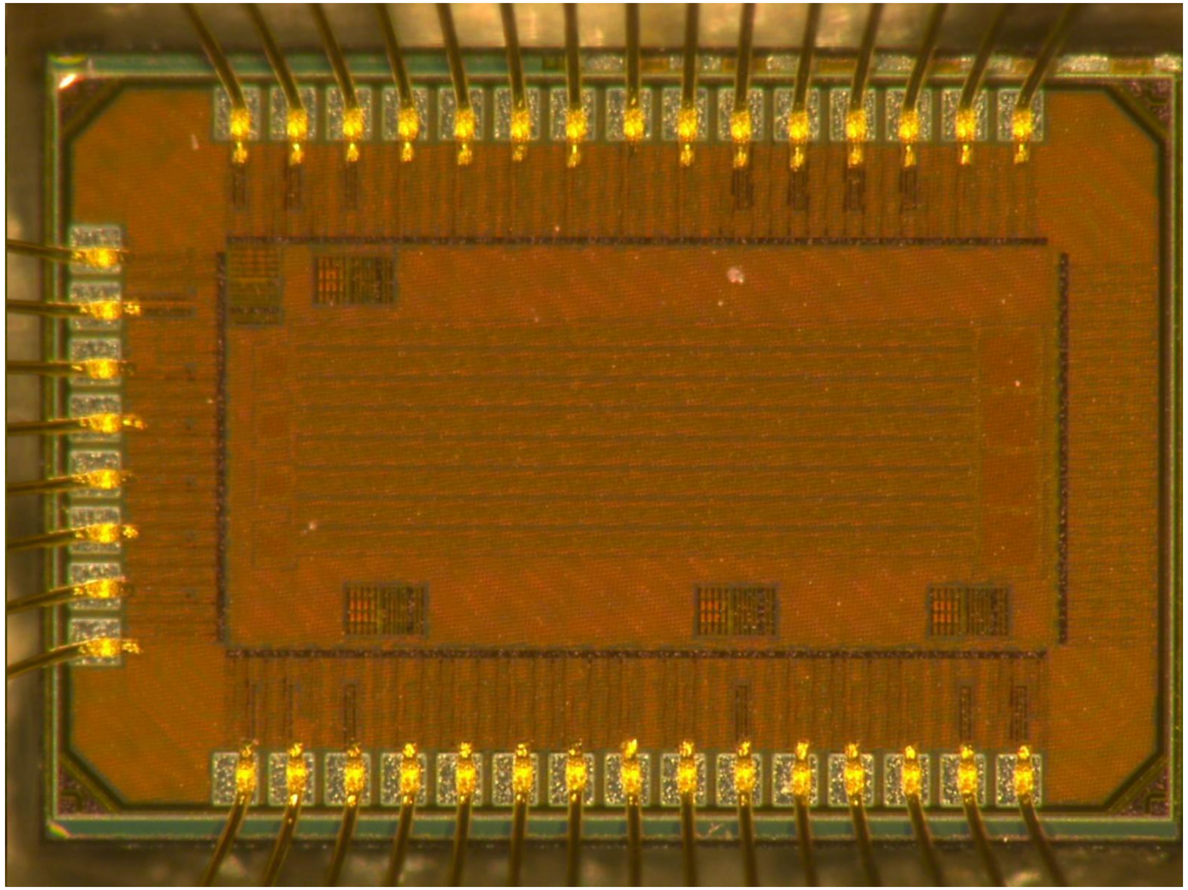
HPSoCv2 evaluation board



Fabricated chip

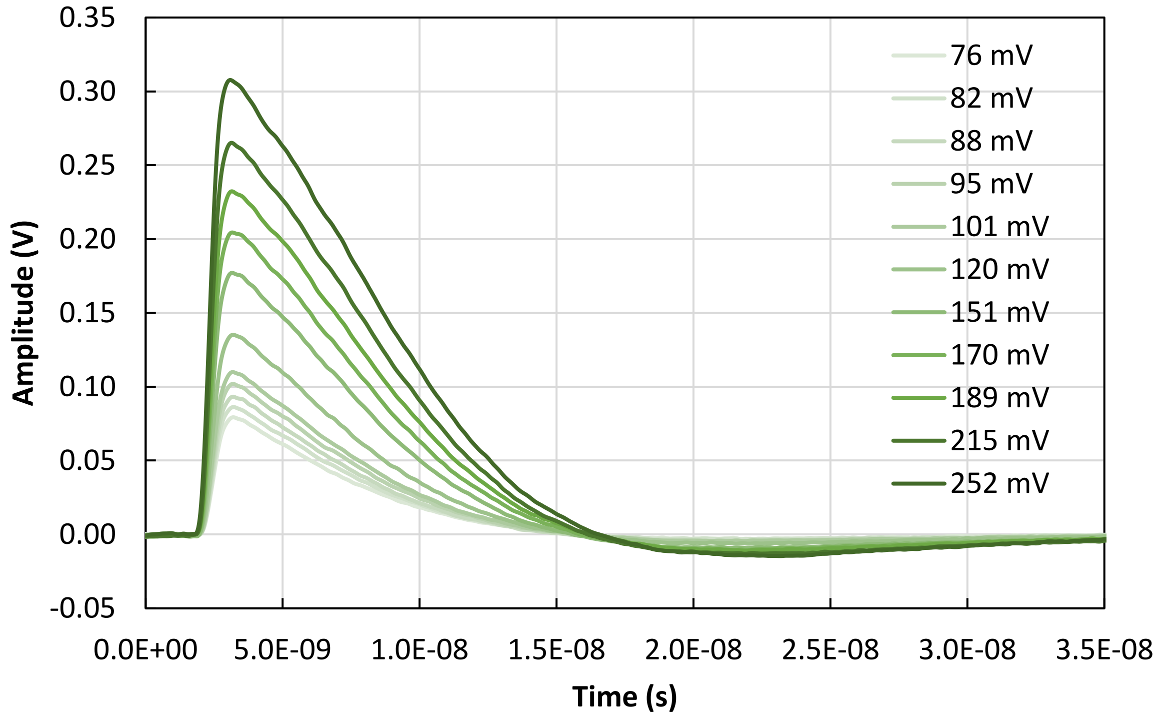
- Initial shorting of wirebond heels to chip seal (metal frame) required adjustments to bonding wire and parameters!

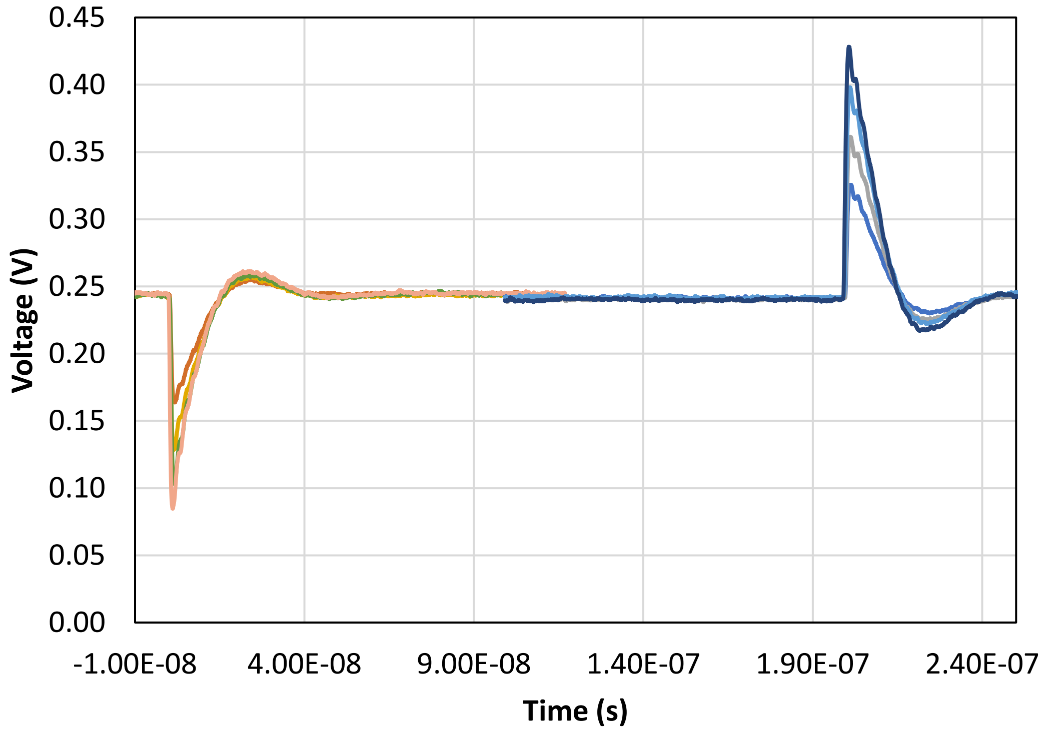




Calibration with external injection

- After adjustment of transimpedance amplifier bias, signals of either polarity could be detected without reaching saturation
  - On chip, triggering is targeting only the expected signal polarity from p-type sensors

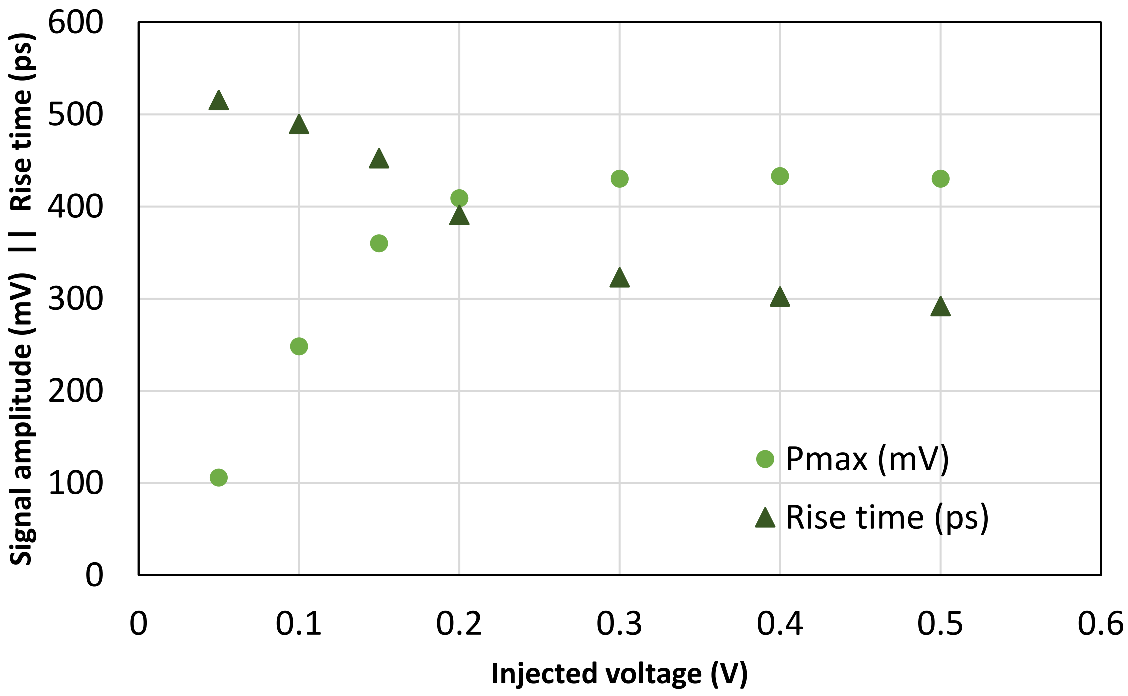


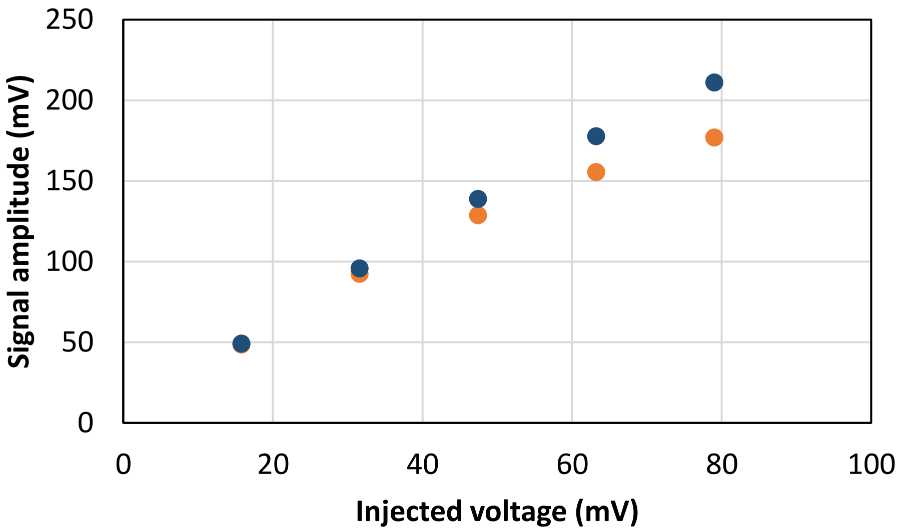


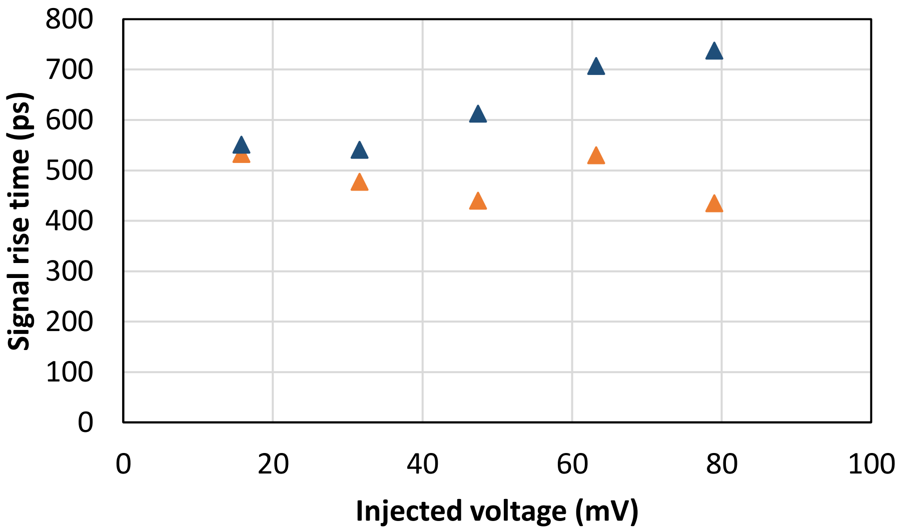
J. Ott et al, HP-SoC Update

Calibration with external injection

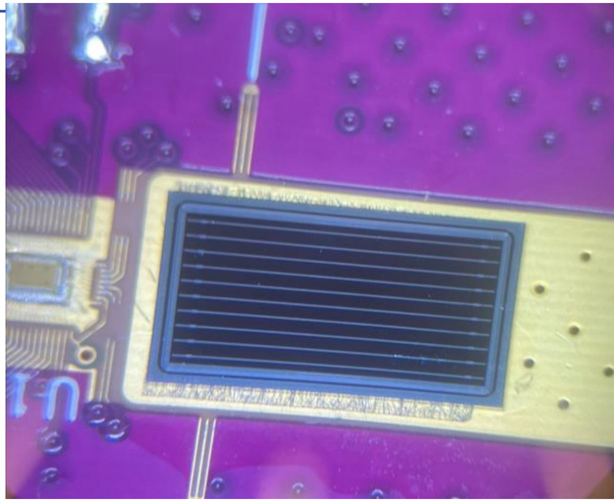
- Signal linear up to ~200 mV = 100 fC
- Gain (at highest setting) is improved significantly compared to v1
- Rise times down to 450-500 ps!







Characterization with sensors



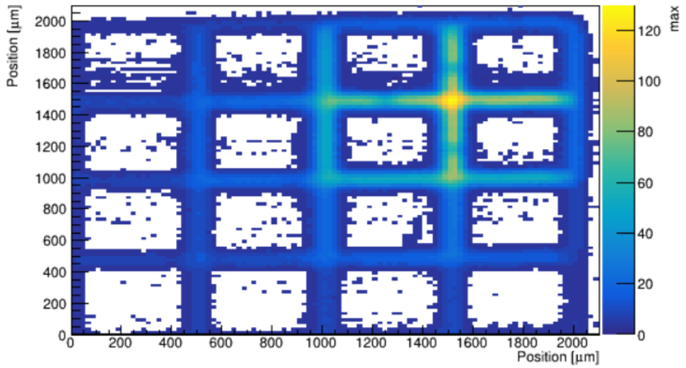
HPK AC-LGADs, 500 µm pitch

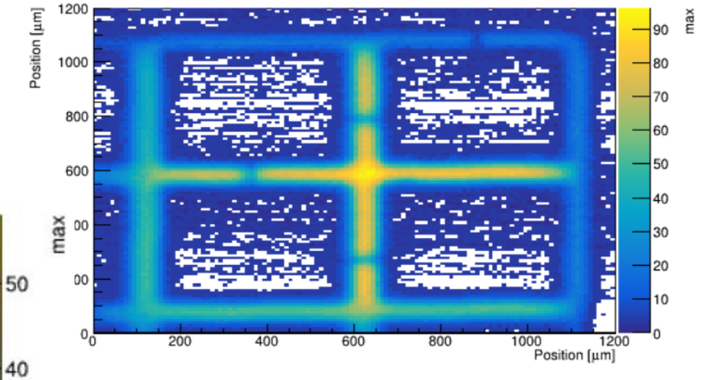
- 4x4 pad array, type C600, 50 µm thick, 300 and 450-µm pad size
  - Tested with laser and Sr-90 beta source
- 1 cm strip, 50 µm thickness, 50 µm metal width, type C600
  - Tested with laser, tests with source to be done soon
  - Noise: on the order of 2 mV – has not degraded significantly with larger strip sensor capacitance

Data acquired using GHz probe and oscilloscope connected to standalone TIA output – 3-4 channels are connected for full digitization, but were not read out yet

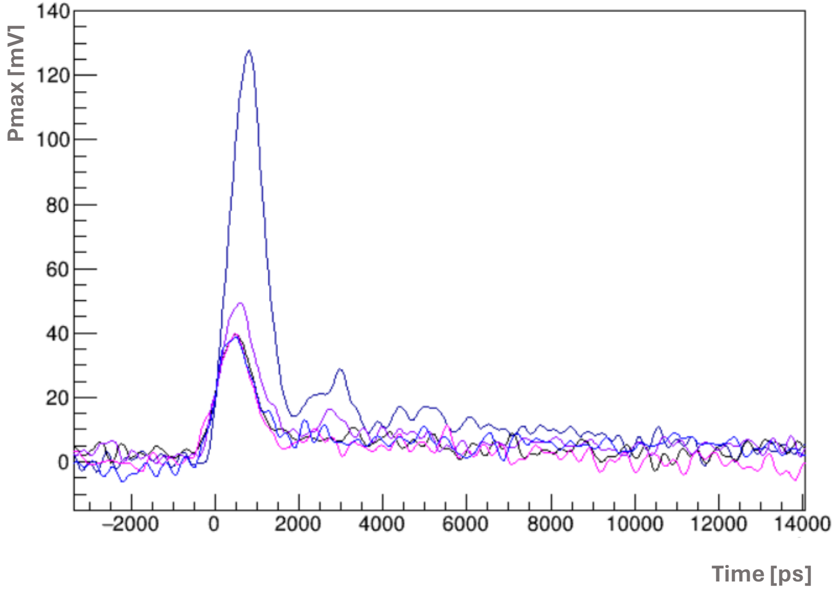
Characterization with sensors

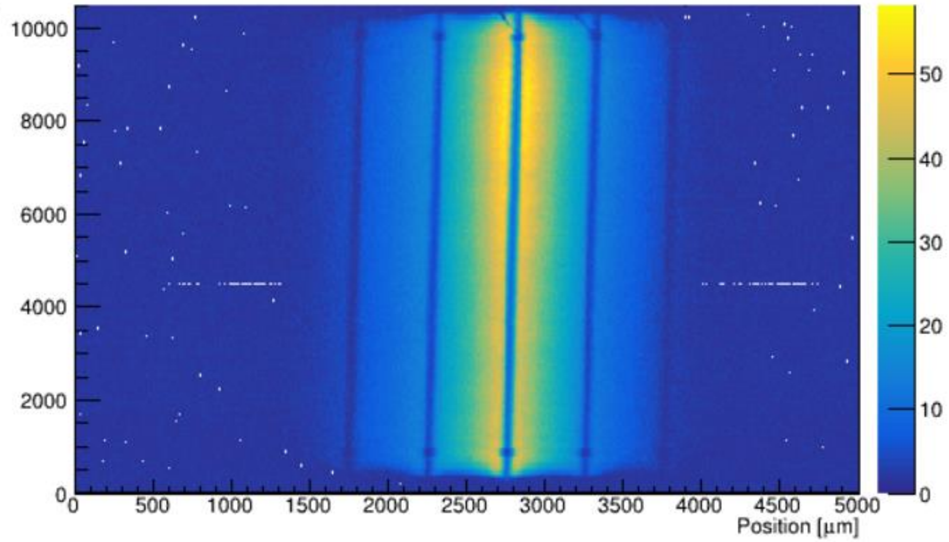
- x-y scans of pad and strip sensors were conducted
- E.g. strip sensor: rise time 600-750 ps, jitter ~35 ps





- Beta source exposure of pad sensor (self-triggered): MPV 40 mV, rise time 550 ps, noise rms 1.8 mV





Digitizer testing

- So far operated only at Nalu with calibration input and/or supplied waveform
- Firmware development finished recently
  - Will be made available also at SCIPP for evaluation of the full system with sensor and multiple channels
- Initial testing of internal delay line, internal conversion clock generation and counter, comparator, ramp has been conducted
  - Functional bug in joint control of ramp and counter prevents full internal conversion
  - Planning to submit a corrected version of the chip immediately, at the end of the month
- Alternative approaches still allow majority of chip testing, including pedestal acquisition and synchronous wave acquisition & conversion
- Power consumption: 24 mW for 4 channels with full digitization + 1 additional TIA + clock. Adjustment not perfect yet – may reach closer to targeted 3.3 mW/channel

Conclusions

- The second revision of HP-SoC has been designed and fabricated, incorporating most of the functionality envisioned for the final implementation
- Preliminary results from the first month of testing with both calibration inputs and sensors are encouraging:
  - Pre-amplification seems compatible with high performance readout of state-of-the-art LGAD sensors
  - Most digitizer modules perform according to the specifications
  - Functional errors precluding full architecture assessment are being addressed with additional testing of present and old prototyping and new fabrication
- HP-SoC v3: 9-channel module – pending funding decisions
  - To utilize results from previous front-end and digitizer evaluation
  - Optimization of feature extraction mechanisms based on acquired data
  - Channel fusion information based on experimental data from multiple channels

https://indico.jlab.org/event/751/contributions/13575/attachments/10453/15696/EIC-HPSoC%202023-24-%20response%20to%20reviewers%20(1).pdf