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CRYO ASIC: A System-on-Chip (SoC) for Charge Readout in the nEXO Experiment

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CRYO ASIC plays a vital role as the charge readout component in the nEXO experiment. Its primary purpose is to process signals from sensors situated within the liquid xenon chamber, facilitating the study of phenomena such as neutrinoless double-beta (0νββ) decay and other rare events. Featuring a compact system-on-chip (SoC) architecture in a small 7mm x 9mm form factor, its primary functions involve signal preamplification, channel multiplexing and waveform digitization, enabling it to convert analog data generated by interactions within the liquid xenon detector into a digital format suitable for in-depth analysis. Designed to operate reliably under the extreme cryogenic temperatures of nEXO, preliminary assessments conducted at ~165K indicate that the CRYO ASIC, presently in its R&D prototype phase, is steadily approaching compliance with nEXO's stringent requirements.

This talk provides a comprehensive overview of the CRYO ASIC's architecture, describing design choices made to align with the experiment's demands. Furthermore, it outlines key specifications and encompasses future design implementations to reach its final version. A dedicated bench setup developed at SLAC is also described for initial chip characterization at cryogenic temperatures. Results from two ASICs operating efficiently at ~165K will be presented, demonstrating how these findings mitigate early-stage critical design risks within the nEXO project.

Early Career

No

Primary author: PENA PEREZ, Aldo (SLAC)

Co-authors: DRAGONE, Angelo; GUPTA, Aseem; REESE, Benjamin; MARKOVIC, Bojan; LENARDO, Brian; DOERING, Dionisio; ANGELICO, Evan; HERNANDEZ, Hugo; YANG, Liang; ROTA, Lorenzo; CONVERY, Mark; BREUR, Sander; LI, Zepeng

Presenter: PENA PEREZ, Aldo (SLAC)

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