2023 Coordinating Panel for Advanced Detectors (CPAD) Workshop

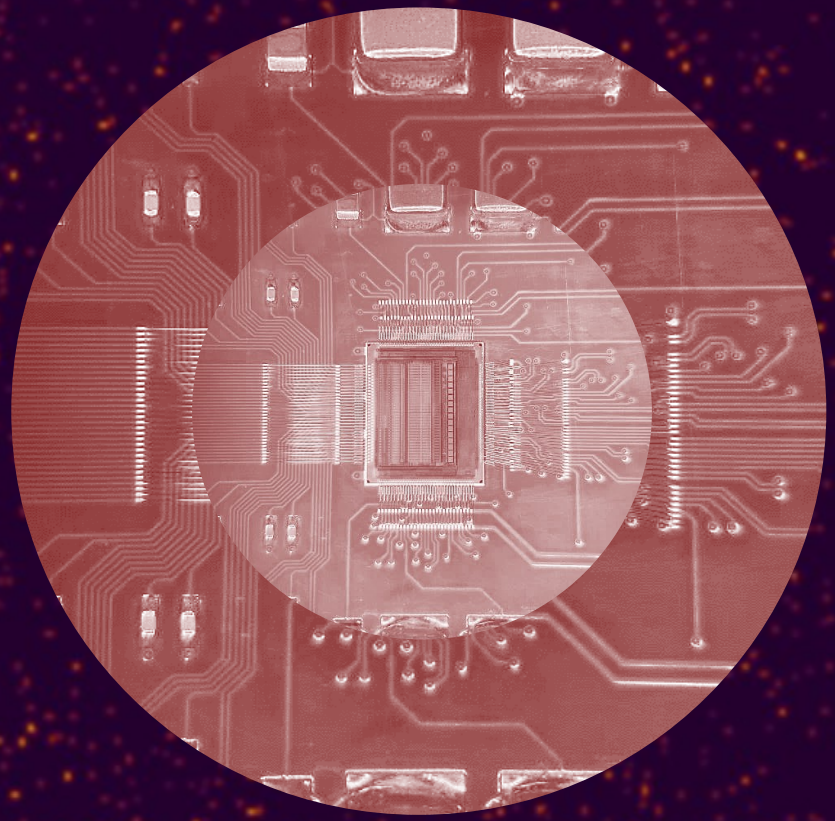
Nov. 7-10, 2023 | SLAC National Accelerator Laboratory

RDC4 | Readout and ASICs

ID: 77

CRYO ASIC

A System-on-Chip (SoC) for Charge Readout in the nEXO Experiment



Aldo Pena Perez on Behalf of SLAC TID-ID ICs Dept. and nEXO Collaboration

Thursday, 09 Nov 2023 | aldopp@slac.stanford.edu

SLAC | TID TECHNOLOGY INNOVATION DIRECTORATE

TID-ID INTEGRATED CIRCUITS DEPARTMENT

U.S. DEPARTMENT OF ENERGY

STANFORD UNIVERSITY

Agenda

1. **nEXO**

   A brief glance at the experiment

2. **CRYO ASIC**

   System-on-chip (SoC) for charge readout

3. **Functional verification at ~165K**

   SLAC test bench system and measurement results

4. **Ongoing work and conclusions**

   LXe setups and charge readout prototype for nEXO

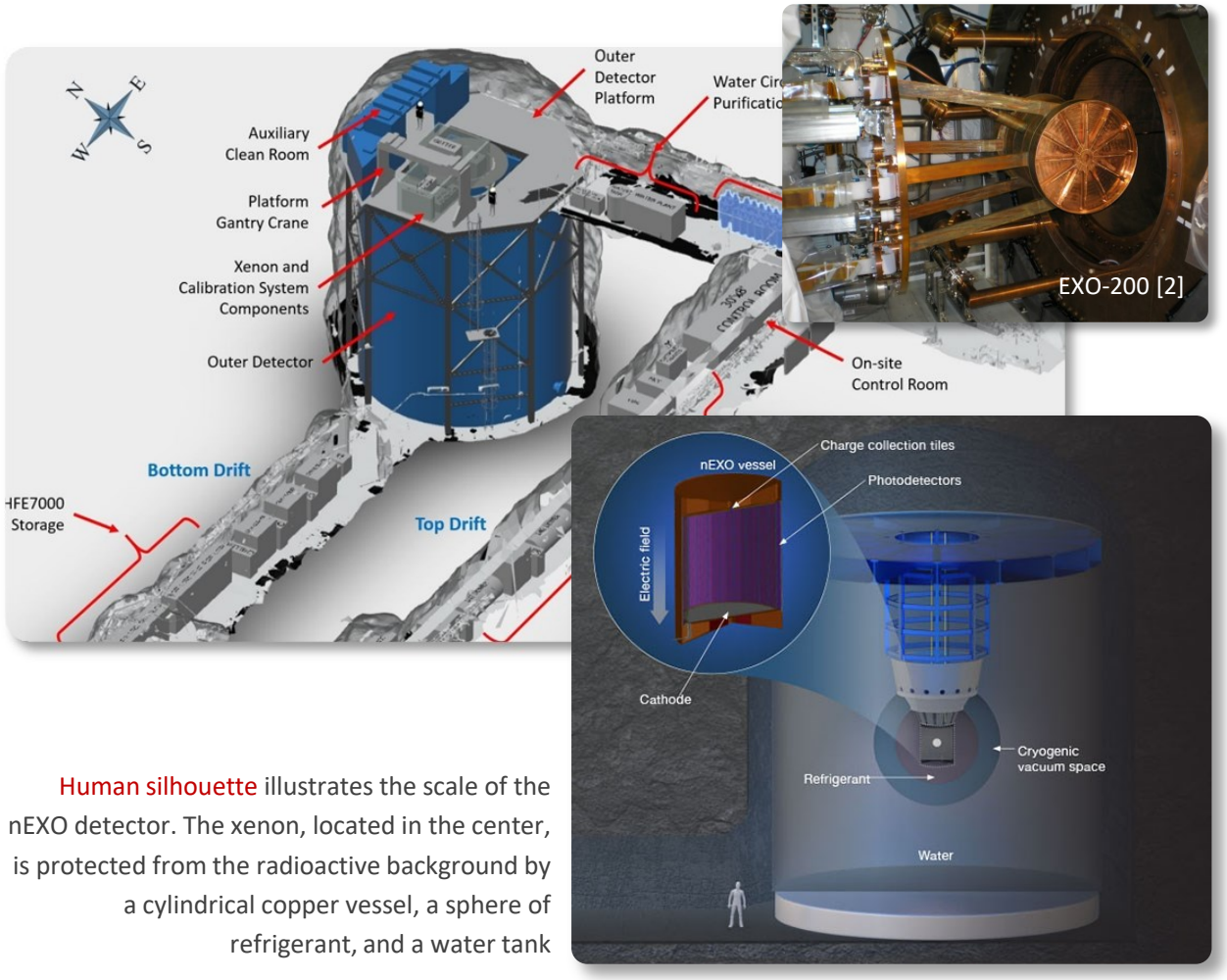
1

nEXO

A brief glance at the experiment

nEXO Experiment

A brief glance to the Experiment



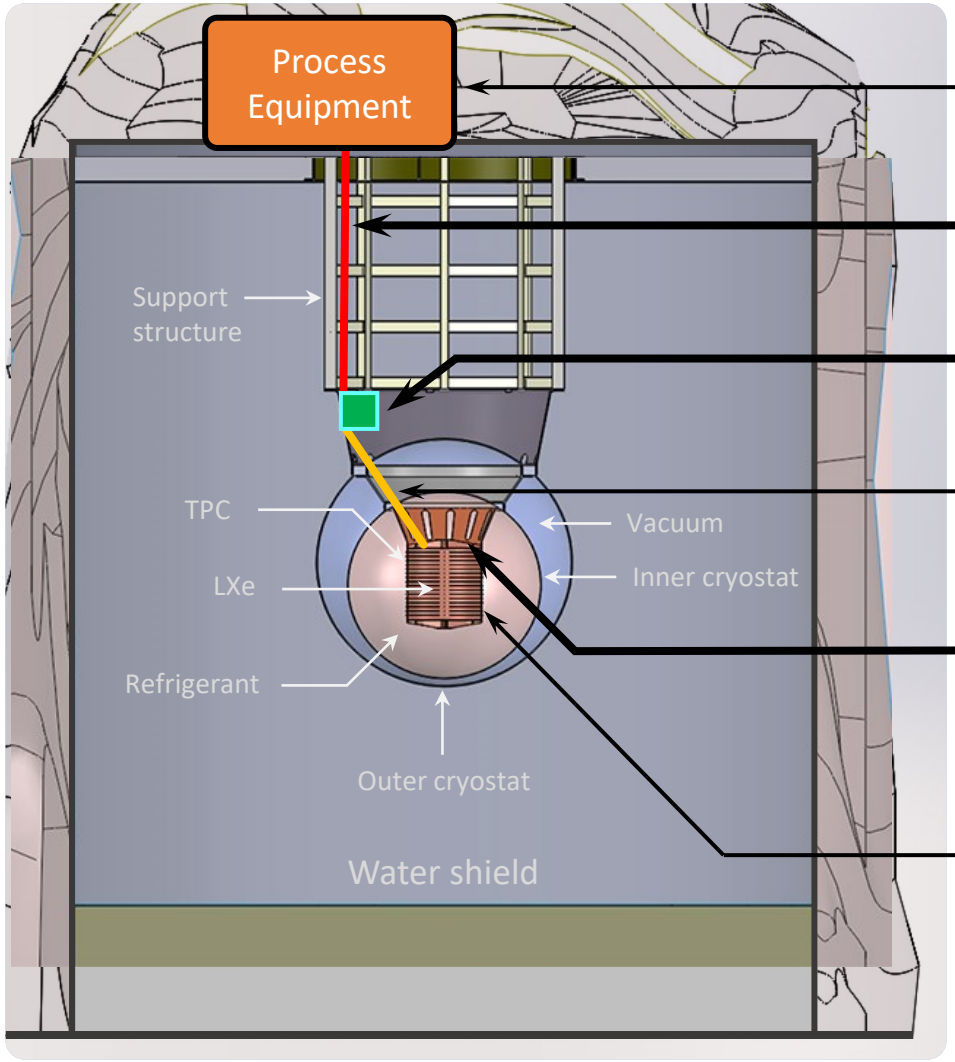
Human silhouette illustrates the scale of the nEXO detector. The xenon, located in the center, is protected from the radioactive background by a cylindrical copper vessel, a sphere of refrigerant, and a water tank

nEXO

Source: https://nexo.llnl.gov/

- **nEXO** [1] is designed as the successor of EXO-200 [2]
- **Mission:** Investigate neutrinoless double-beta ($0\nu\beta\beta$) decay
- **Core detector:** Single-phase 5-tonne Liquid Xenon (LXe) Time Projection Chamber (TPC)
- **Operating temperature**: ~165 K
- **Potential site:** SNOLAB, deep underground research lab located in Vale's Creighton mine near Sudbury, Ontario Canada
- **Location:** 2 km underground, providing protection from cosmic radiation

nEXO – Anatomy of the Electronics Sub-System



Backend for Charge Readout & Photon Readout Electronics (CRE, PRE):
Data reception, slow controls, trigger processing,
clock distribution, etc.

Transition box, upper conduit with power and data lines. Power supplies

Warm transition cards (LVDS to Fiber) for CRE & PRE:
Multiplex LVDS to fiber, LV + bias handling/distribution,
slow controls processing, etc.

Radiopure High-Speed Kapton Cables

Charge Tiles / Stave ← **Charge ASICs** + **ASIC Board** — **Charge**

SiPM Tiles / Stave ← **SiPM ASIC Board** — **SiPM**

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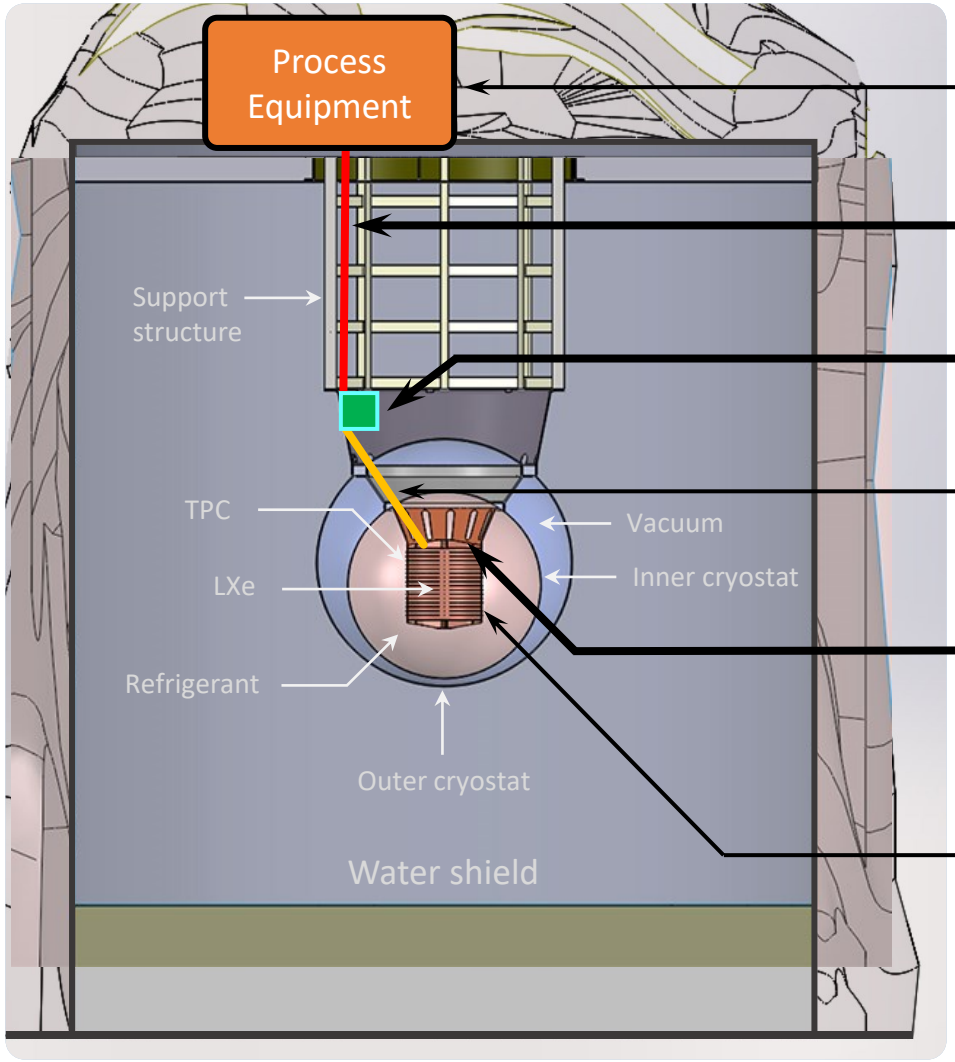

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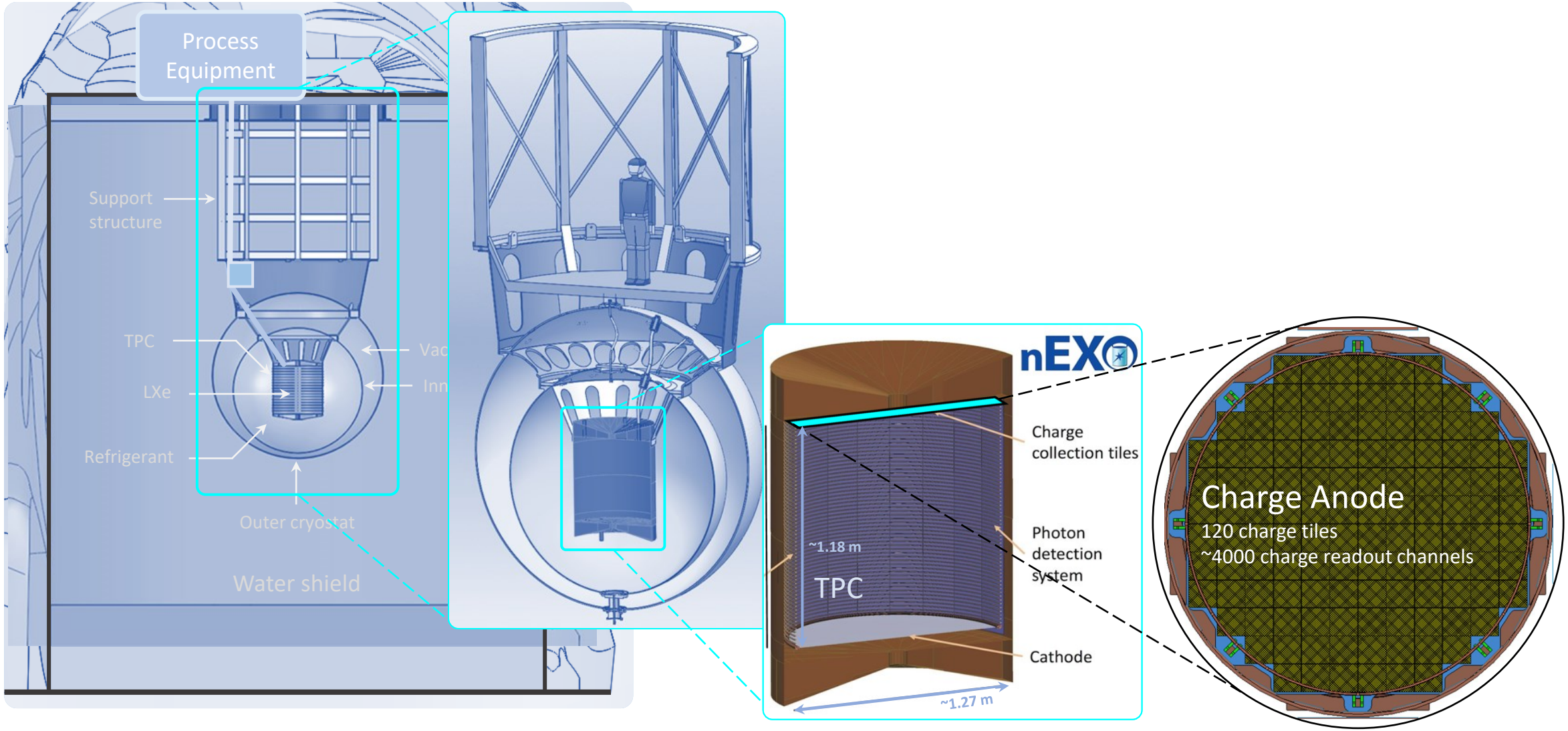
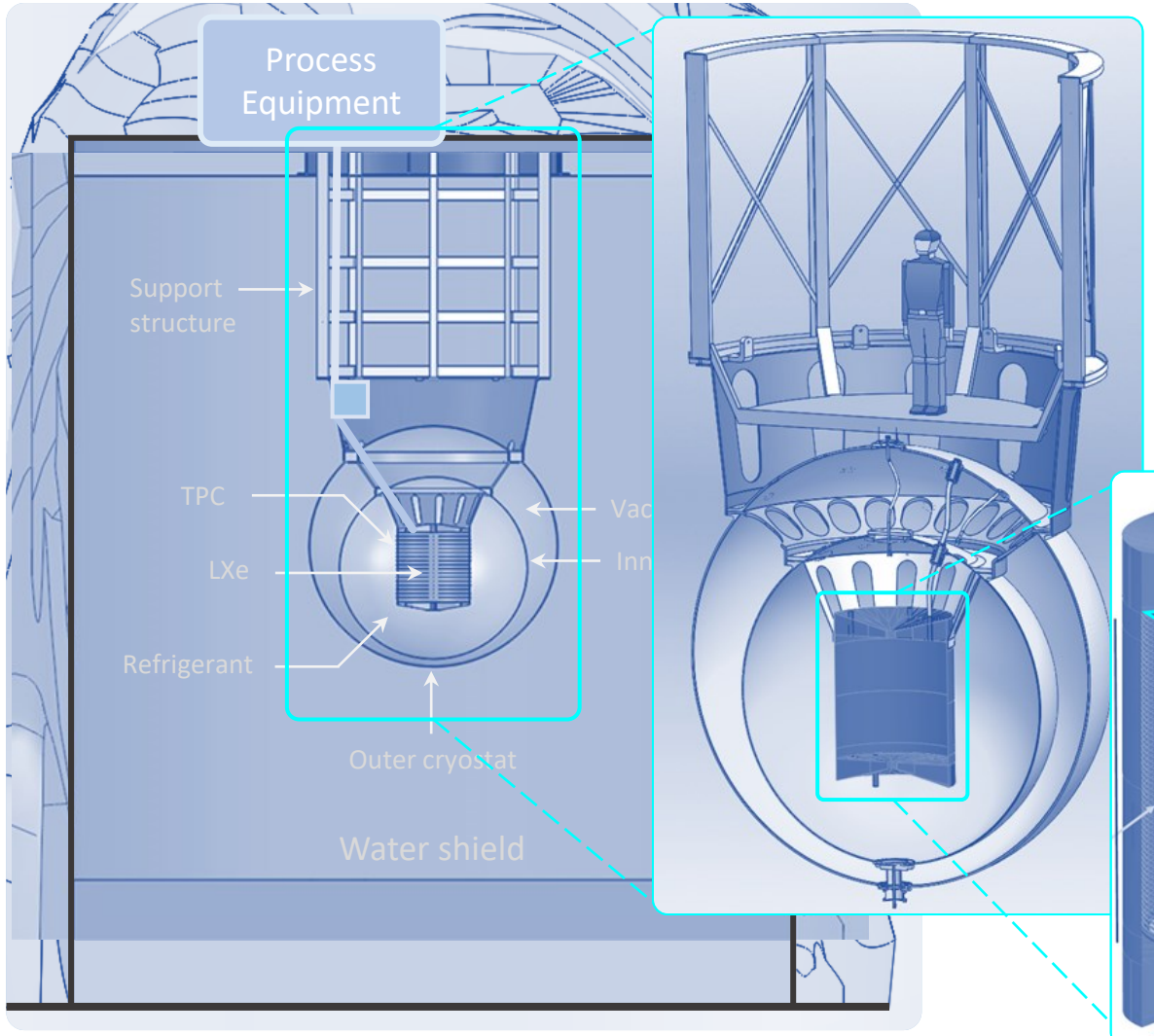
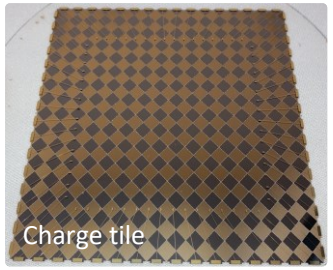
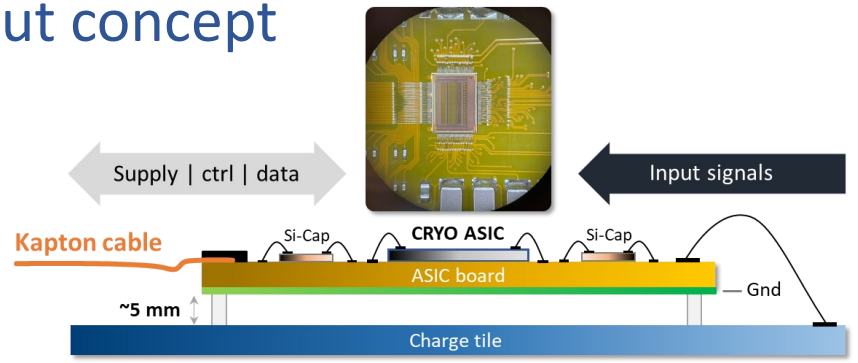


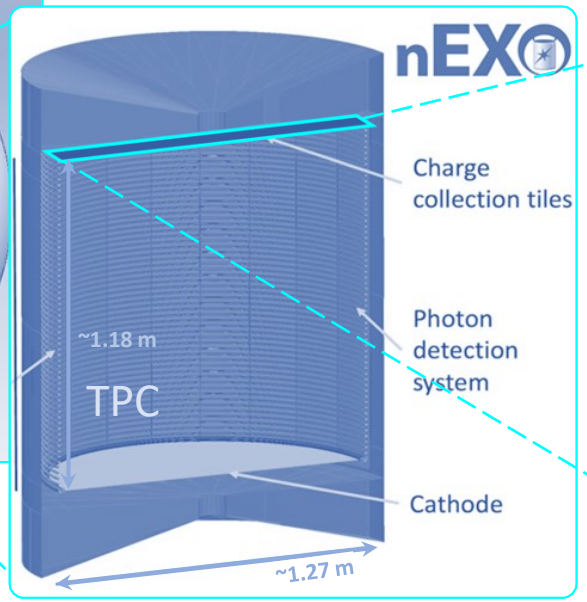
nEXO – Anatomy of the Electronics Sub-System

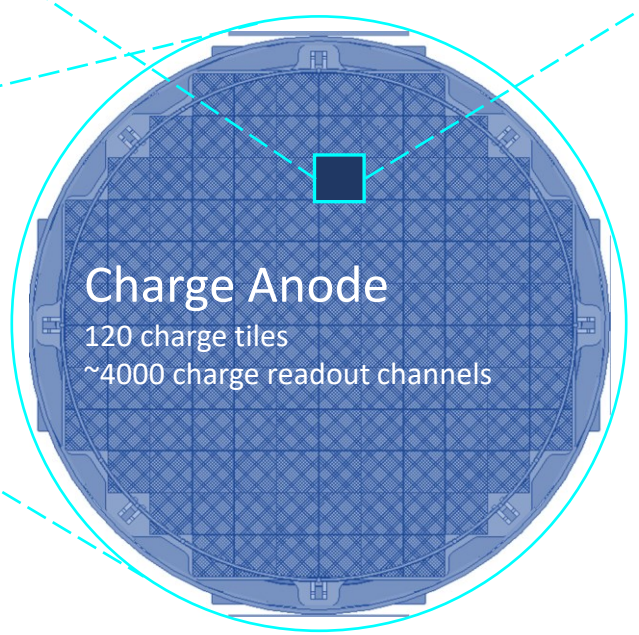


Charge readout concept









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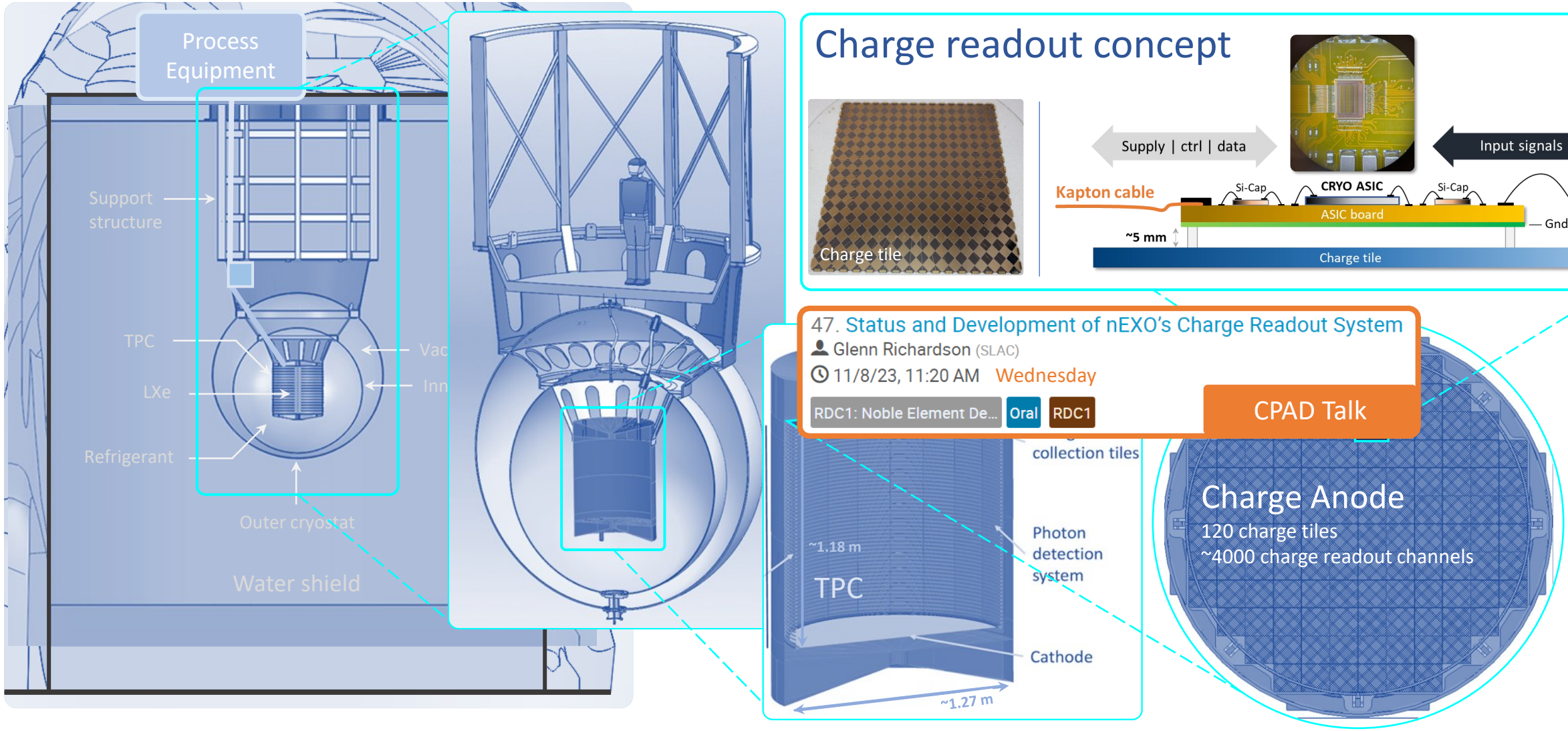


nEXO – Requirements

Crafting a specialized cryogenic ASIC close to the detector

- **Cold electronics vs warm electronics** → Improve noise & facilitates System-on-Chip (SoC) integration
- **Enhanced energy resolution** → Low-noise, highly linear charge amplification
- **nEXO's low radiopurity** → Reduce at minimum external components
- **Waveform digitization** → A-to-D conversion with digital data streaming
- **Location of digitization** → Improves signal integrity and enables channel multiplexing
- **Low power consumption** → ASIC approach eliminates the need for a heat sink
- **SoC ASIC solution** → Effectively reduces system complexity

ASIC specifications

TPC Experiment	nEXO			
CMOS process	130nm			
Supply voltage	2.5V (2V, 1V internal)			
Input capacitance	~ 20pF - 30pF			
Anti-aliasing filter	5th order Bessel architecture			
Peaking times	0.6us, 1.2us, 2.4us, 3.6us			
Gain settings	6.0X (57.2mV/fC)	3.0X (28.6mV/fC)	1.5X (14.3mV/fC)	1.0X (9.6mV/fC)
Max. input charge	25fC	50fC	100fC	150fC
Noise	< 150e- @ 3.0X and 1.2us			
ADC	12-bit 2MSPS / CH			
INL and DNL	±1LSB			
Power Consumption	< 15mW / CH (32-CH version)			
Temperature	LXe ~165K (-113ºC)			

2

CRYO ASIC

System-on-Chip (SoC) for charge readout

System-on-Chip for charge readout

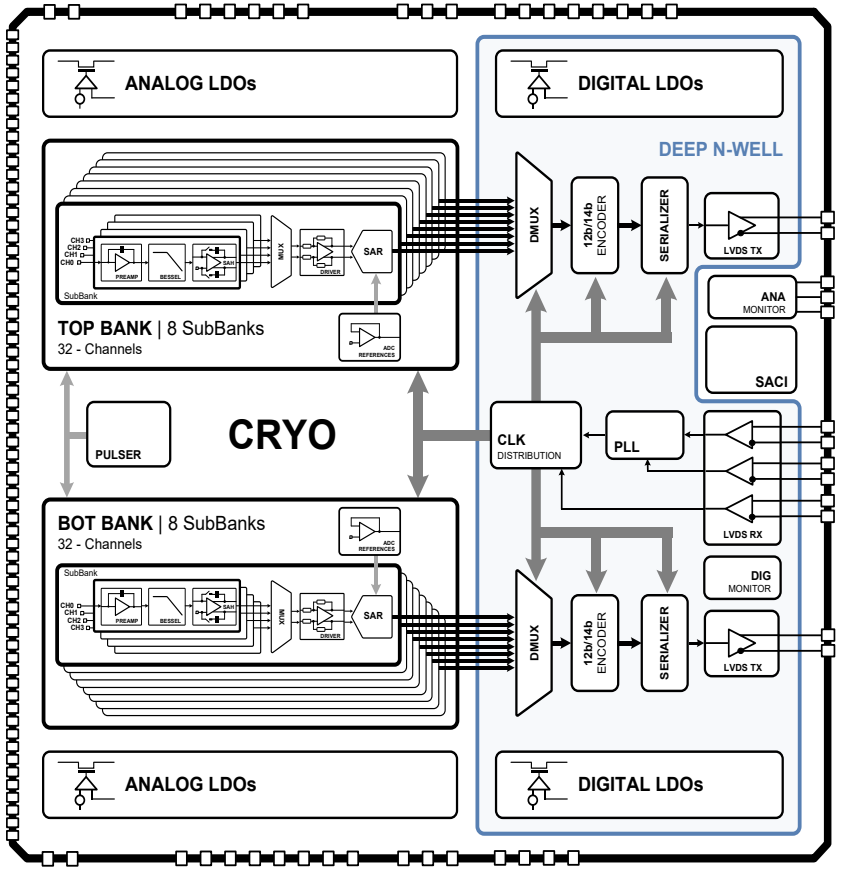
CRYO ASIC [2]-[4]

Key features

- System-on-Chip (SoC) architecture
- Linear charge preamplification with channel multiplexing, A-to-D conversion and digital data streaming
- On-chip supply regulation
- 64 inputs / 2 digital outputs
- Fully programmable:
  - 4 gain settings and 4 shaping times
  - Single and dual polarity signal
- **Small footprint:** 7mm x 9mm

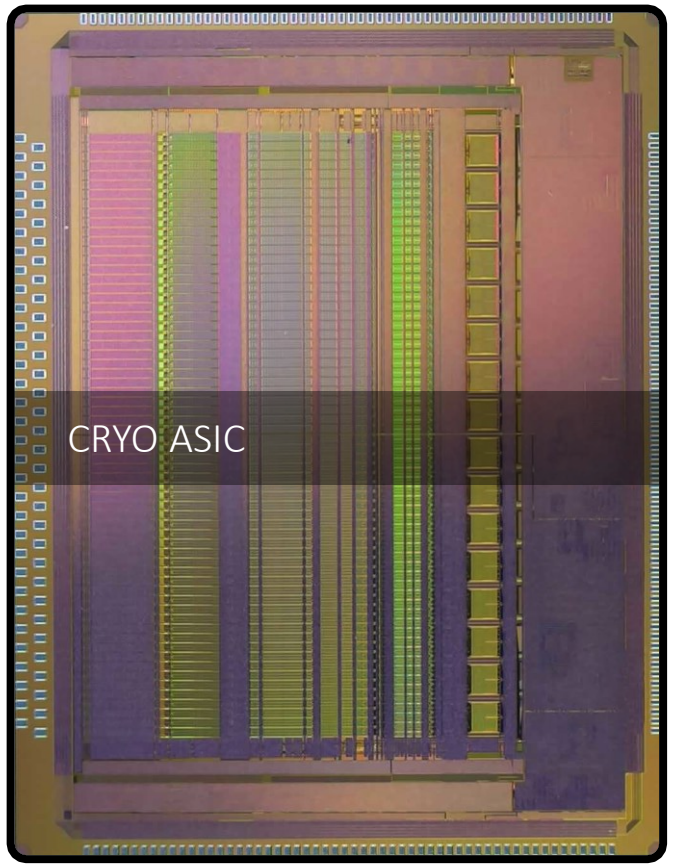
SoC Architecture

Analog/digital functions



Chip Photograph

R&D Prototype | 7mm x 9mm



System-on-Chip for charge readout

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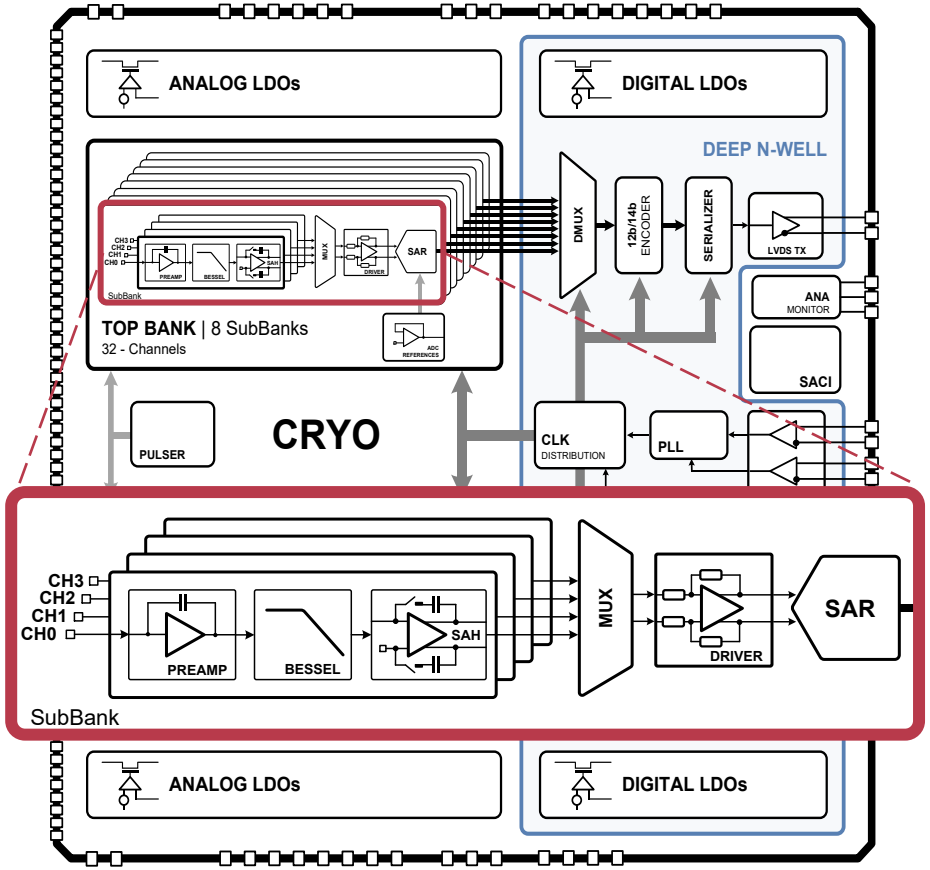
SoC Architecture

Analog/digital functions



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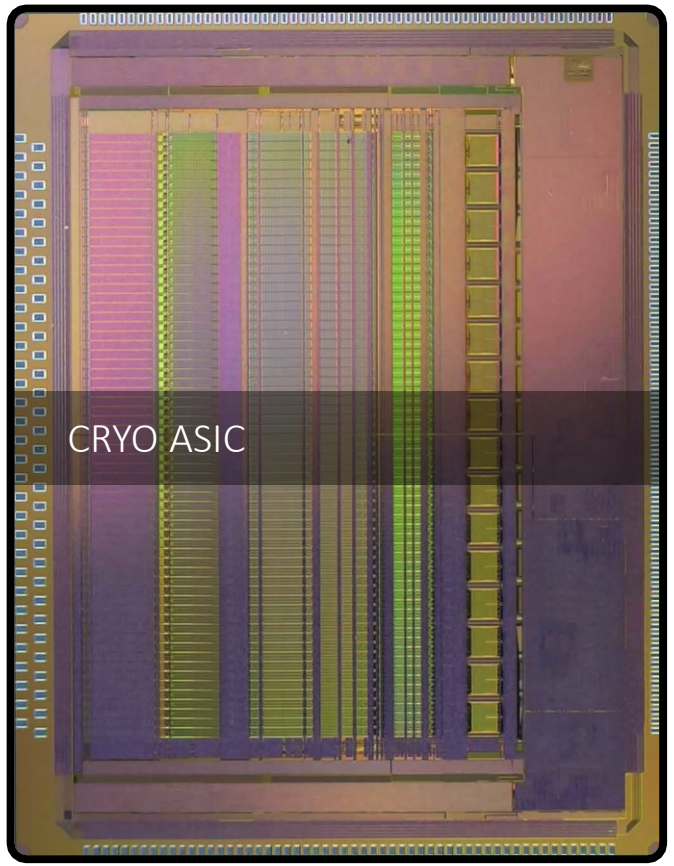

System-on-Chip for charge readout

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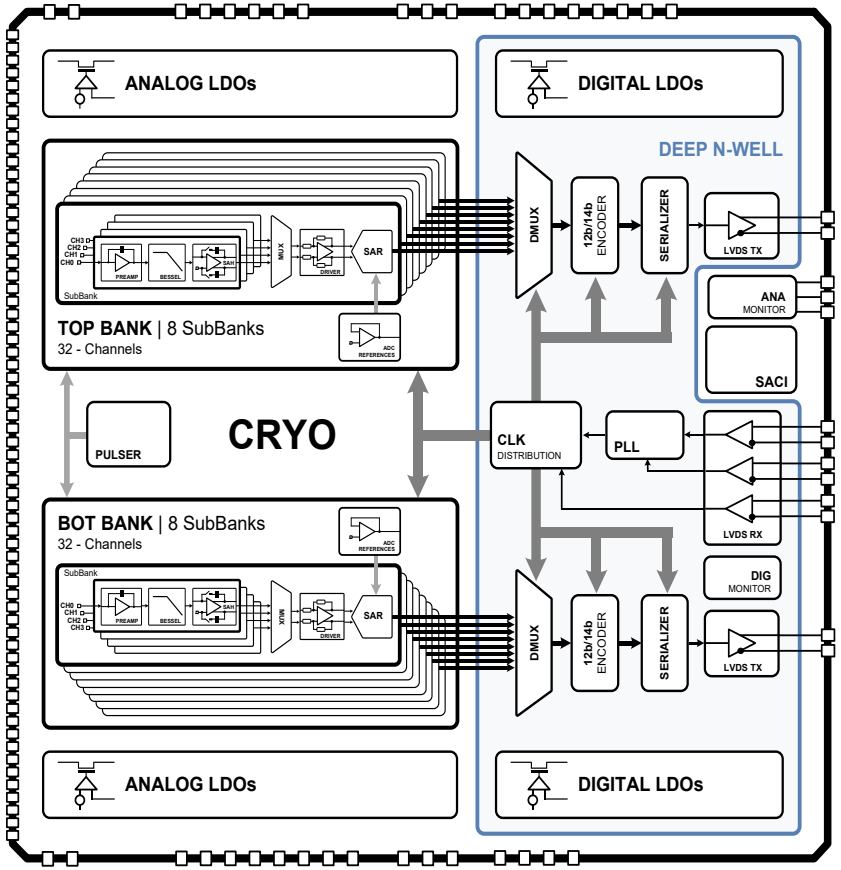
SoC Architecture

Analog/digital functions



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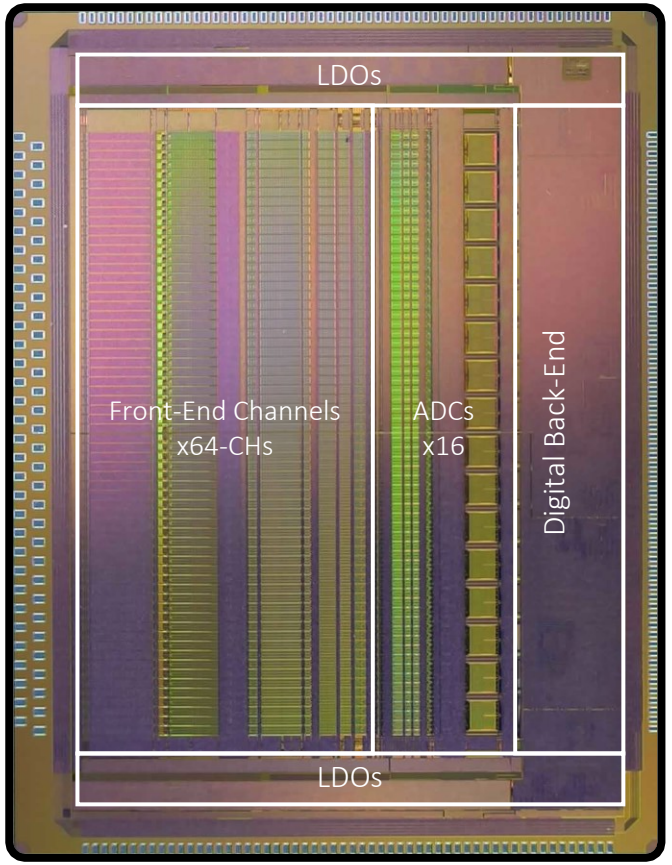

System-on-Chip for charge readout

CRYO ASIC [2]-[4]

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- On-chip supply regulation
- 64 inputs / 2 digital outputs
- Fully programmable:
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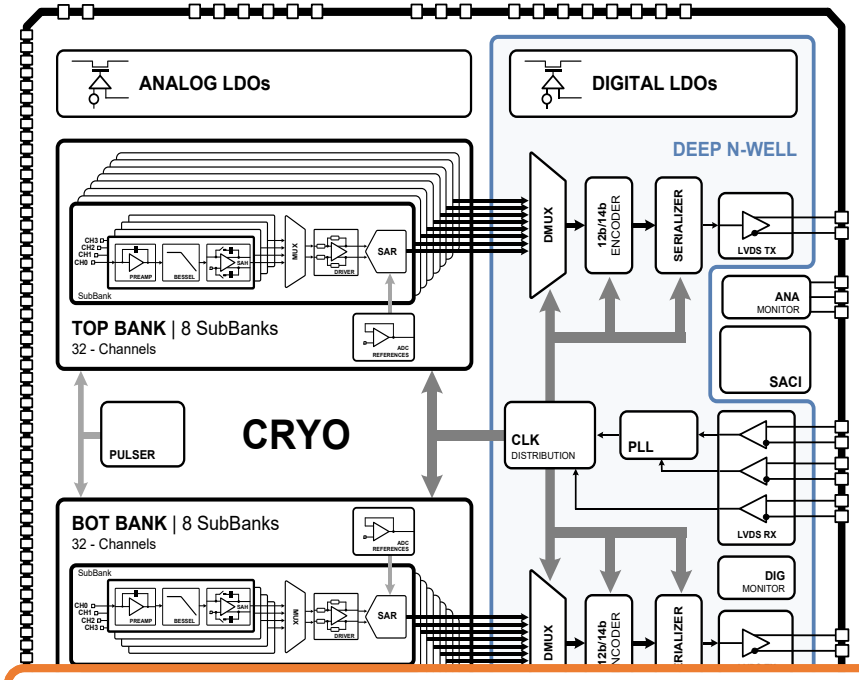
  - Single and dual polarity signal
- **Small footprint:** 7mm x 9mm
- Fully functional in LXe with performance close to requirements

SoC Architecture

Analog/digital functions



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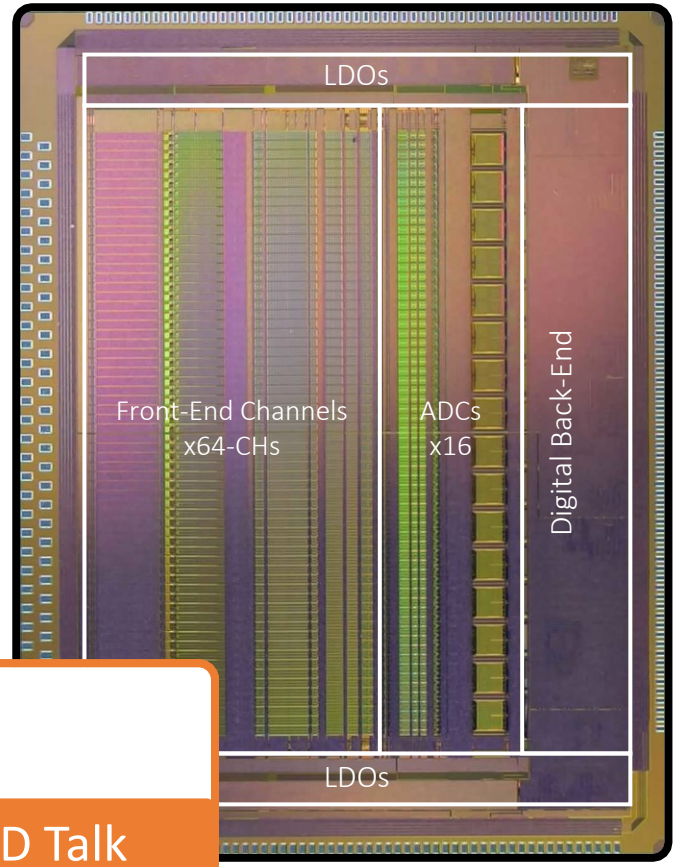


45. Testing of CRYO ASIC for the nEXO Experiment

Zepeng Li (UCSD)

11/10/23, 9:15 AM Friday

RDC1: Noble Element De... Oral

CPAD Talk

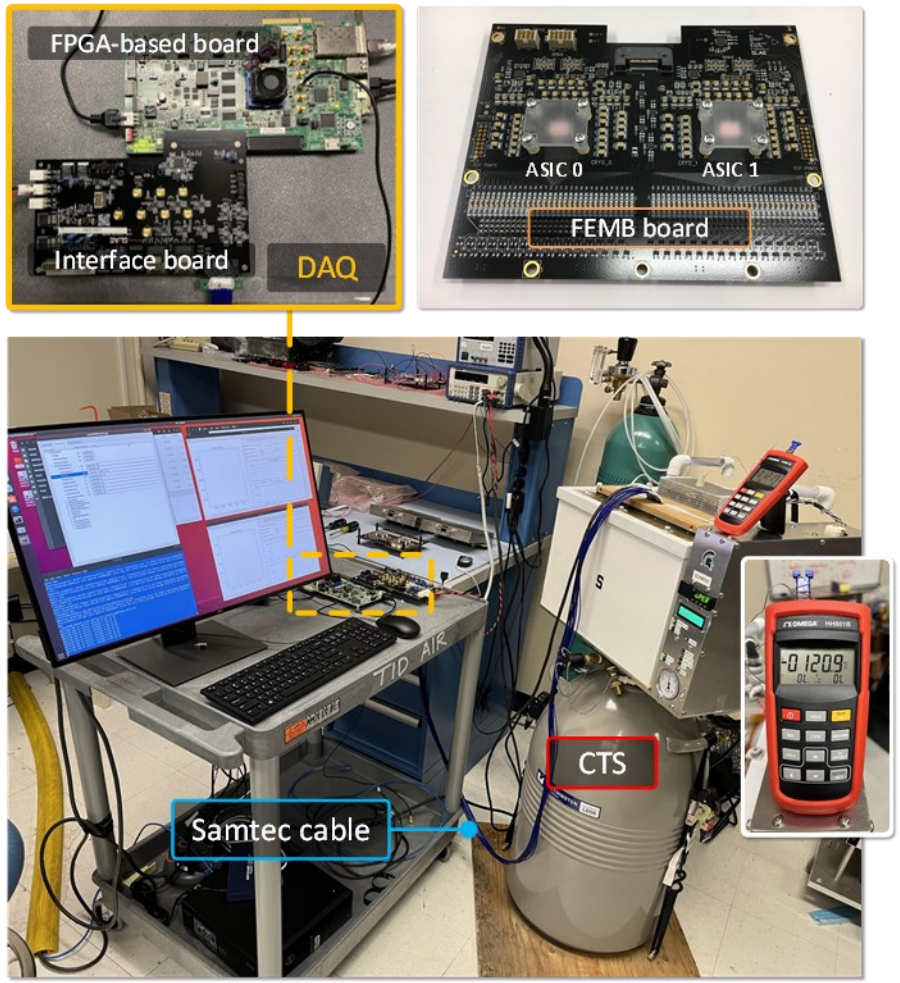
3

Functional verification at ~165K

SLAC test bench system and measurement results

Functional verification at ~165K – SLAC test bench system

Cryogenic test bench setup



Front-End Motherboard (FEMB)

- Allows the characterization of x2 ASICs simultaneously

Cryostat

- Cryostat Testy System (CTS) designed by Michigan State University
- Chip characterization at room and ~165K (cold gas mode)

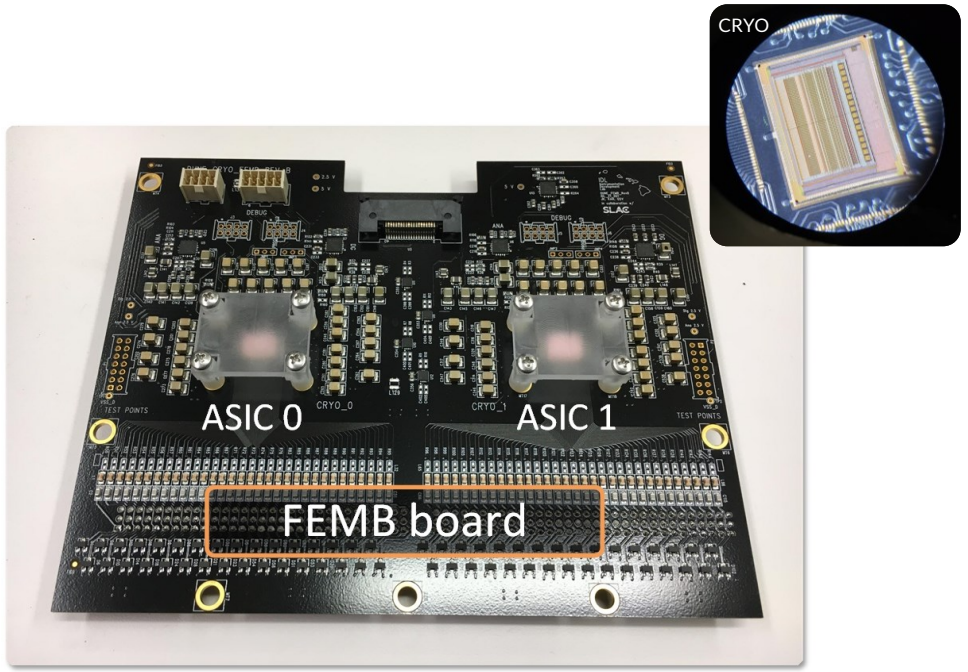
DAQ system

- KCU105 – Commercial FGPA based board
- Custom interface board to drive FEMB
- Custom ~3m high-speed SAMTEC cable for data and control
- Python-based GUI software, part of a ROGUE library [6]

Functional verification at ~165K

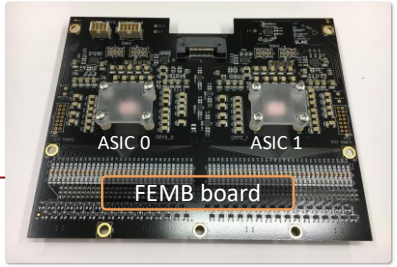
Verification

FEMB system	300 K	~165 K
ASIC initialization	✓	✓
On-chip supply regulation (LDOs)	✓	✓
Reference generation of ADC	✓	✓
Settings and configuration through SACI	✓	✓
Data communication (CRYO ASIC - FPGA)	✓	✓
LVDS TXs and RXs	✓	✓
Analog front-end response/settings	✓	✓
ADC section	✓	✓
Back-end operation	✓	✓
Full-chain of CRYO ASIC	✓	✓



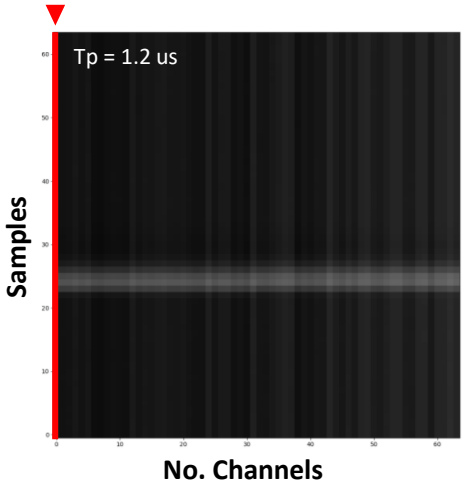
- **Initial R&D prototype strongly mitigated risk for the project:** Full functionalities demonstrated. Initial chip characterization of CRYO ASIC shows performance close to requirements

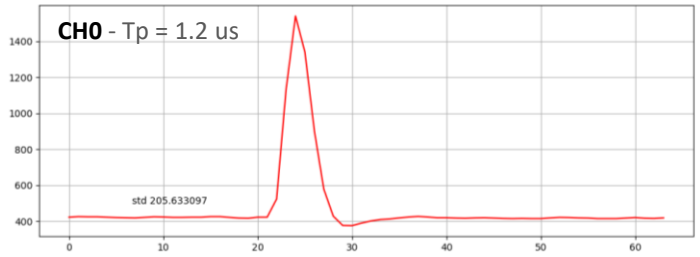
Functional verification at ~165K

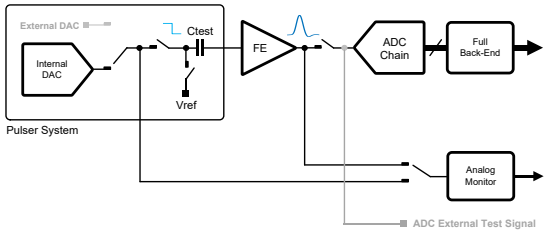


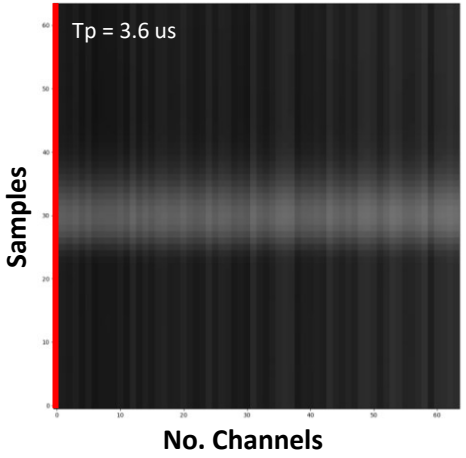
Pulse response at gain 1.5X, nominal speed (2 MSPS)

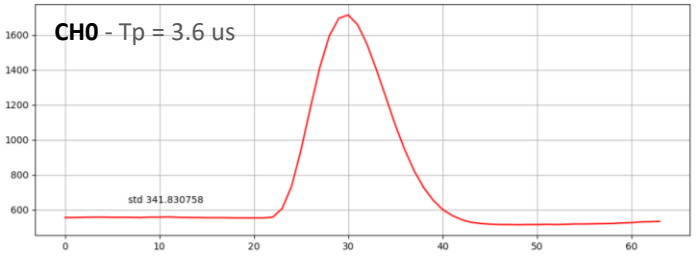
ASIC-0 | Single Polarity







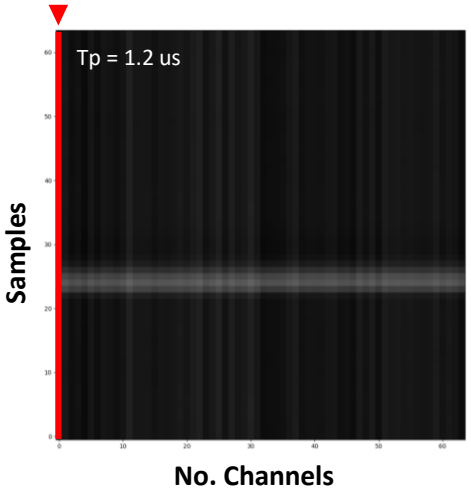


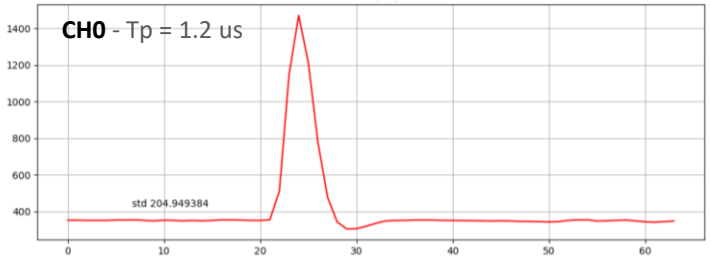


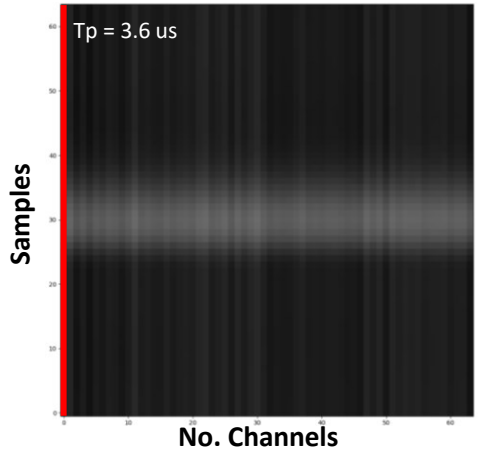
Note:

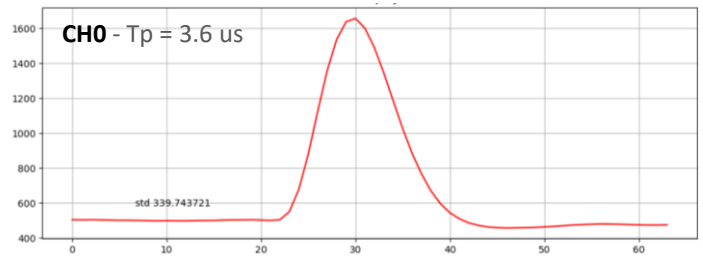
CH0 is shown. Other channels show similar response

ASIC-1 | Single Polarity

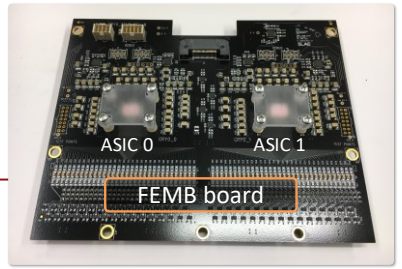




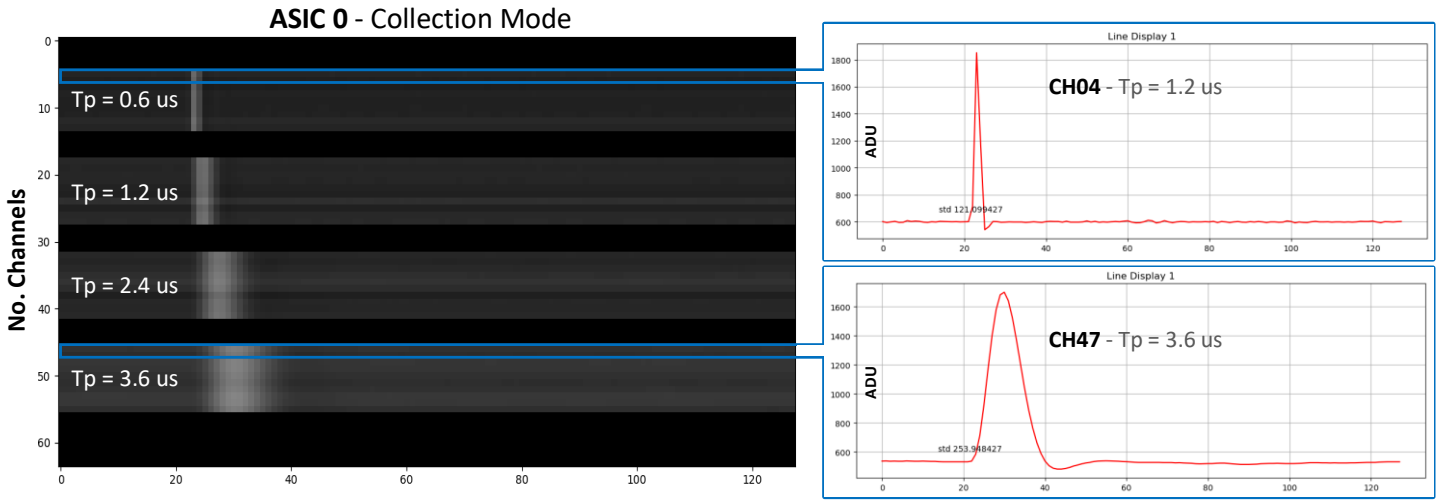




Functional verification at ~165K



Pulse response with single and dual polarity at gain 1.5X, nominal speed (2 MSPS)

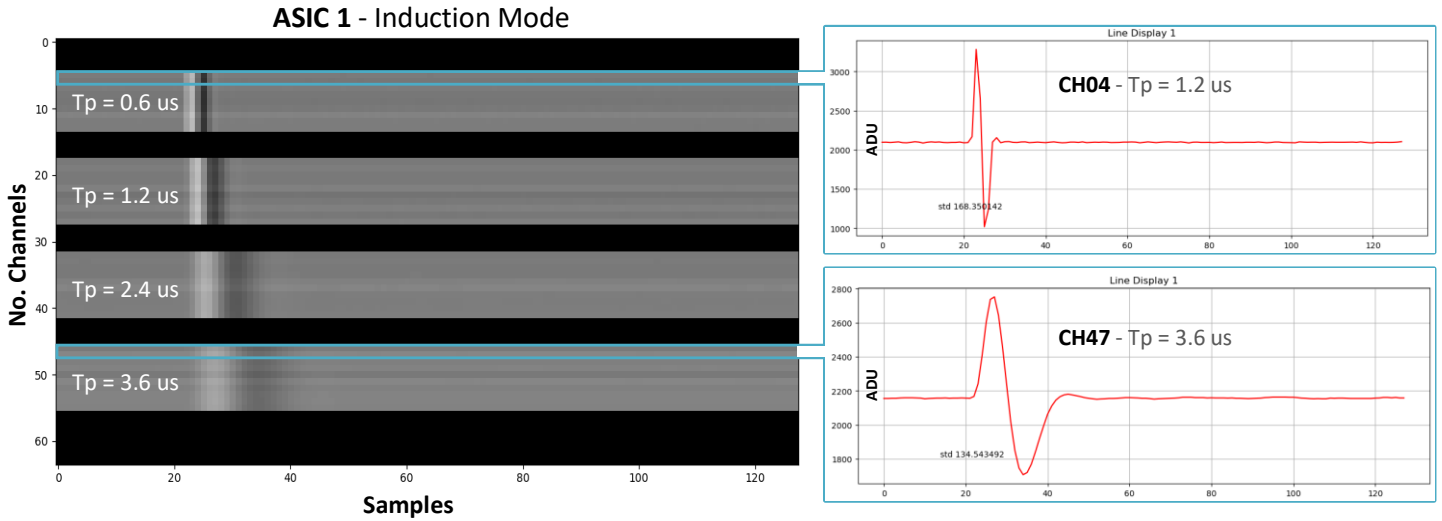


ASIC-0 | Single Polarity

- Specific groups of channels (x10) are pulsed on purpose
- Each set is configured with a different peaking time and single polarity
- Baseline reference level set to lower ADC range
- Remaining channels are masked (black areas)

ASIC-1 | Dual Polarity

- Specific groups of channels (x10) are pulsed on purpose
- Each set is configured with a different peaking time and dual polarity
- Baseline reference level set to middle ADC range
- Remaining channels are masked (black areas)

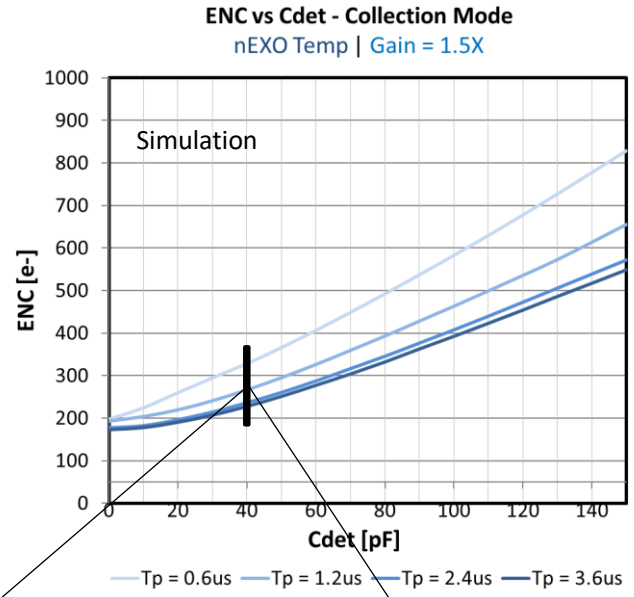


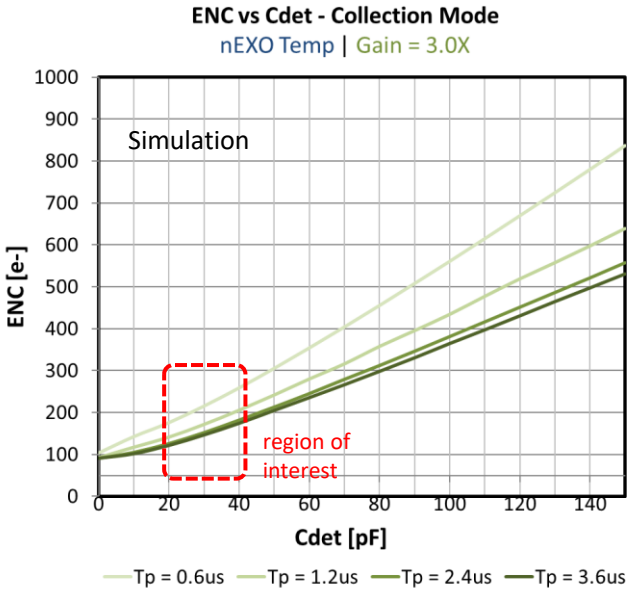
Functional verification at ~165K

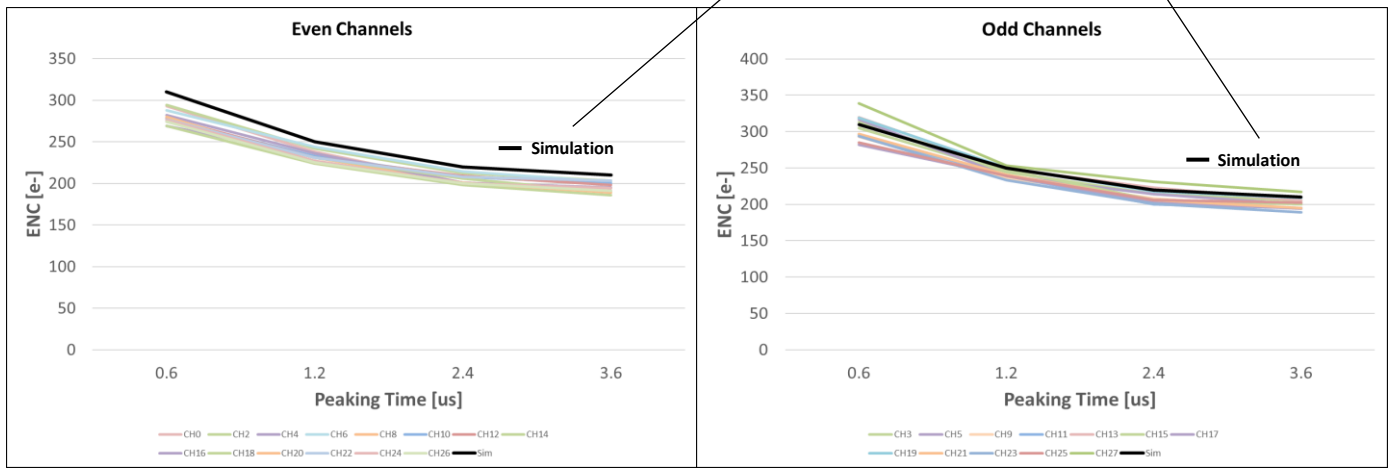
Electronic noise (ENC)

Remarks

- R&D prototype preliminary tested at ~165K
- Front-end (FE) settings:
  - Gain 1.5X in collection mode
  - Load at Cdet = 39pF
- Measured ENC shows good agreement with simulations
- Chip testing with higher gains is ongoing
  - Results will be compared to simulations

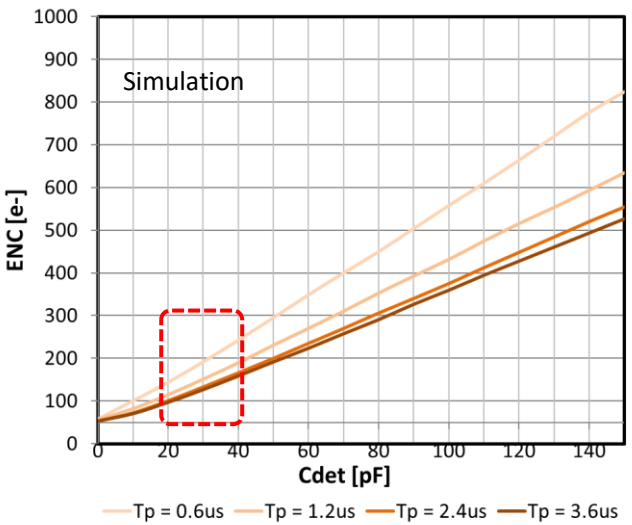






Chip testing ongoing for higher gains across system setups

Goal: ENC < 150 e-
Cdet range: 20-40pF



4

Ongoing work and conclusions

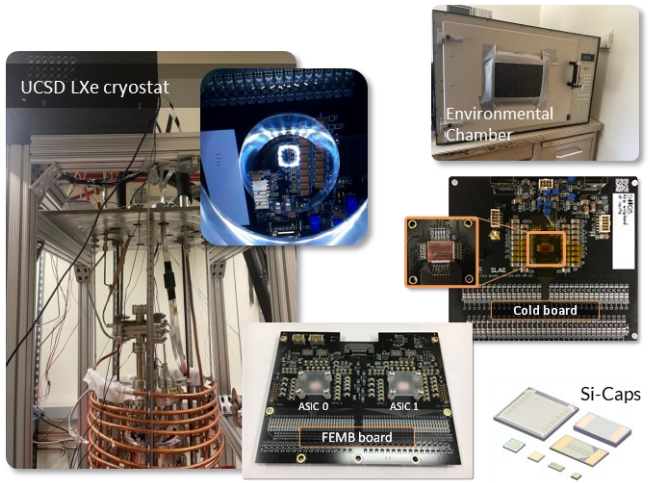
LXe setups and charge readout prototype for nEXO

Ongoing work

LXe setups and charge readout prototype for nEXO

UCSD System

- **System-1:** Cold board (single ASIC) + ePix DAQ
- **System-2:** FEMB (dual ASIC) + Commercial FPGA
- **Cryostats:** LXe capable (cooled by HFE bath) & environmental chamber
- **Goal:** ASIC performance, noise, and testing of flex cable for data communication
- Testing with Si-Caps and reduced number of external caps
- Thermal analysis (camera setup)



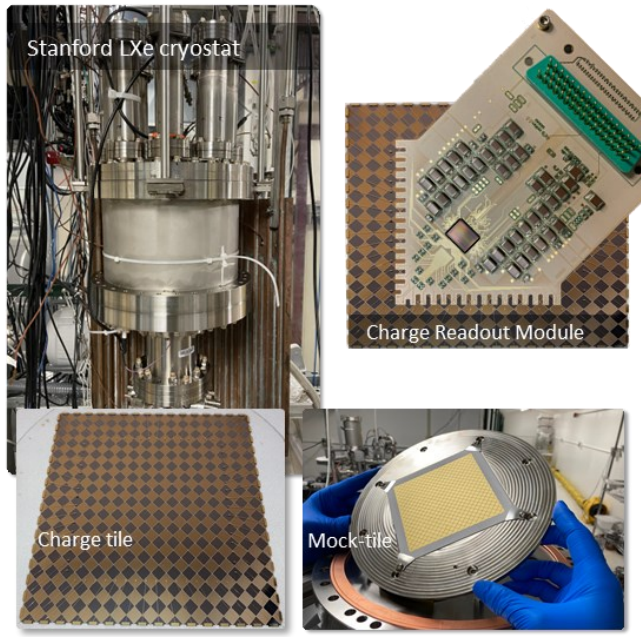
45. Testing of CRYO ASIC for the nEXO Experiment
Zepeng Li (UCSD)
11/10/23, 9:15 AM Friday
RDC1: Noble Element De... Oral
CPAD Talk

- **Demonstrated full ASIC operation at room temp and LXe environment**

Stanford System

- **System:** Charge readout (single ASIC) + ePix DAQ **(operational)**
- **Cryostat:** LXe capable (cooled by HFE bath)
- **Goal:** Measure LXe ionization with full charge readout prototype (CRYO ASIC + charge tiles)
- Capacitance measurement

47. Status and Development of nEXO's Charge Readout System
Glenn Richardson (SLAC)
11/8/23, 11:20 AM Wednesday
RDC1: Noble Element De... Oral RDC1
CPAD Talk



- **Demonstrated full ASIC operation at room temp**
- Upcoming tasks:
  - Assembly with charge tile
  - Testing in LXe

Conclusions

- **CRYO ASIC is a SoC solution** designed as the charge readout for nEXO
- Established various cryogenic systems for chip characterization (SLAC/UCSD/Stanford)
- Fully functional R&D prototype at ~165K in cold gas and LXe environments
- Mitigated several risks in the design
- Preliminary performance aligns with simulations (further testing at in progress)

References

1. S. Al Kharusi, *et. al.* (2018), nEXO Pre-Conceptual Design Report, [Online]. Available: arXiv:1805.11142

2. M. Auger, et al., JINST 7, P05010 (2012), The EXO-200 detector, part I: Detector design and construction, [Online]. Available: arxiv.org/abs/1202.2192

3. A. Pena-Perez, et al., "CRYO: A System-on-Chip for Charge Readout in the nEXO Experiment," 2022 Nuclear Science Symposium, Medical Imaging Conference and Room Temperature Semiconductor Detector Conference (NSS/MIC/RTSD'22)

4. A. Pena-Perez, et al., "CRYO: A System-On-Chip ASIC for Noble Liquid TPC Experiments," 2020 IEEE Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC'20). https://doi.org/10.1109/NSS/MIC42677.2020.9507812

5. A. Gupta, et al., "Read-Out Architecture of CRYO System-on-Chip ASIC for Noble Liquid TPC Detectors," 2020 IEEE 63rd International Midwest Symposium on Circuits and Systems (MWSCAS'20). https://doi.org/10.1109/MWSCAS48704.2020.9184452

6. ROGUE, https://github.com/slaclab/rogue.Accessedin05/05/2020

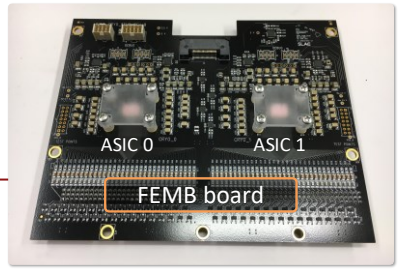
Thank you for your kind attention!

Q&A and Comments

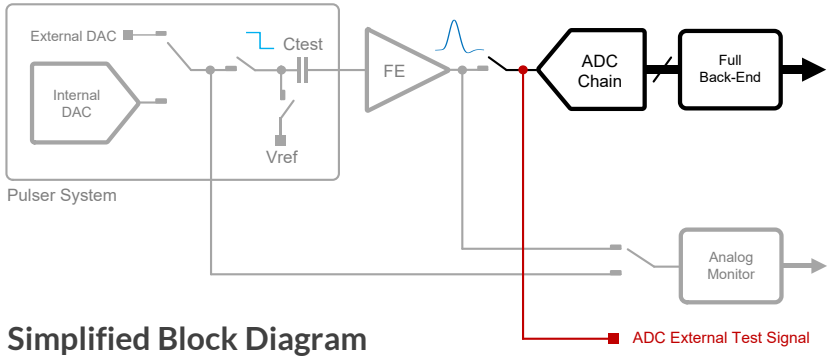
aldopp@slac.stanford.edu

BACK-UP SLIDES

Preliminary results at ~165K

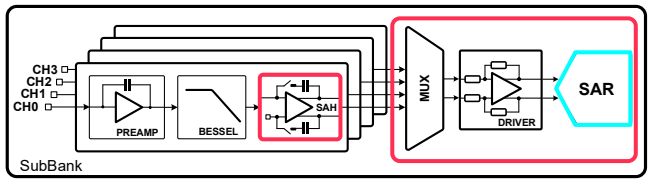


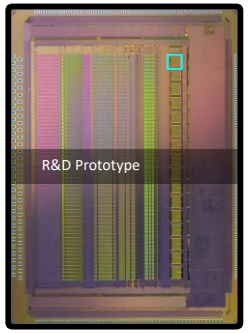
Conditions: ASIC in test mode for ADC verification, nominal speed (2MSPS)

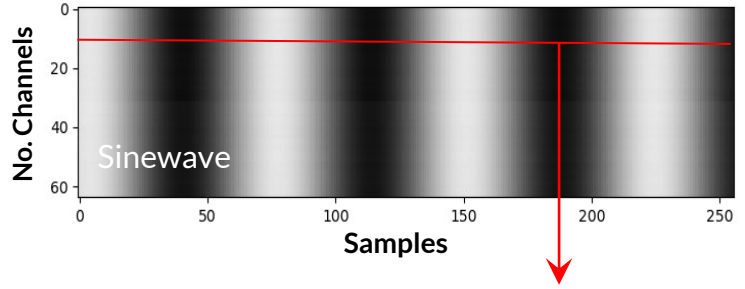


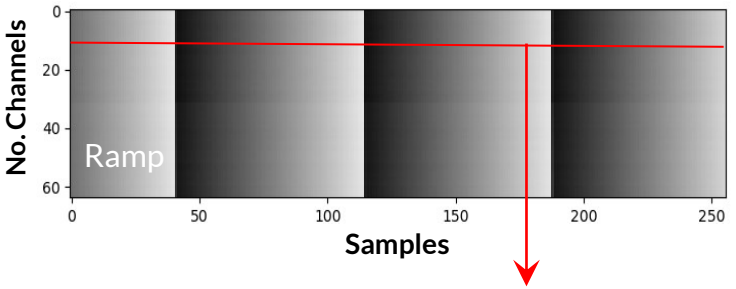
Simplified Block Diagram
CRYO in test mode (ADC section)

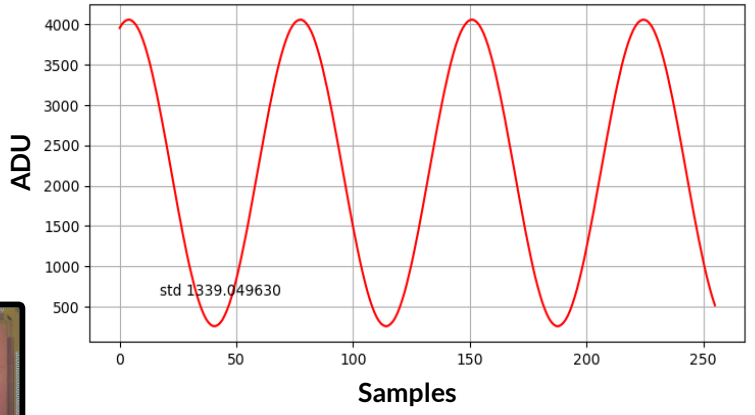
- External signal (i.e. sinewave and ramp) is applied to the ADC sections of CRYO ASIC
- **ADC section:** Sampled and hold, analog MUX, signal driver, ADC reference voltages and 12-bit SAR ADC

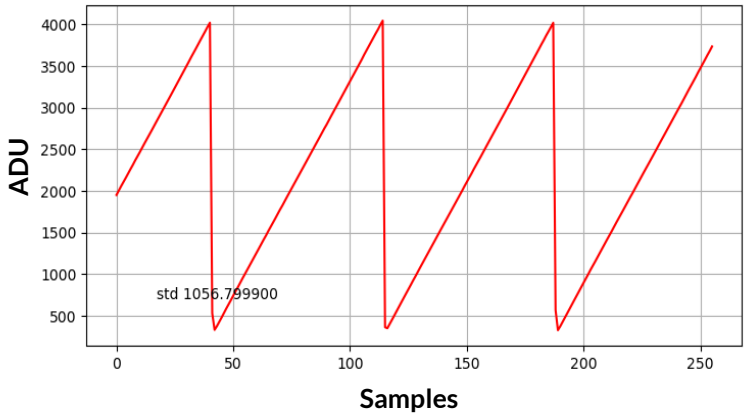








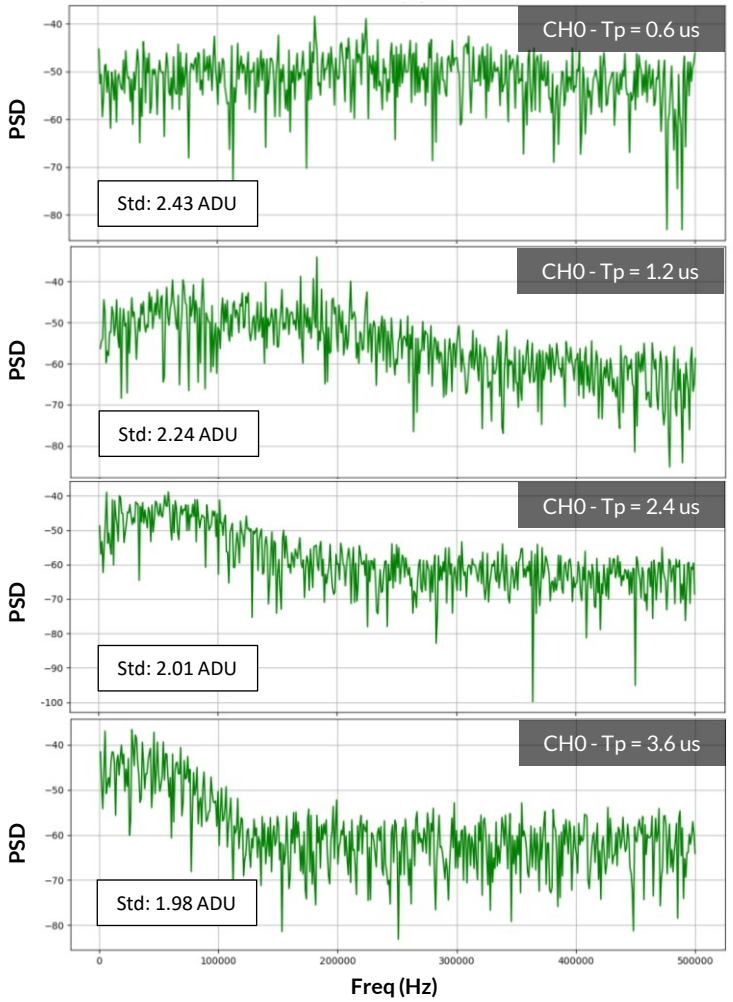




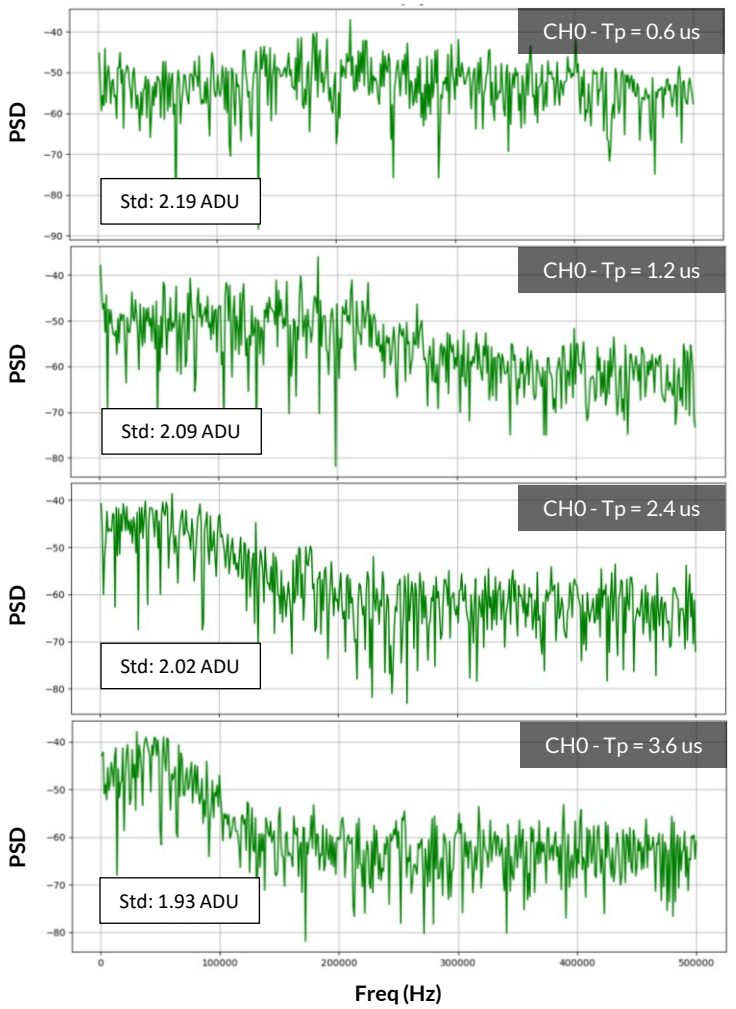
Functional verification at ~165K

Power spectral density (PSD) at gain = 1.5X, collection

ASIC-0
Single Polarity



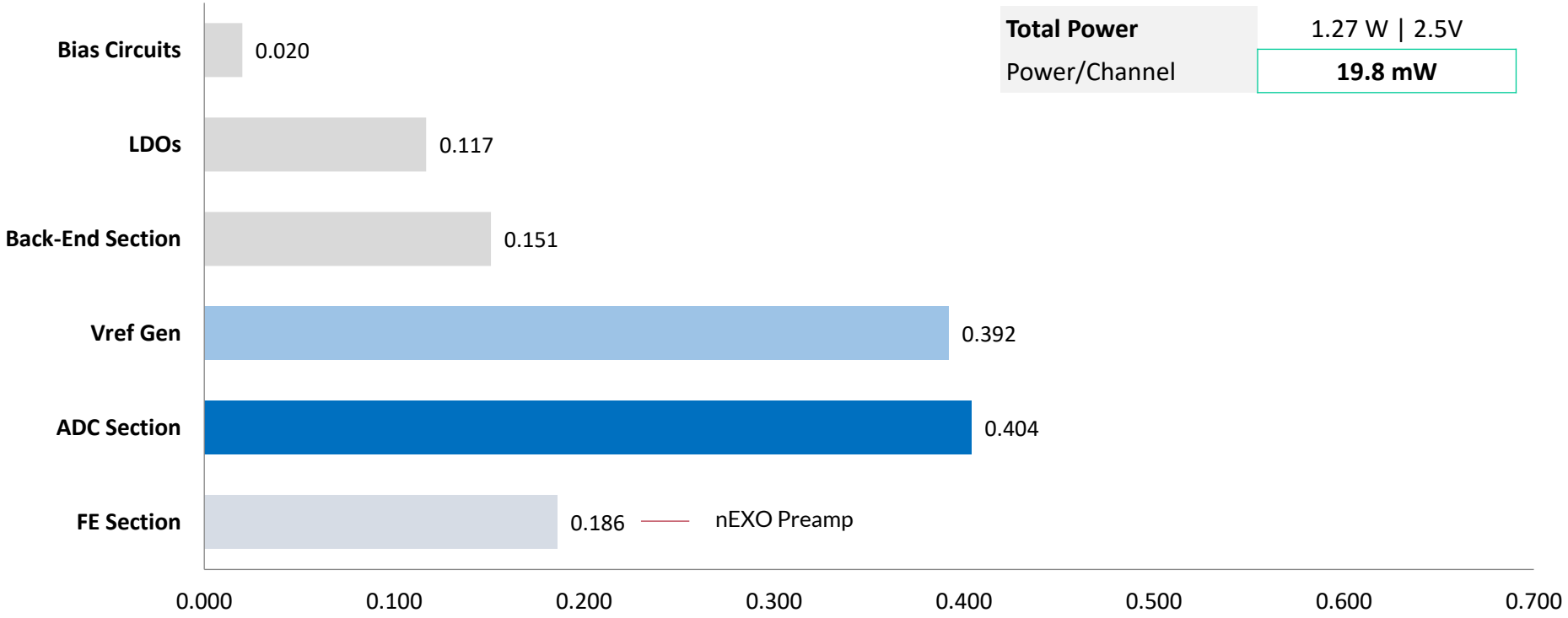
ASIC-1
Single Polarity



Note:
CH0 is shown only. Other channels shown similar response

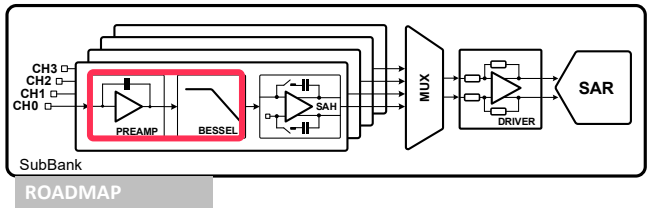
Power breakdown

CRYO ASIC R&D Prototype



Total Power	1.27 W | 2.5V
Power/Channel	**19.8 mW**

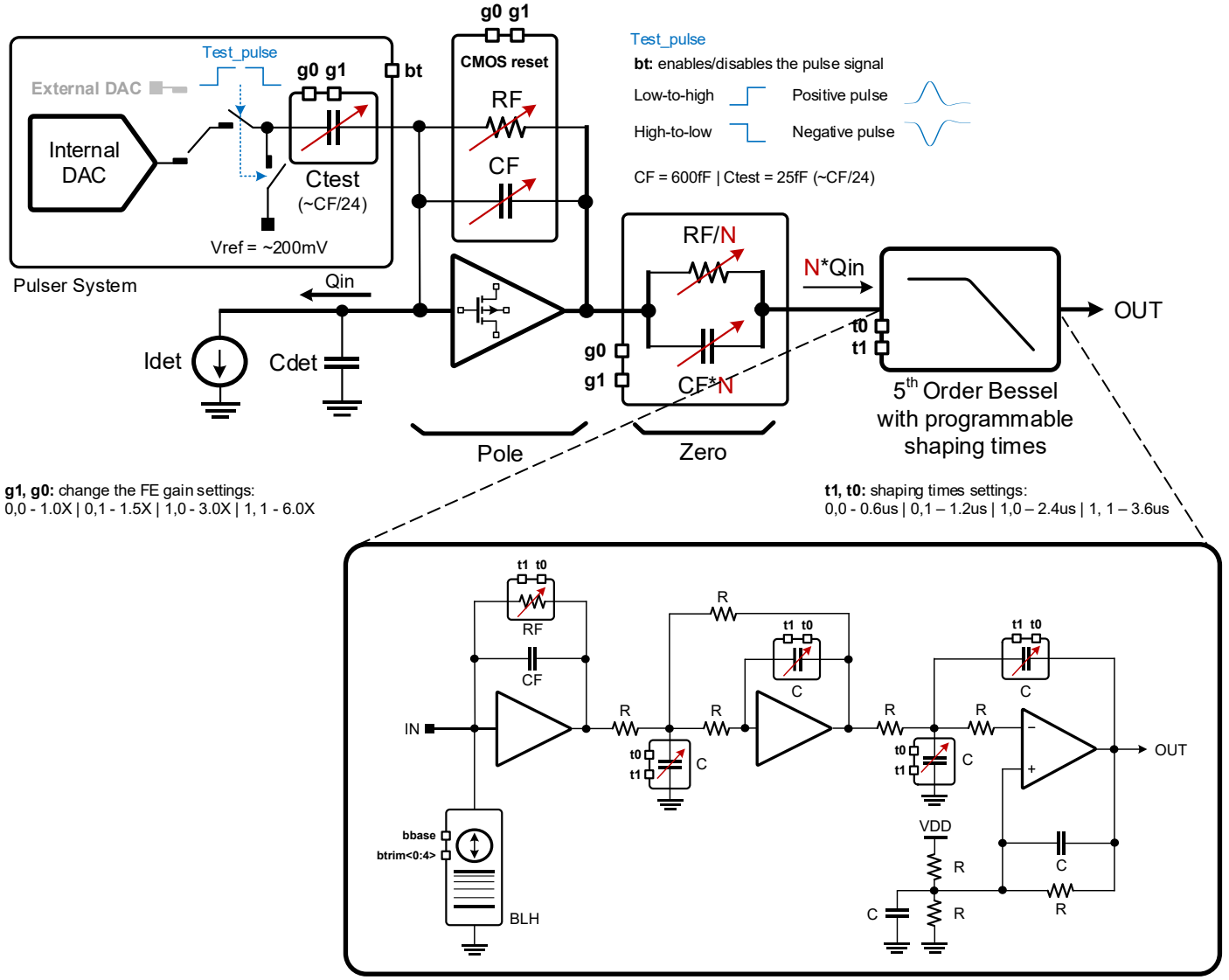
CRYO ASIC Architecture: Front-End Channel



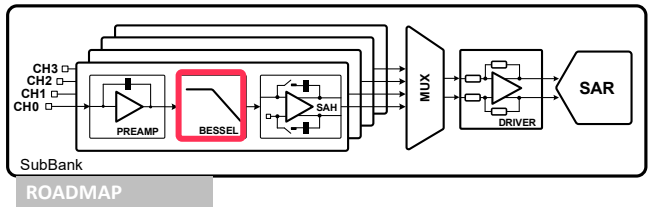
Front-End (FE) Channel

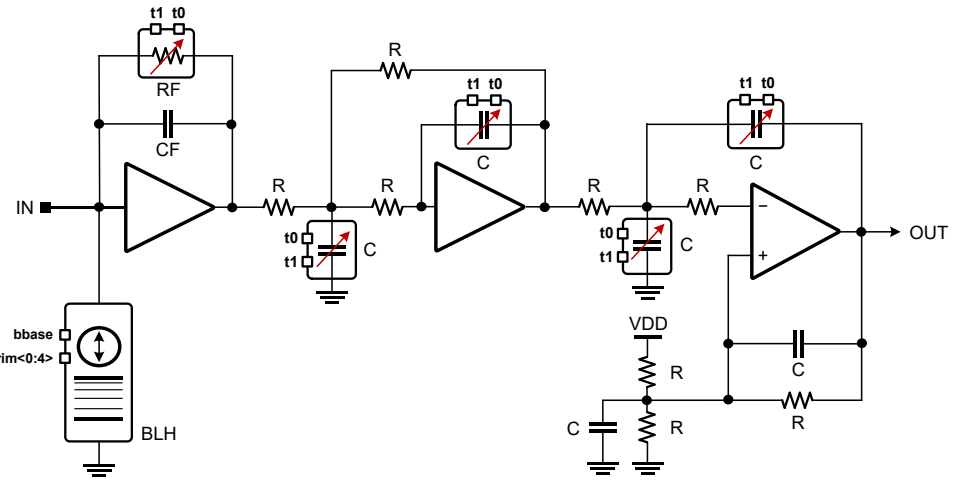
Key features

- Preamplifier with CMOS reset and pole-zero cancellation
- On-chip leakage compensation (-3.2nA ≤ Ileak ≤ 300pA)
- On-chip pulser system with programmable 10-bit DAC
- Effective linear charge amplification (N)
- 5th - Order Bessel filter
  - Avoids aliasing and optimizes SNR
  - Flat group delay (low distortion)
  - Short impulse response with no ripples
- Baseline Holder (BHL) with adjustable level (bbase, btrim)
  - Global coarse and local fine tuning
- 4 gain settings (g0 and g1) and 4 peaking times (t0 and t1)
- Highly programmable through SACI



CRYO ASIC Architecture: Bessel Filter





5th - Order Bessel

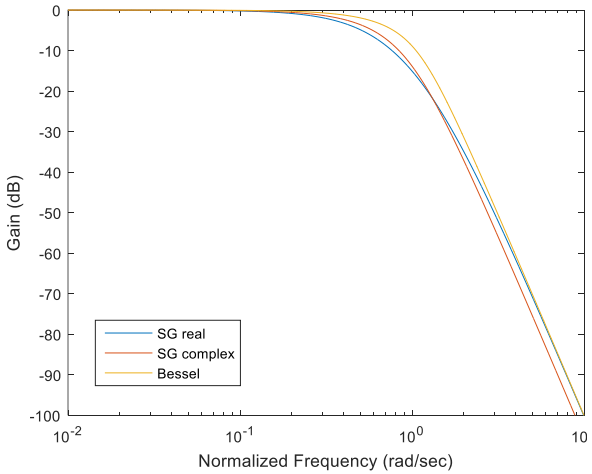
Key features

- Avoids aliasing and optimizes SNR
- Flat group delay (low distortion)
- Short impulse response with no ripples
- Programmable peaking times (t0 and t1)

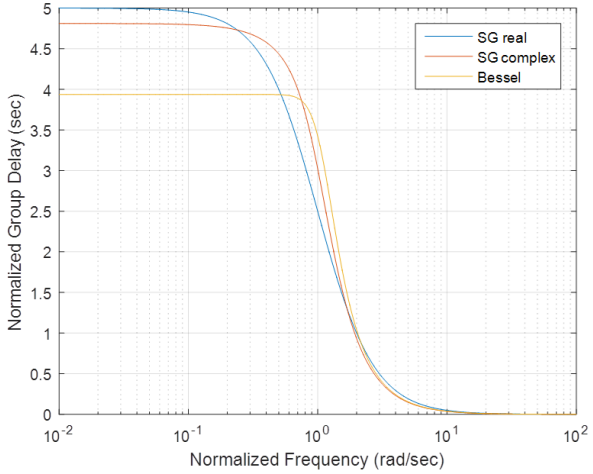
Noise Coeff.	5th Semi-Gaussian	5th Bessel
a_w	0.96	**0.98**
a_f	0.52	**0.52**
a_p	0.46	**0.43**

$$ENC^2 = (C_{in} + C_g)^2 \left[\frac{S_w}{\tau_p} a_w + A_f 2\pi a_f \right] + S_p \tau_p a_p$$

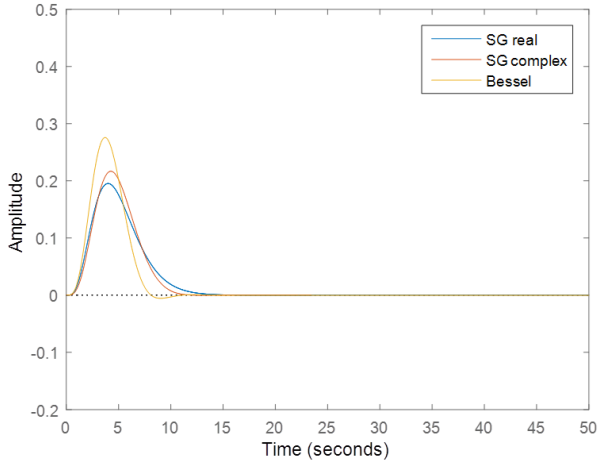
Frequency response dB



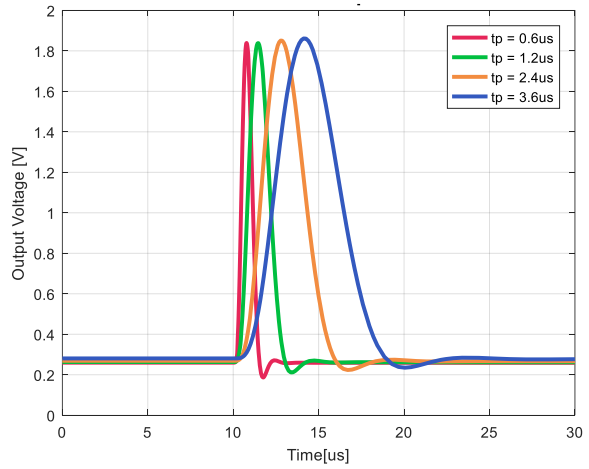
Group Delay



Impulse Response



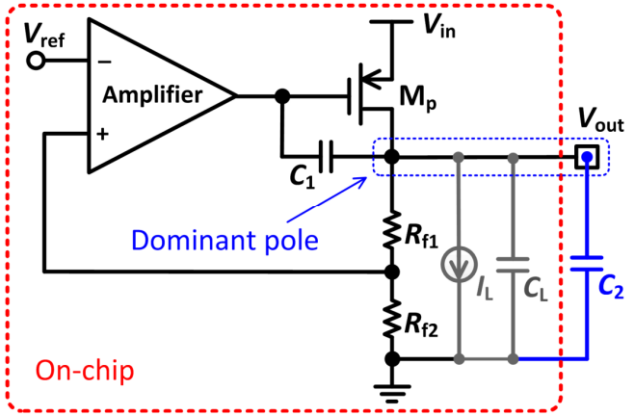
Programmable peaking time



CRYO ASIC Architecture: Low Dropout (LDO)

Conventional LDO

Externally compensated



Picture: X. Tong and K. Wei, ISVLS'2017

Simulation at ~165 K - Transient response with change in load current

Current Demand	Error [%]	Voltage drop [V]	Settling time [us]
ΔI_{LH}= 0 → 30 mA	0.8	1.003V-0.995V	6
ΔI_{HL}= 30 mA → 5 mA	0.5	1.001V-0.996V	7
ΔI_{LH}= 5 mA → 10 mA	0.1	1.000V- 0.999V	10

Simulation at ~165 K - Loop stability (LSTB) / Noise / PSRR

2.5V supply voltage | 1.0V reference voltage (Vref) | 4.7uF external capacitor

Temp	I_{Load}	RMS noise @100 KHz	PM	A_{dc} (dB)	PSRR @ 1MHz	PSRR @ 158 MHz
Room	40mA	2.70uV	> 90	30	-93 dB	-45 dB
nEXO	40mA	1.50uV	> 90	40	-93 dB	-44 dB

CRYO ASIC: Future development

Goal: Improve noise, power and radiopure

* Based on results at LXe

** Based on transition board requirements

- **Implementation of output capacitor-less LDOs**
  - Substantial reduction in I/Os, wire bonds and number of external capacitors
  - PCB design simplification → Cost savings in term of Bill of Materials (BOM)
- **Reduce the number of front-end channels from 64 to 32**
  - Compatible with nEXO charge tile
  - Benefit power dissipation distribution of front-end channels and ADCs
- **SUGOI protocol**
  - It will replace SACI communication to reduce number of I/Os
- **Additional improvements based on learnings from chip testing**
  - Based on test results from cryogenic systems at SLAC, UCSD and Stanford