Rapid Firmware/Software Development with SLAC's Open-Source Tools: SURF, RUCKUS, and ROGUE

Ryan Herbst For SLAC TID Instrumentation

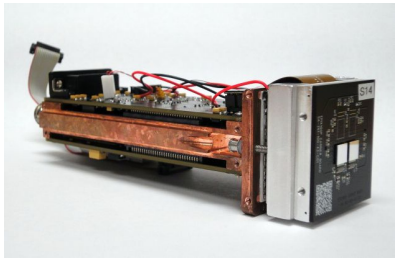
November 9, 2023

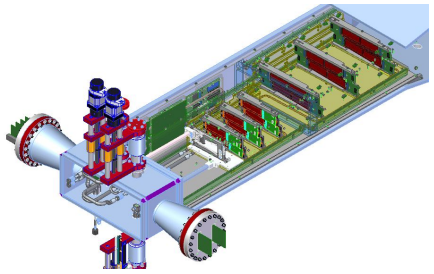
SLAC NATIONAL ACCELERATOR LABORATORY

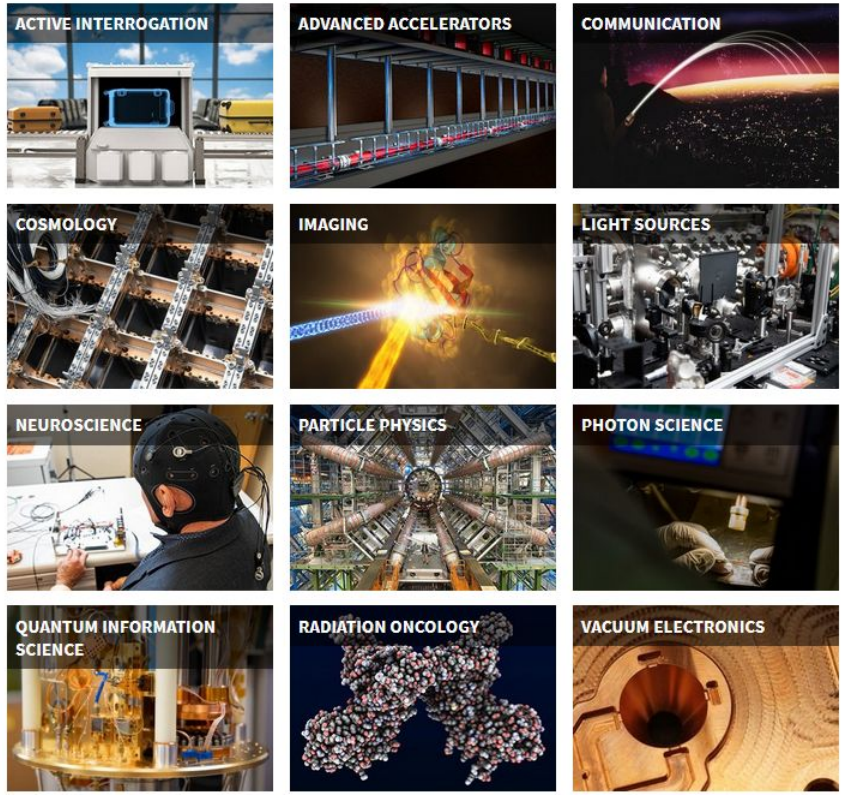
Stanford University | U.S. DEPARTMENT OF ENERGY

Who We Are And What We Do

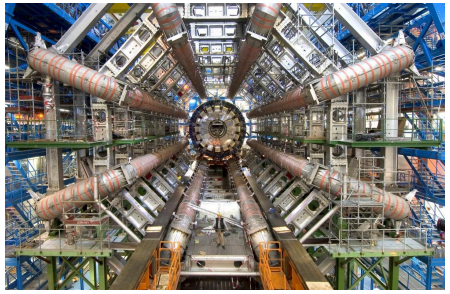
- TID-ID has broad expertise in detector and instrument creation:
  - Sensor design and fabrication
  - Integrated circuit design
  - Micro packaging and interconnects
  - Advanced analog & digital electronics
  - High-performance, high-density FPGA design
  - RF DSP processing in FPGAs
  - Large-scale system integration
  - Low-latency AI inference in FPGAs
  - High-rate data collection & processing
  - Firmware defined radio
  - QIS materials research





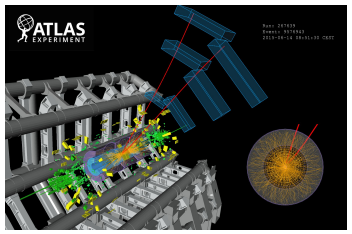


- Develop Instrumentation & Data Acquisition (DAQ) electronics for a wide range of science experiments:
  - HEP: ATLAS, CDMS, ProtoDUNE, HPS
  - Photon Science: LCLS/LCLS-II X-Ray Cameras
  - Others: LSST, CMB, LCLS-II beamline controls

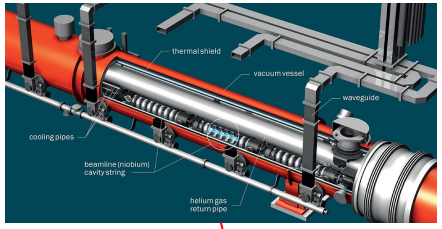


Identifying Cross Application Synergies
Leveraging Building Blocks To Enhance Science

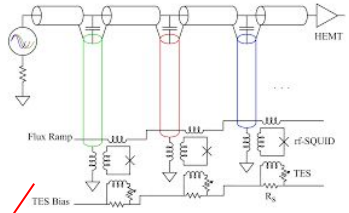
BaBar Data Processing Challenges



ATLAS Muon SubSystem Readout Challenges

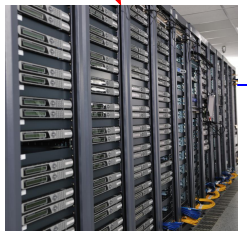


LCLS2 1Mhz Accelerator Controls & Instrumentation Challenges

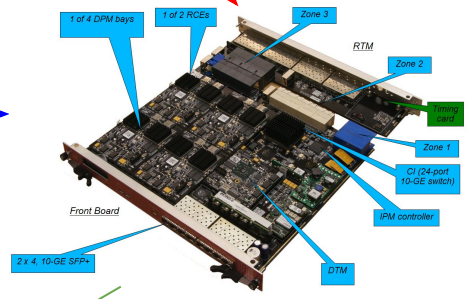


RF Multiplexing For SQUIDS Challenges

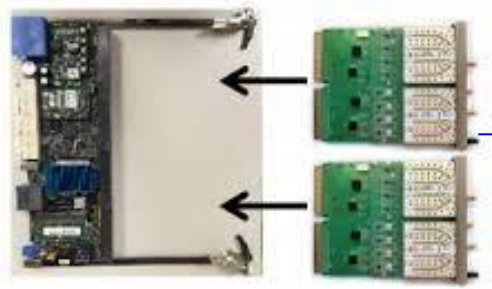
Challenge



PetaCache R&D Effort



RCE Platform R&D (ATCA, Digital)

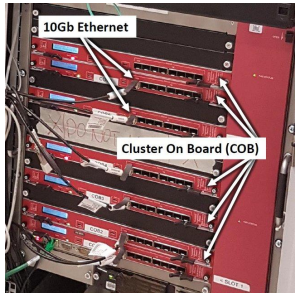


Common Controls Platform R&D (ATCA, Analog)

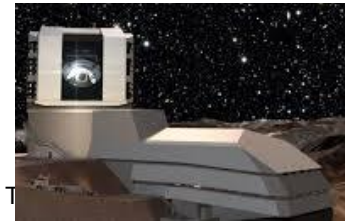
Microwave Multiplex Readout R&D (SMURF, SO, CMBS4)

Next Generation RFSOC Based DAQ/Analog Platform TBD!

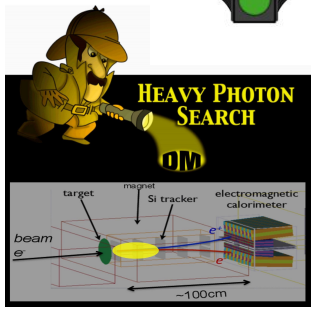
Technology



Introduction Of First ATCA System T
ATLAS For Muon Sub-system
(possibly first ATCA @ CERN)

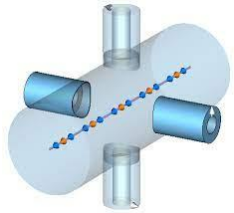


LSST / RUBIN DAQ System

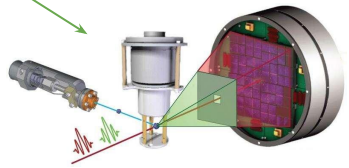


HPS DAQ

LCLS2 Machine Protection (MPS)



LCLS2 / FACET Instrumentation
Beam Position Monitors (BPM)
Beam Length Monitor (BLEN)
Bunch Charge Monitor (BCM)



LLCS2 1Mhz Timing, Precision Timing & Laser Lockers

Low Level RF (LLRF) For FACET, LCLS, C3, etc

Simons Observatory
(opened the door to CMBS4)

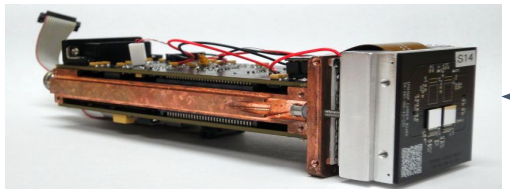
Application

SLAC TECHNOLOGY INNOVATION DIRECTORATE

SLAC TID-ID Is Committed To Open Source Libraries

- Reliable UDP (RUDP) Network offload engine to support network attached devices (NAT)
- High bandwidth synchronous (timing & trigger delivery) & asynchronous fiber protocols for front end readout (PGP2,PGP4)
- SLAC Ultimate RTL Framework (SURF):
  - Open source VHDL/Verilog framework for rapid FPGA/ASIC development using common generic, extensible libraries
  - Ruckus: Open source build system
- Open source DMA engine & associated driver for high bandwidth & high rate DMA transfer
  - Works both in amd64 & Zynq (SOC + RFSOC) platforms
  - Zero copy user space buffer mapping
  - Direct to GPU data transfer support
- Rogue: Open source Python/C++ hardware abstraction software for rapid readout development & test stand support
  - Easily integrated into back end DAQ systems
  - Balanced python (ease of use) and C++ (high bandwidth & high event rate) implementation

https://github.com/slaclab/surf
https://github.com/slaclab/ruckus
https://github.com/slaclab/rogue



Rogue

DAQ Core

Linux Kernel
aes-stream-drivers

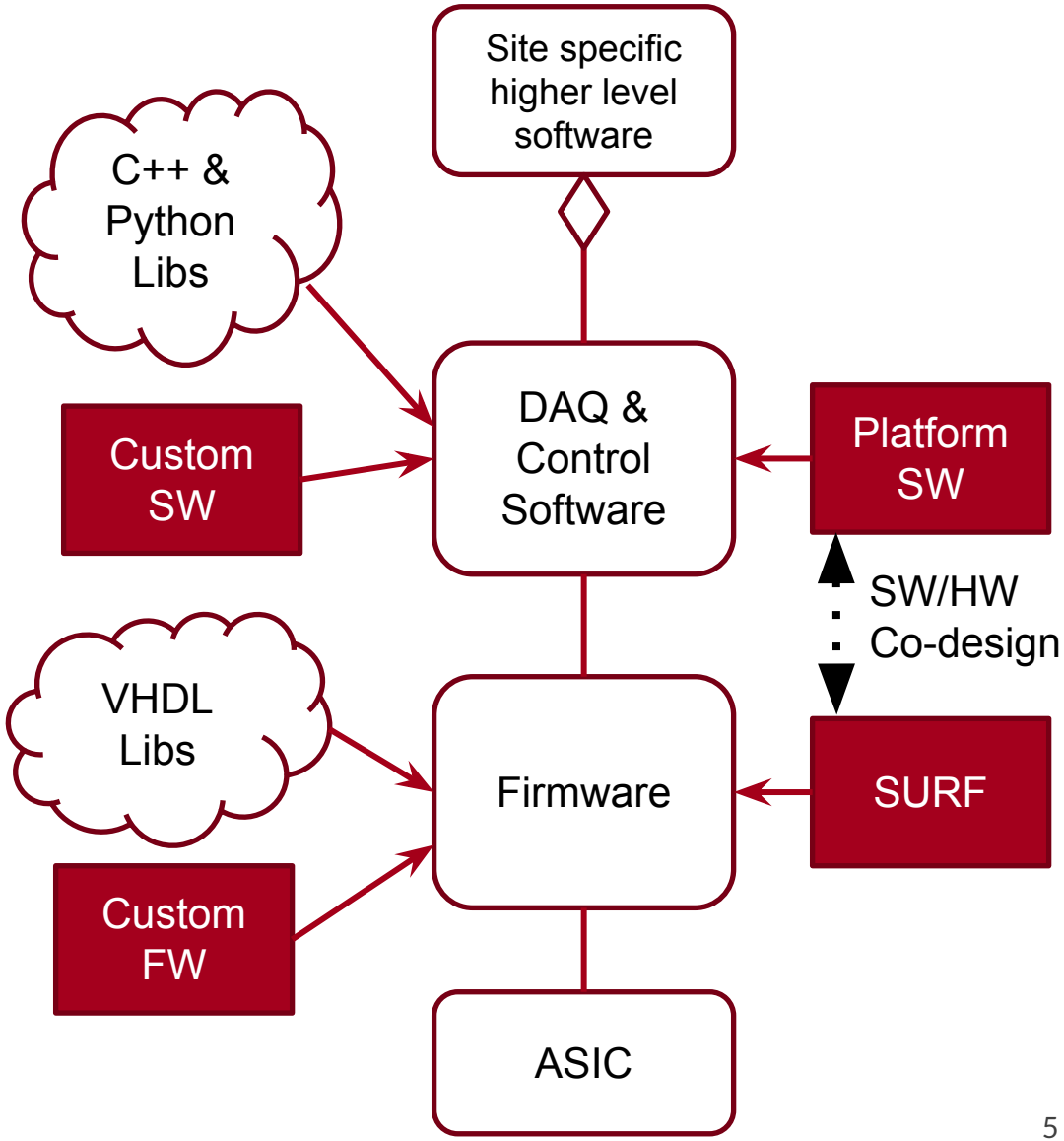
Linux Kernel
GPU Drivers

Direct to GPU DMA support in open source DMA Engine & Driver

SLAC TECHNOLOGY INNOVATION DIRECTORATE

Maximize Firmware / Software Reuse With Common Building Blocks With Standard Interconnects

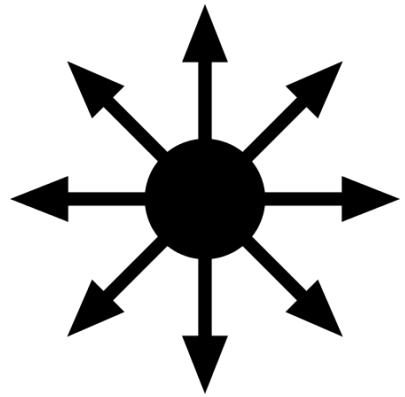
- Platform Software
  - Python/C++ framework to deploy custom readout systems
  - Enables register level and stream communication
  - Enables local control & back end DAQ integration
- SURF (SLAC Ultimate RTL Framework)
  - VHDL firmware library
  - Contains a library of protocols, device access and commonly used modules
- Software and Firmware are tightly integrated providing firmware/software parallel development
  - Application firmware in HLS (High-Level Synthesis), Model Composer, etc



SLAC Ultimate RTL Framework (SURF) Firmware

- https://github.com/slaclab/surf
- **HUGE** VHDL library for FPGA development
- Used in **Xilinx** FPGAs, **Intel** FPGAs and **ASIC** digital designs
- VHDL-based IPs for commonly implemented modules
  - **Ethernet** Library: (IPv4, ARP, DHCP, ICMP, UDP)
  - **AXI4** Library: (Crossbar, DMA, FIFO, etc.)
  - **AXI4-Lite** Library: (Crossbar, AXI4-to-AXI4-Lite bridge, etc.)
  - **AXI4 stream** Library: (DMA, MUX, FIFO, etc)
  - Device Library: (ADI, Micron, SiliconLabs, TI, etc.)
  - **Synchronization** Library: (Synchronize bits, buses, vectors, resets, etc)
  - Wrapped Xilinx Library: (clock managers, SEM, DNA, IPROG)
  - **Serial Protocols** Library: (I2C, SPI, UART, line-code, JESD204B, etc)
- New features and bug fixes on a weekly basis

Ruckus: RTL Build System



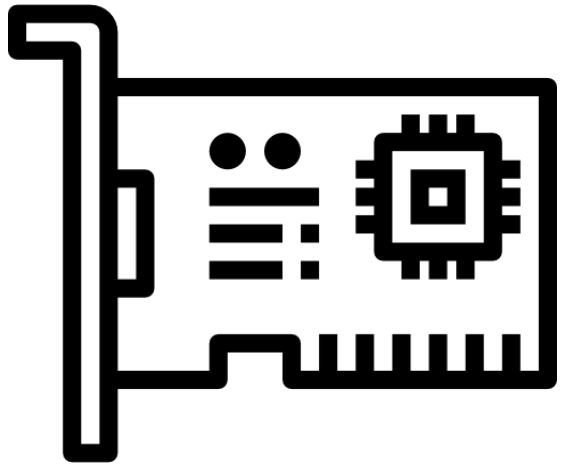
- https://github.com/slaclab/ruckus
- Open source, “Ruckus” is not an acronym
- **Compliments** the SURF/Rogue libraries
- Hybrid Makefile/TCL system
- **Integrates the git repo into the RTL build**
  - Provides the git hash at time of build as a readable register
  - Scripts to help with tag releasing and release note generation
- TCL helper function to help with add code
- Supports the following IDEs:
  - Vivado (AMD/Xilinx FPGAs)
  - Synopsys DC compiler (Digital ASICs)
  - Cadence Genus (Digital ASICs)
  - Fabulous (eFPGA)
- Able to reproduce the project's initial state with a “**make clean; make**”

Rogue Software

- https://github.com/slaclab/rogue, https://slaclab.github.io/rogue/
- Software tools for both rapid prototyping and experiment deployment
- “Rogue” is not an acronym
- Operates either in a **python/C++ hybrid** or **C++ only** mode
  - Higher level python for connecting the high performance C++ modules together
- x86-64, ARM32 and ARM64 support
- Able to run on **Linux, MAC or windows**
  - Windows and MAC requires use of released or custom docker containers
- **Lots of ways to run the rogue software**
  - 100% C++ only code
  - python script (non-GUI)
  - EPICS
  - Python GUI (e.g. PyQT, PyDM, etc)
- Actively maintained

PCIe FW/SW Framework

- https://github.com/slaclab/axi-pcie-core (Firmware/Software)
- https://github.com/slaclab/aes-stream-drivers (Linux Kernel Driver)
- Firmware framework for BAR0 **AXI-Lite** interface with **up to 8 DMA lanes**
  - 256 TDEST per DMA lane (up to 2048 destinations total)
- Provide a “common platform” firmware frame and software kernel driver for any Xilinx PCIe card
  - Common **Xilinx Dev board** support
    - AC701, KC705, KCU105, KCU116, VCU128
  - Common **Xilinx Data Center Card** support
    - U50, U55C, U200, U250, U280, C1100
  - Much more card support can be added as needed
- Demonstrate up to **113 Gb/s for large frames** (PCIe GEN3 x 16, 1MB frames)
- Demonstrate **> 1MHz frame rate for small frame** (<128B) without frame batching
- Support for direct data transfer to GPU or other commercial processors



Zynq Ultrascale+ FW/SW Framework

- https://github.com/slaclab/axi-soc-ultra-plus-core (Firmware/Software)
- https://github.com/slaclab/aes-stream-drivers (Linux Kernel Driver)
- Firmware framework for **AXI-Lite interface** with up to **8 DMA lanes**
  - 256 TDEST per DMA lane (up to 2048 destinations total)
- Provide a “common platform” firmware frame and software kernel driver for any Zynq Ultrascale+
  - Common **Xilinx Dev board** support
    - KV260 (non-RFSoC)
    - ZCU111 (RFSoC GEN1)
    - ZCU208 (RFSoC GEN3)
    - ZCU216 (RFSoC GEN3)
    - ZCU670 (RFSoC DFE)
    - RealDigital RFSoC4x2 (RFSoC GEN3)
  - Much more Zynq Ultrascale+ board support can be added as needed
- **Inspired** by the work done on **axi-pcie-core**
- Managed and maintained by TID-ID Electronics Systems Department

Future Libraries For Open Source

- SLAC Neural Network Library (SNL)
  - Talk by A. Dave in Tuesday RDC5 session
  - Currently opening up to interested collaborators
  - Interested in ways to integrated into HLS4ML

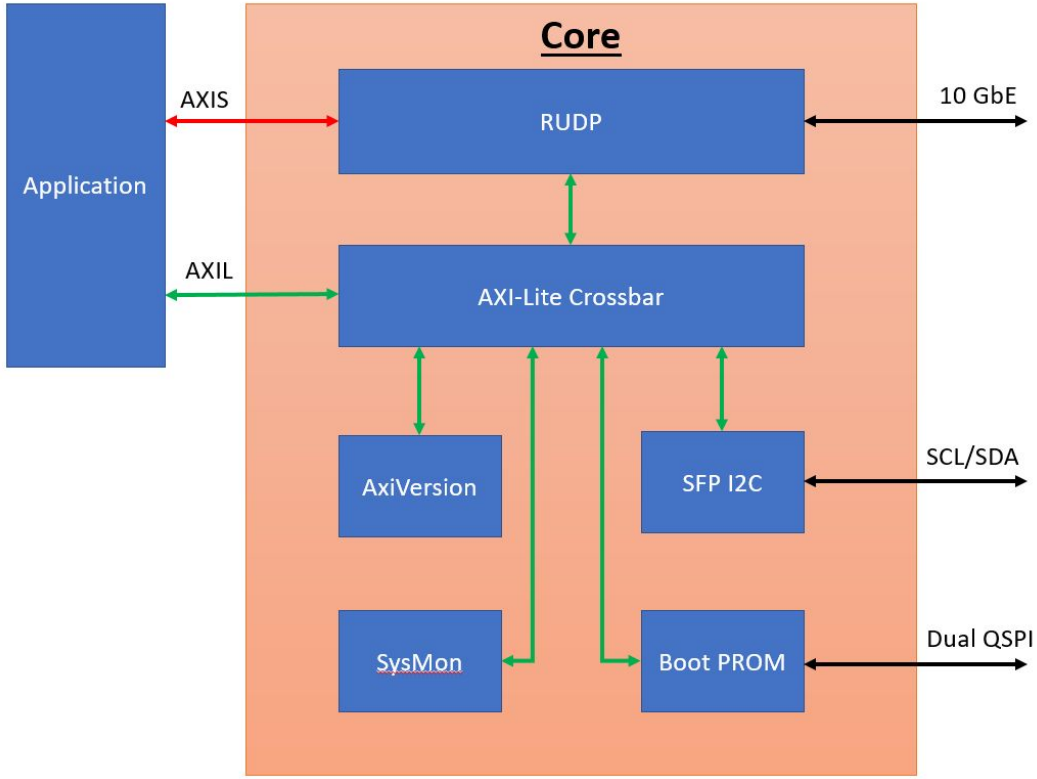
- RFSOC based RF processing libraries
  - Based upon work done for SMURF, AXION, Q-Bit readout, LLRF etc
  - Still cleaning up library structures
  - Potential for collaboration with QICK platform

Current Known External Collaborators And Customers

- CMS Muon Detector Team
  - CERN, Princeton, University of Minnesota Twin Cities, Notre Dame, U. Virginia
- SparkPix-RT digital ASIC
  - ANL
- Altiroc 1 Development
  - CERN
  - Annuaire IN2P3
- Cosylab
  - Medical device applications
- Belle-2 & general KEK
  - University of Hawaii
- Other SPP partners
- Other silent users

Getting Started: Development Board Example

- Question: How can I get started?
  - Answer: We provide a **working example** that someone can **copy and modified**
- https://github.com/slaclab/Simple-10GbE-RUDP-KCU105-Example
- https://slaclab.github.io/Simple-10GbE-RUDP-KCU105-Example/



IEEE Real Time Conference: SURF Workshop/Tutorial

- 24th IEEE Real Time Conference
  - ICISE, Quy Nhon, Vietnam
  - April 22-26, 2024
  - https://indico.cern.ch/event/940112/
- Abstract submissions are now open.
  - **Deadline: 2 Dec 2023, 11:59**
- Pre-Conference Program: 4 workshop/tutorials will be held
  - Cocotb
  - **SURF**
  - FABulous eFPGAs
  - Open-source ASIC Design (Skywater, Caravel)