Scalable SNSPD Cryogenic Readout

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Coordinating Panel for Advanced Detectors (CPAD) Workshop - November 2023

DOE Microelectronics Codesign: "Hybrid Cryogenic Detector Architectures for Sensing and Edge Computing enabled by new Fabrication Processes" (HYDRA)

Two complementary cryogenic state-of-the-art single-photon and particle detectors:

- the **Skipper CCD-in-CMOS** silicon detector (Skipper CCD-in-CMOS CPAD Talk)

- a **hybrid detector platform based on superconducting nanowires**

Development and co-design of:

- advanced **fabrication and integration techniques**

- novel optimized **hybrid readout architectures**

- cryo-ASICs and cryotron-based superconducting electronics for **integrated sensing** and data reduction at source, through **feature extraction** and **edge computing**.
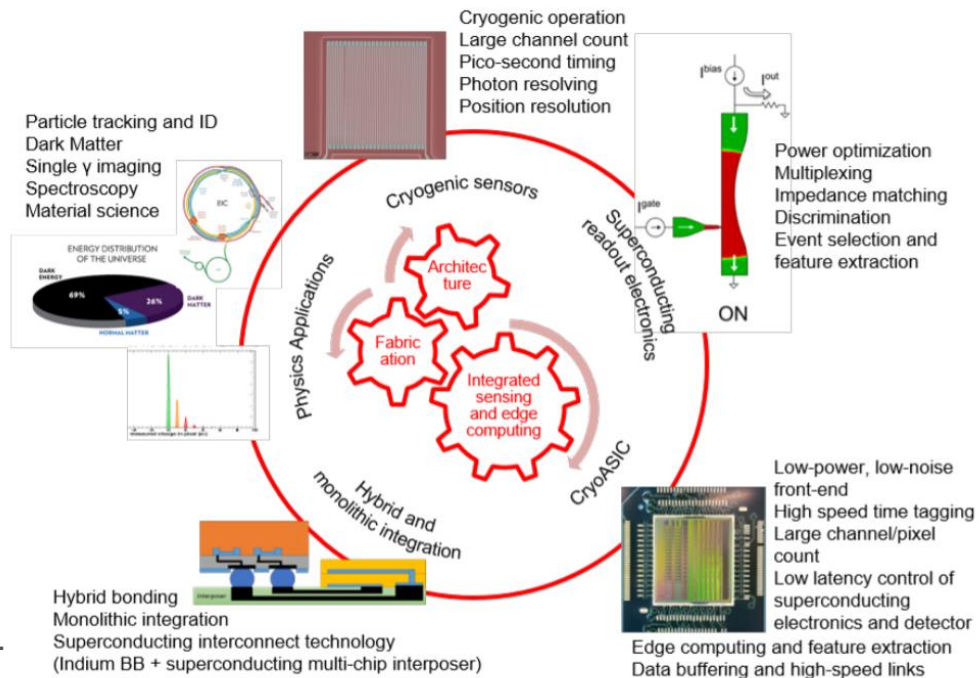
PDK-compatible 4K models for 22nm FDSOI

Fermilab is working with **Synopsys** to develop PDK-compatible (BSIM-IMG) isothermal models at 4K with **Mystic** (advanced **compact model** parameter extraction tool for **SPICE** models)

- Currently working on thin and thick oxide cmos
- HV devices next
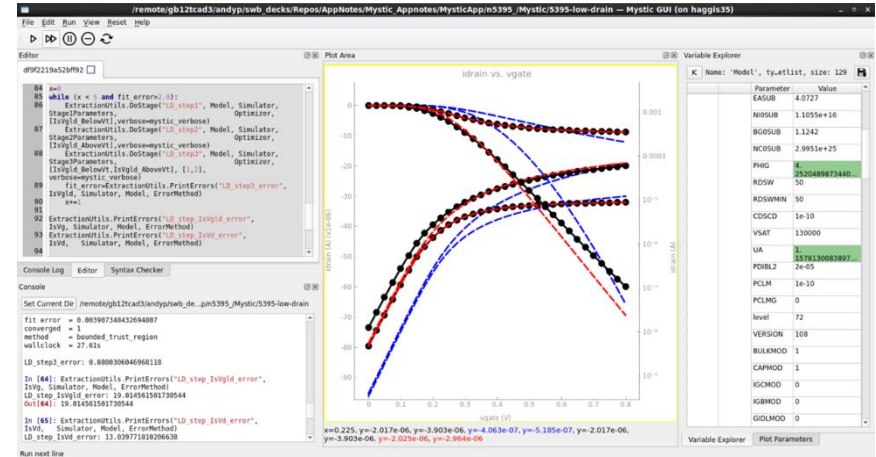
O.Seidel CPAD Talk:
CryoCMOS modelling and PDK development for GF 22 FDX

measurement data
foundry model
fitted model
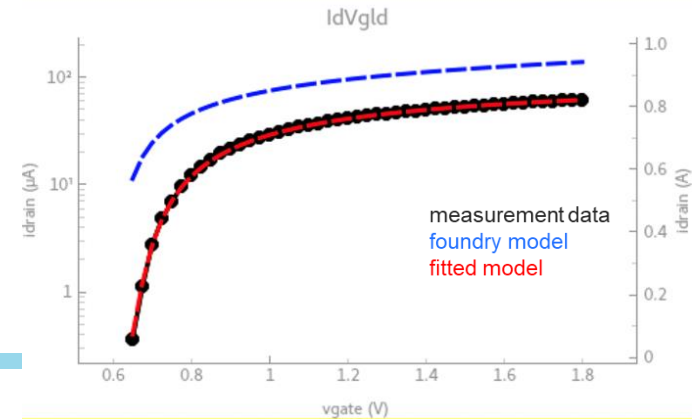
Superconducting Nanowires Detectors

LHC/TOTEM Roman pots

As PHOTON DETECTORS:

- Highest performing detectors available for time-correlated single photon counting from the deep UV to the mid-infrared
- Demonstrated detection efficiencies as high as 98% at 1550 nm
- Timing jitter below 3 ps
- Effectively zero dark count rates
- Intrinsic photon number resolution
- Maximum count rates exceeding 1 Gcps in arrays

Exploited for photon detection (classical and quantum optics and communication)

As PARTICLE DETECTORS:

- Can have high segmentation (~10um "pixels")
- Can be truly edgeless detector (important for beam monitoring)
- Operation in high magnetic field (5T)
- Radiation hardness to be investigated at Fermilab test beam facility

Unique capabilities for far-forward detectors that operate close to the beam (high T, high radiation, high segmentation)
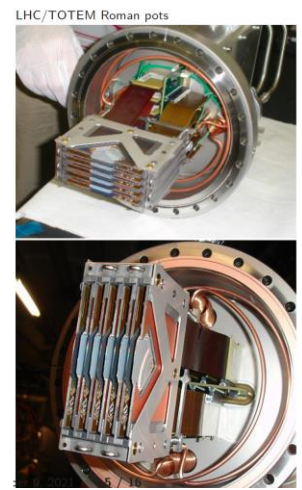
W.Armstrong and S.Lee CPAD talk
Novel Applications of Superconducting Nanowire Detectors in Nuclear Physics

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SNSPD + nanocryotron + cryoASIC detector

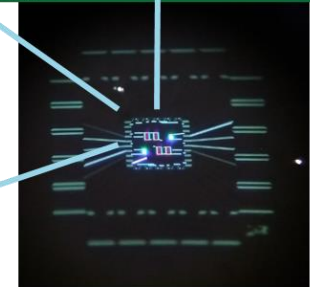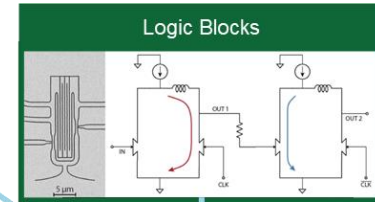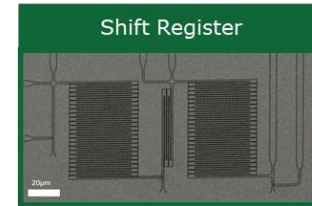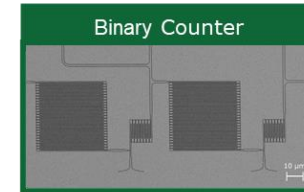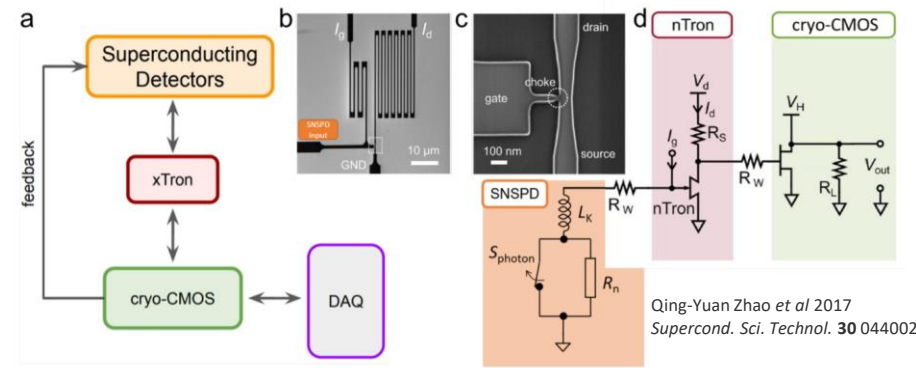Heterogeneous architecture based on the co-design of:
1. SNSPD sensor (ANL)
2. edge nanocryotron-based superconducting electronics (MIT)
3. cryoCMOS ASIC (FNAL)
4. Cryogenic interposer and scalable interconnect scheme (JPL)
5. PDK-compatible cryogenic models (FNAL, Synopsys, EPFL)

Nanowire cryotron (nTron) circuit architectures are used to interface superconducting circuits with cryogenic CMOS and perform counting, shifting, and standard logic functions for edge processing.

The cryoCMOS ASIC provides timestamping and complex signal processing and readout

Goal: scalable, large count detector with edge computing and integrated sensing

The goal of the first ASIC prototype is to provide a versatile and high-performance cryogenic readout solution ahead of a second optimized version.

Qing-Yuan Zhao *et al* 2017
Supercond. Sci. Technol. **30** 044002

Logic Blocks

Binary Counter

Shift Register

SUNROCK

(Superconducting Nanowire Readout Chip - v1)

- 32 channels, each including amplification + biasing + termination + discriminator + fast time tagging

- Suitable for both SNSPD (internal gain) or nanocryotron (external gain) readout

- High performance on-chip PLL

- Additional DAC biasing channels for global biasing

- 22nm CMOS, operation at 4K

- Tape out in Dec 2024, chips expected from fabrication in March 2024

Readout and Biasing

- Programable load
  resistor   (In progress)

- Programmable current DAC to bias
  sensors

- Clocked bias
  current   (In progress)

- Signal Amplification from 1mV pulse
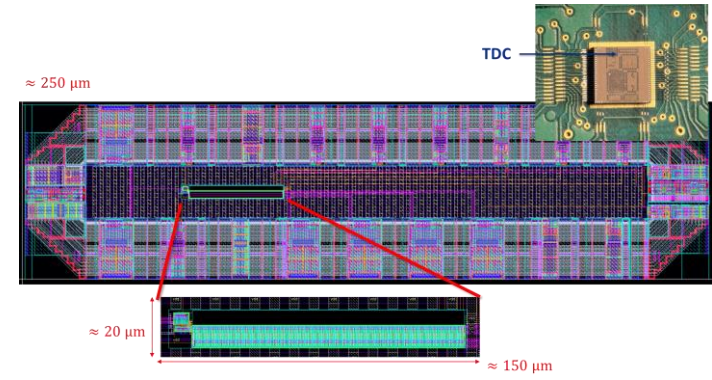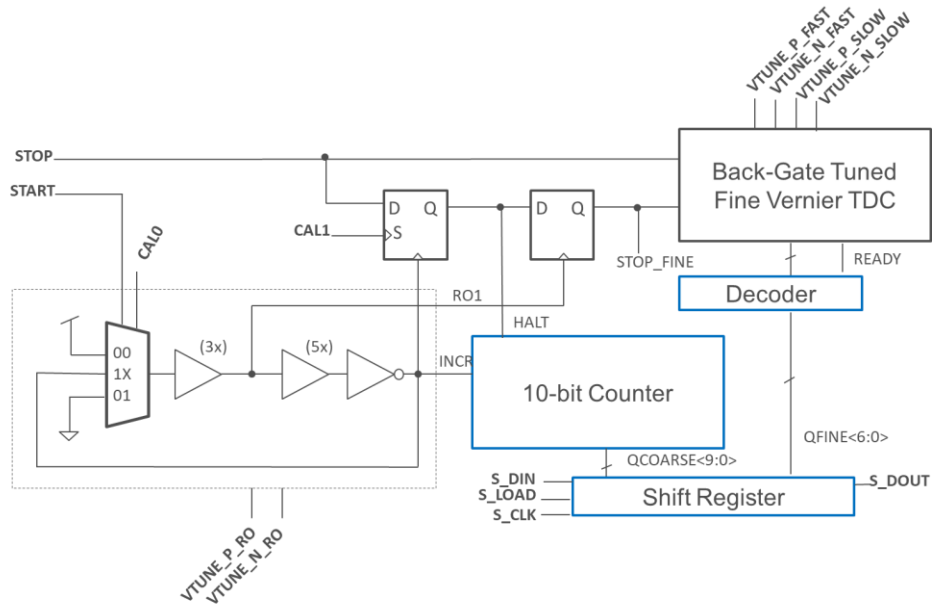 to Rail-Rail signal
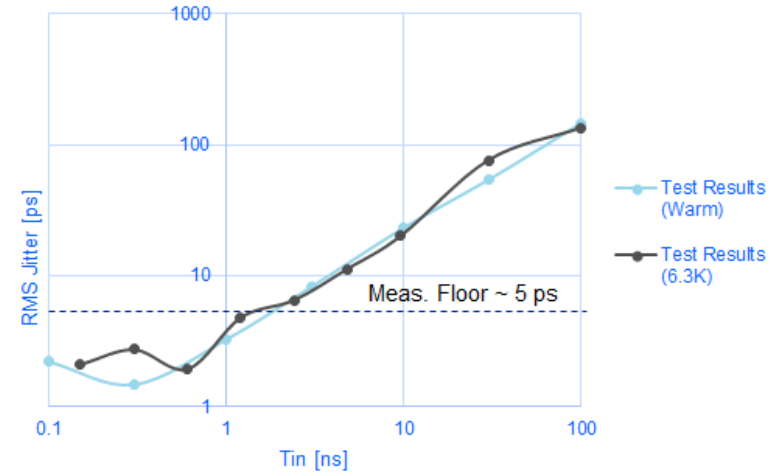
- TDC measurement

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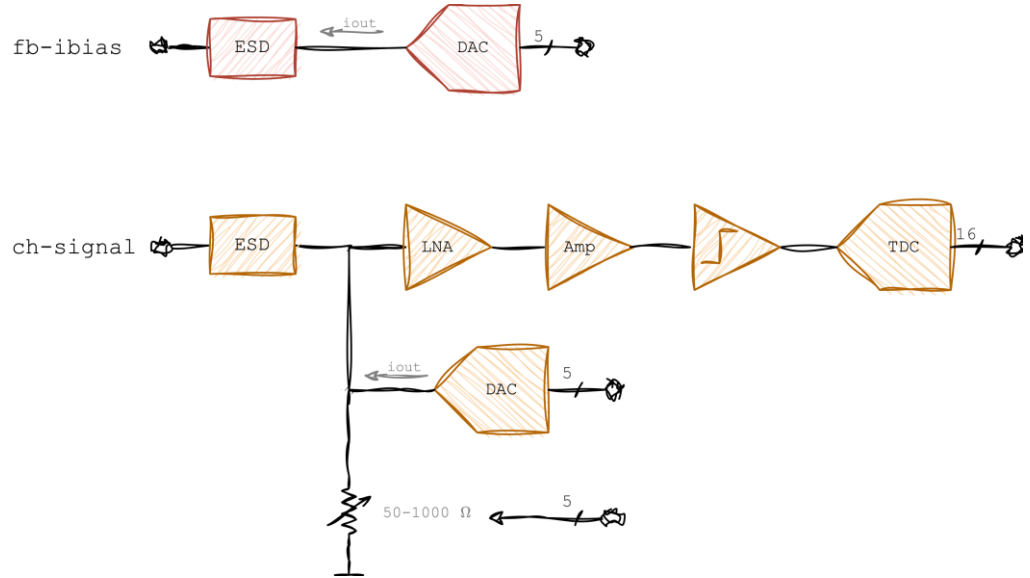
Readout and Biasing Specs

Name		Target		Actual		Comment
Channel Input Resistance	max	1000	Ω	–	Ω	Programmable input resistance for each channel.
	min	50	Ω	–	Ω	
Channel Output Current Magnitude	max	100.0	uA	100.0	uA	Programmable output current for each channel. The LSB tracks reference current, so min/max/lsb can be scaled with the alternative reference values: 250nA, 500nA, 1uA, 2uA, etc.
	min	10.0	uA	10.0	uA	
	lsb	1.0	uA	1.0	uA	
	dnl	0.1		0.1		
Channel Timing Error	rms	~15.0	ps	–	ps	Total RMS timing error.
Amplification Jitter	rms	10.00	ps	–	ps	Timing error from the amplification.
TDC Accuracy	lsb	5.00	ps	–	ps	Timing error from the TDC measurement.
High-Speed Clock Distribution	rms	5.00	ps	–	ps	Timing error from the TDC measurement.

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"DILVERT" TDC test structure (Nov 2021)


Speed is tuned by FDSOI back-gate biasing
- Low complexity, small footprint, no noise contribution from bias circuits

6 separate tuning voltages:
- Fine TDC fast chain, slow chain, and coarse TDC ring oscillator
- Tune NMOS and PMOS separately.
- Both 0~2V w.r.t VSS

~300 µW at 100MHz (power scales roughly linearly with rate)


Jitter [rms ps] vs Input Time [ns]

Updated TDC

- Delay line uses both PMOS and NMOS backgate bias voltages to control delay. (A common bias is shared across all channels)

- When an event is detected (Comparator output), the delay line is triggered, a sample signal is sent to the aggregator to sample the high speed clock index.

- When delay line is done, the circuit will self reset and prepare for next measurement.

- Logic is implement using digital flow.

  - Delay line is hand placed custom digital

  - Delay line sample flops are hand placed custom digital

  - Delay done signal is hand placed custom digital to leverage useful skew

  - Retiming registers on delay done allow for multicycle path through combinational therm-to-bin decoder.

  - 1.0GHz clock leverages inferred clock gating wherever possible.

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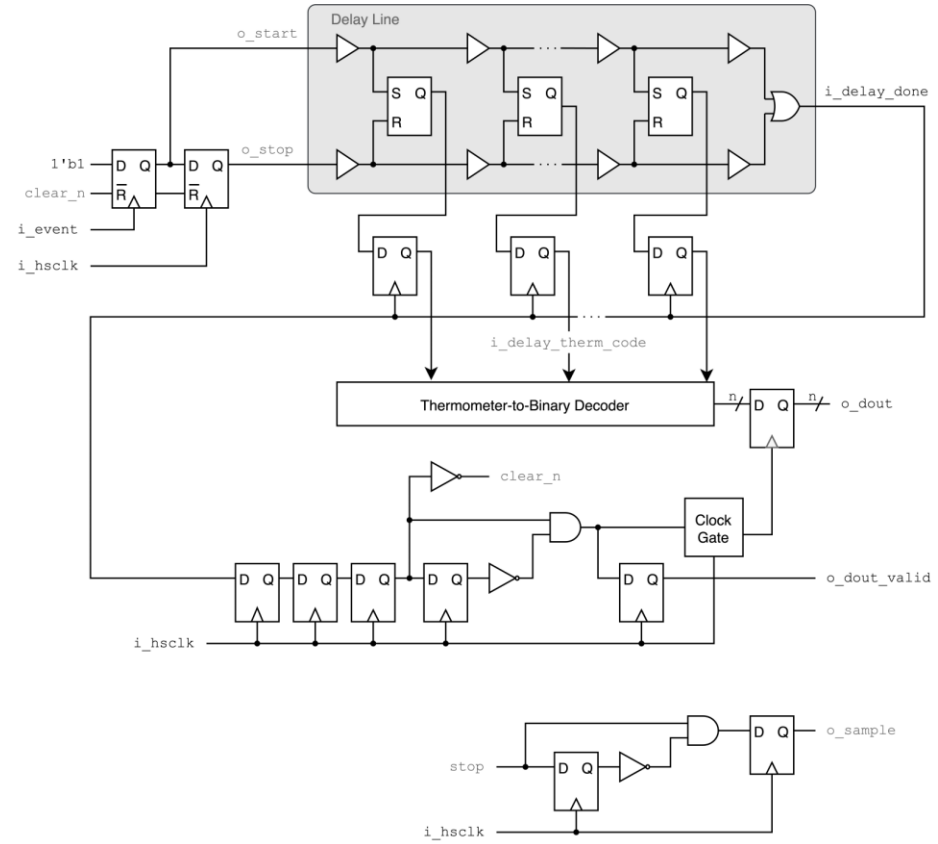
Architecture

- Readout channels perform timing measurements on input event.

- Bias Channels provide extra current biasing capabilities.

- TDC Aggregator receives channel TDC measurements and generates counter index.

- Readout subsystem streams the channel data into the serial output.

- The programming interface provides access to the control and status registers (~5 kb memory)

- The PLL provides a high quality 1.0 GHz clock. (PLL operates at 10.0 GHz)

- Clock Controller muxes system clock between PLL output and the reference clock. Also provides programmable binary divider for debug/test.

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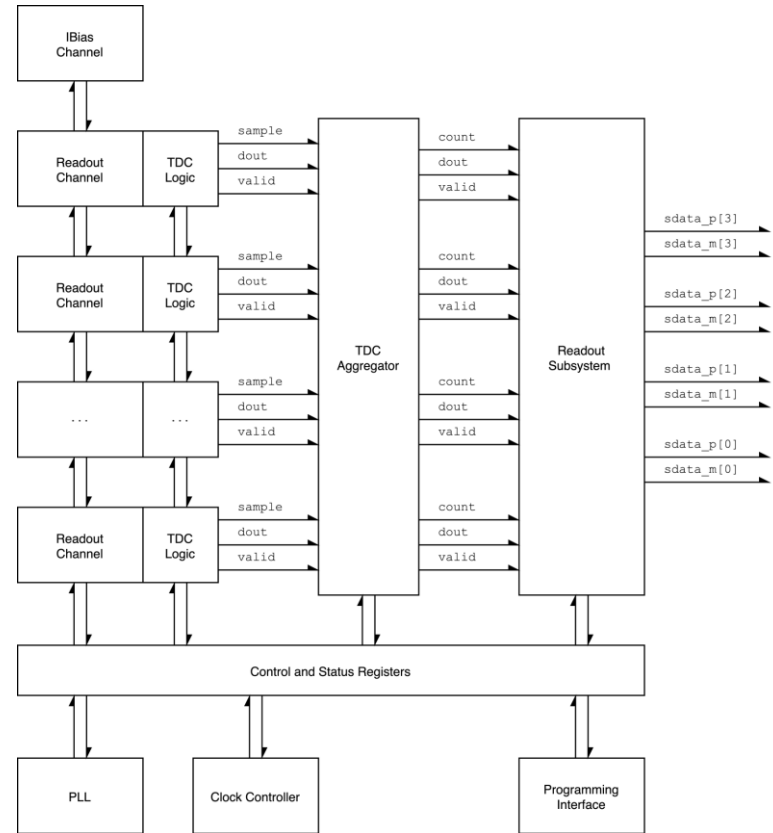
Readout Subsystem - Sequencer

- FSM organizes the output serial data stream.

- The FSM first initializes the preamble generator to build the preamble and mux it directly to the serializer.

- Next the FSM cycles between the Header and Channel Generators to produce the channel packet information.

- The channel priority logic is embedded in the FSM so that it can simultaneously control both the output and channel selection muxes.

- Generator outputs are loaded into multi-stage FIFOs and ready/valid handshakes are used to both transition states and packetize data for serializer

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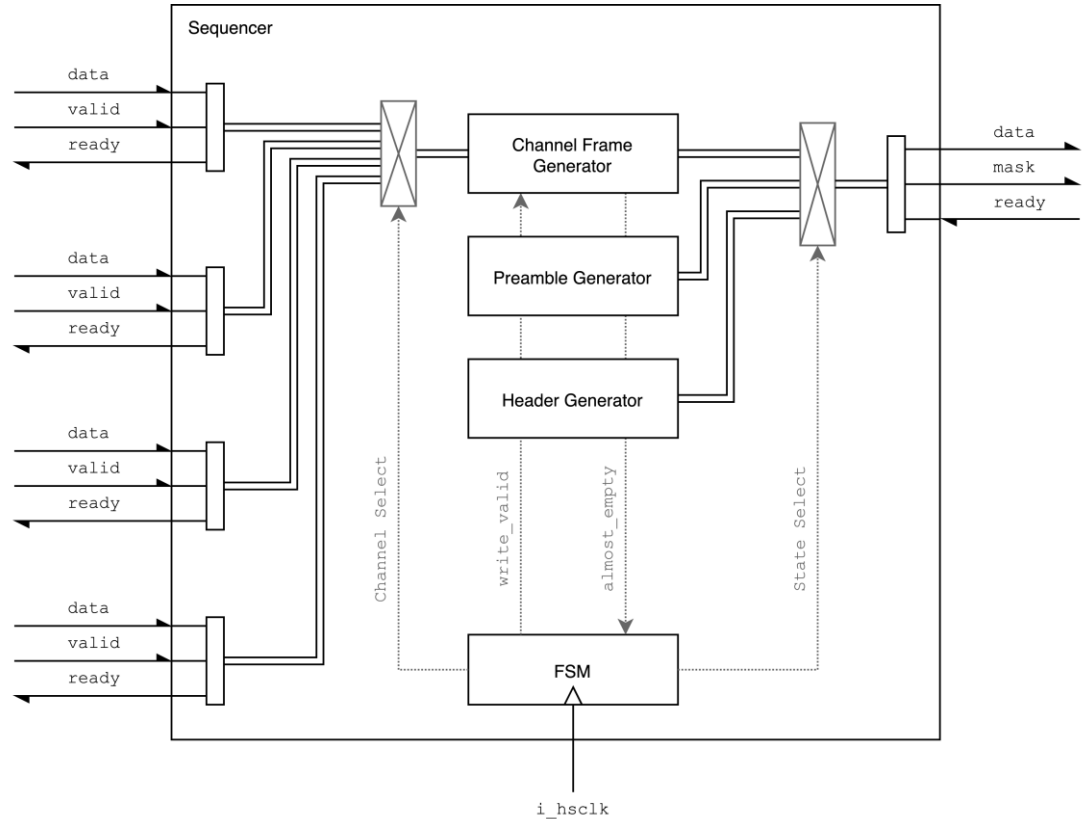
Serial Output

- Readout subsystem provides two data streaming formats

  - Fixed Priority

  - Dynamic Priority

- Programmable preamble duration

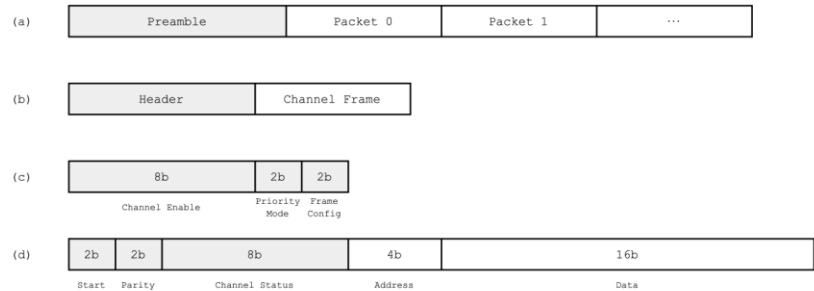- Programmable packet header information

- Programmable channel data information

Fixed Priority Serial Format

(a)	Preamble	Packet 0	Packet 1	...

(b)	Header	Channel N-1	...	Channel 1	Channel 0

(c)	8b	2b	2b
	Channel Enables	Priority Mode	Frame Config

(d)	2b	2b	8b	4b	16b
	Start	Parity	Channel Status	Address	Data
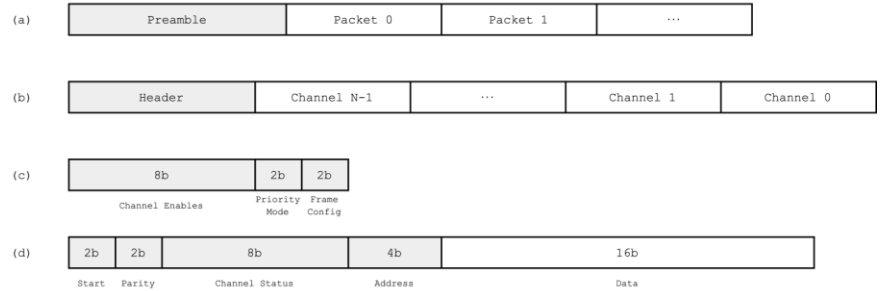
** Reconfigurable Fields in Gray

Dynamic Priority Serial Format

(a)	Preamble	Packet 0	Packet 1	...

(b)	Header	Channel Frame

(c)	8b	2b	2b
	Channel Enable	Priority Mode	Frame Config

(d)	2b	2b	8b	4b	16b
	Start	Parity	Channel Status	Address	Data

** Reconfigurable Fields in Gray

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Summary and Outlook

SUNROCK will provide our collaborators with a first multichannel cryogenic readout solution with time-tagging for SNSPD readout.

The next version will focus on substantial power reduction through:
- Data-driven readout
- Efficient serializers and transmitters
- Optimized cryomodels

Given the rapid adoption of SNSPDs, other programs and applications can benefit and adopt a cryogenic readout ASIC

See C.Pena CPAD talk:
Towards Low Energy Threshold and Large Area Superconducting Nanowire Single Photon Detectors for HEP Science

Power [mW]

- Readout Channels
- Bias Channels
- Digital Power
- SerDes Lane
- PLL Power

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