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Developments of Reconfigurable Digital Logic in the ASIC using 130nm and 28nm CMOS

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With the push for future high-energy physics detectors to move more processing to the edge in an effort to reduce data volumes at the earliest possible stage, the ability to use programmable digital logic further up the digital signal processing chain becomes increasingly important. While embedded Field-Programmable Gate Arrays (eFPGAs) built into Application-Specific Integrated Circuits (ASICs) are nothing new, these frameworks were neither free nor open source. In recent years, several popular FPGA architectures have aged beyond 20 years, which means that the original patents have expired. In 2021, the University of Manchester initiated a project called FABulous, which is an open-source eFPGA Framework.
FABulous has demonstrated eFPGA designs in 180nm CMOS and 130nm CMOS at the University of Manchester. In 2022, SLAC demonstrated an eFPGA design using FABulous framework in a 130nm CMOS Multi-Process Wafer (MPW). For 2023, our team taped out a 28nm CMOS MPW in July 2023 and expects to receive the ASIC back in November 2023. The goal of using 28nm is to determine what programmable logic area density can be achieved while using HVT devices for radiation hardening.
This 28nm eFPGA design will utilize the SLAC Ultimate Gateway Operational Interface (SUGOI), which is a lightweight 8B10B-based serial protocol for register access, to load the eFPGA bitstream. The Pretty Good Protocol Version 4 (PGPv4), which is a 64B66B-based serial protocol designed for Trigger Data Acquisition (TDAQ) systems, will be used to move data in and out of the eFPGA.
We will present the performance of our 130nm design, the Post-PnR simulation results for our 28nm design, and a comparison between the two designs at this workshop.

Early Career

No

Primary author: RUCKMAN, Larry (SLAC)

Co-authors: GUPTA, Aseem (SLAC); KIM, Hyunjoon (SLAC); ROTA, Lorenzo (SLAC)

Presenter: RUCKMAN, Larry (SLAC)

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