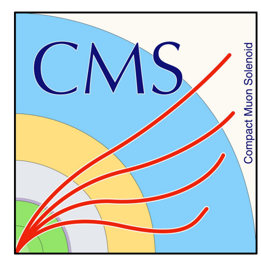

FERMILAB-SLIDES-23-368-CMS

CMS High Granularity Calorimeter ECON-D ASIC overview and radiation testing results

FNAL/LPC: Jyoti Babbar (Panjab) Bhim Bam (Alabama), Davide Braga, Alex Campbell (Alabama), Grace Cummings, Cristinel Gingu, Mike Hammer (Argonne), James Hirschauer, James Hoff, Neha Kharwadkar, Pam Klabbers, Danny Noonan, Paul Rubinov, Alpana Shenai, Cristina Mantilla Suarez, Chinar Syal, Xiaoran Wang, Ralph Wickwire. **FESB/Split:** Duke Coko. **CERN:** Gianmario Bergamin, Davide Ceresa, Rui De Oliveira Francisco, Szymon Kulis, Pedro Leitao, Matteo Lupi, Paulo Moreira, Simone Scarfi'. **Baylor:** Jon Wilson. **SMU:** Di Guo, Datau Gong, Dongxu Yang, Jingbo Ye. **KUL:** Bram Feas, Paul Jozef Leroux, Jeffery Prinzie.

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CPAD, 07 November 2023

Overview

CMS *High Granularity* Calorimeter Endcap, HL-LHC

HD full

R.Yohay

mass ~ 200 T
each endcap

2 m

Plastic Scint Tiles

CE-H (Sc)

CE-E (Si)

CE-H (Si)

$\eta = 1.5$

$\eta = 3$

r = 2.62 m

r = 0.28 m

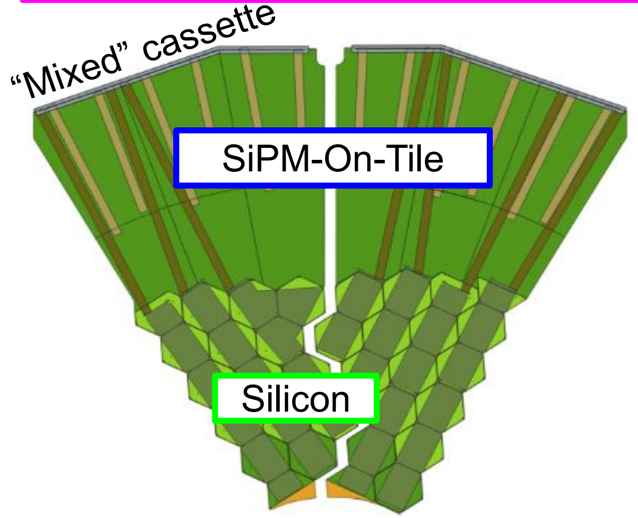
R.Kim

Silicon

47 layers of z-direction segmentation, ~30 ps timing in Silicon sections

HGCAL front end data path

Raw Data:
6M Channels → 5 Pb/s, ~1M links*



*Assumes 40 MHz rate and 50% link packing efficiency for 10.24 Gbps
**Assumes 750 kHz rate (trigger) and 50% link packing efficiency for 10.24 Gbps

HGCAL front end data path

Raw Data:
6M Channels → 5 Pb/s, ~1M links*

"Mixed" cassette

SiPM-On-Tile

Silicon

Hexaboard with HGCROC readout ASICs

Silicon Sensor

kapton

Cu/W absorber plate

HGROC: 1M Channels, trigger path → 300 Tb/s, **60k links***

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kapton

Cu/W absorber plate

HGROC: 1M Channels, trigger path → 300 Tb/s, **60k links***

"**E**ndcap **CON**centrator" On-detector data compression

Trigger decision

ECON-T

ECON-D

ECON-D 2023 V1 23/23

7x compression 40 Tb/s, **9k links***

Concentrator Mezzanine

*Assumes 40 MHz rate and 50% link packing efficiency for 10.24 Gbps
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HGCAL front end data path

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"Mixed" cassette

SiPM-On-Tile

Silicon

Hexaboard with HGCROC readout ASICs

Silicon Sensor

kapton

Cu/W absorber plate

"**E**ndcap **CON**centrator"
On-detector data compression

Trigger decision

ECON-T

ECON-D

accept

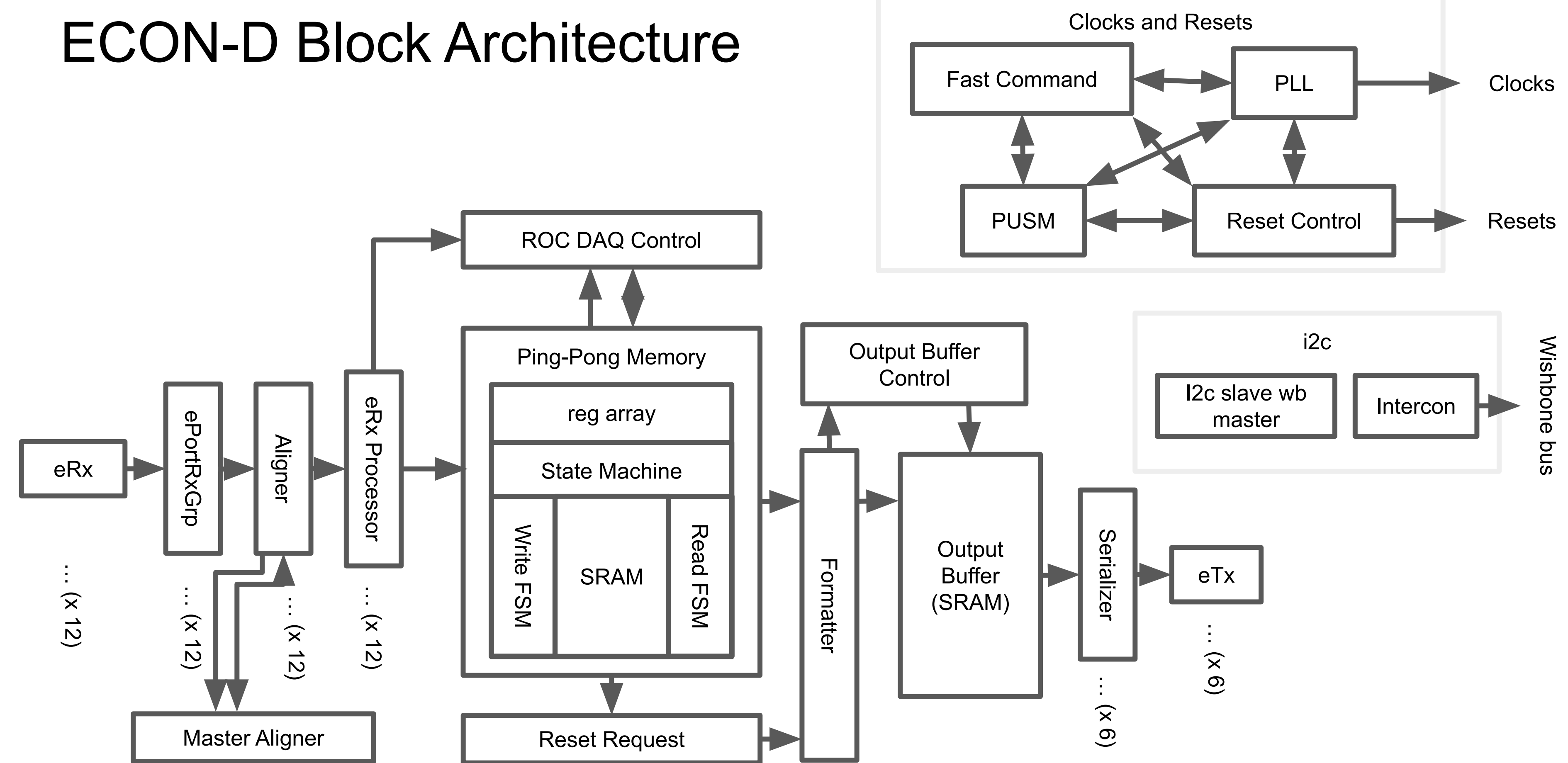
3x compression, **~9k links****

Concentrator Mezzanine

HGROC: data path → ~144 Tb/s, **30k links****

*Assumes 40 MHz rate and 50% link packing efficiency for 10.24 Gbps
**Assumes 750 kHz rate (trigger) and 50% link packing efficiency for 10.24 Gbps

ECON-D Block Architecture



ECON-D Block Architecture

Everything is triplicated EXCEPT

Clocks and Resets
Fast Command
PLL
Clocks
PUSM
Reset Control
Resets

ROC DAQ Control
Ping-Pong Memory
reg array
State Machine
Write FSM
SRAM
Read FSM
Reset Request

eRx
... (x 12)
ePortRxGrp
... (x 12)
Aligner
... (x 12)
eRx Processor
... (x 12)
Master Aligner

Output Buffer Control
Formatter
Output Buffer (SRAM)
Serializer
... (x 6)
eTx
... (x 6)

i2c
I2c slave wb master
Intercon
Wishbone bus

The data path is not (control logic is)

Measured with proton beam from the Northwestern Medicine Proton Therapy Center

Single Event Effect Testing

Goals of Single Event Effect (SEE) Test

1. Set *limit* on cross section (xs) requiring a reset
    - All configuration registers triplicated - did not expect to observe any errors
2. Confirm zero observed errors in triplicated i2c/config registers
3. Measure Single Event Upset (SEU) xs per bit for pre-voted flip-flop (FF)
    - Use TMR (triple modular redundancy) error counters
        - Count of *corrections*
4. Measure SEU-induced bit error rate in data
    - Tests the serializer/deserialzer + SRAMs
        - Errors in deserializer and SRAM only visible in **triggered-data**
        - Serializer errors appear in IDLES

Total Fluence: 4.99E13 protons/cm2

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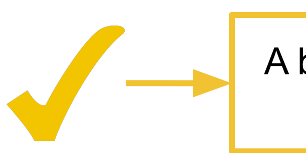
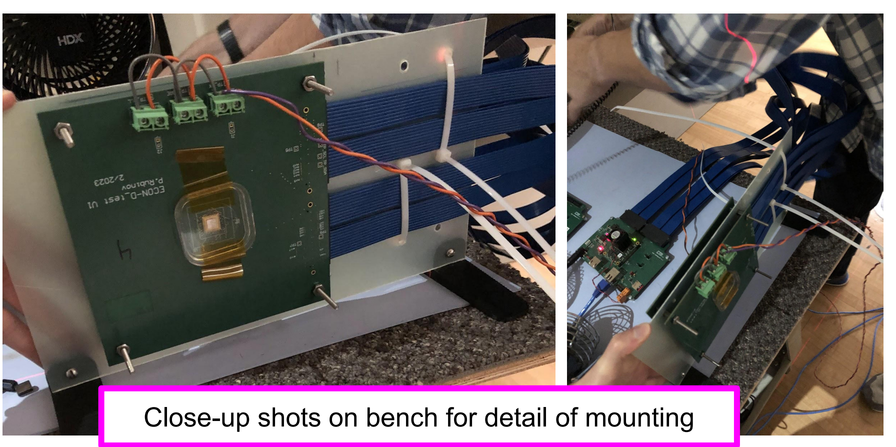


A bit limited - low L1A rate (3 Hz)

Total Fluence: 4.99E13 protons/cm2

SEE Testing Setup

- Test two ECON-D-P1
  - Neither are FIB’d chip
- Beam details
  - Aperture 2 cm x 2 cm
  - Continuous
  - 217 MeV
  - Flux varied per run (at request)



Close-up shots on bench for detail of mounting

Beam aperture

Cyclotron behind the wall - they would not let us see it :(

ECON-D Closest to beam (chip 4)
Farthest (pictured - chip 1)

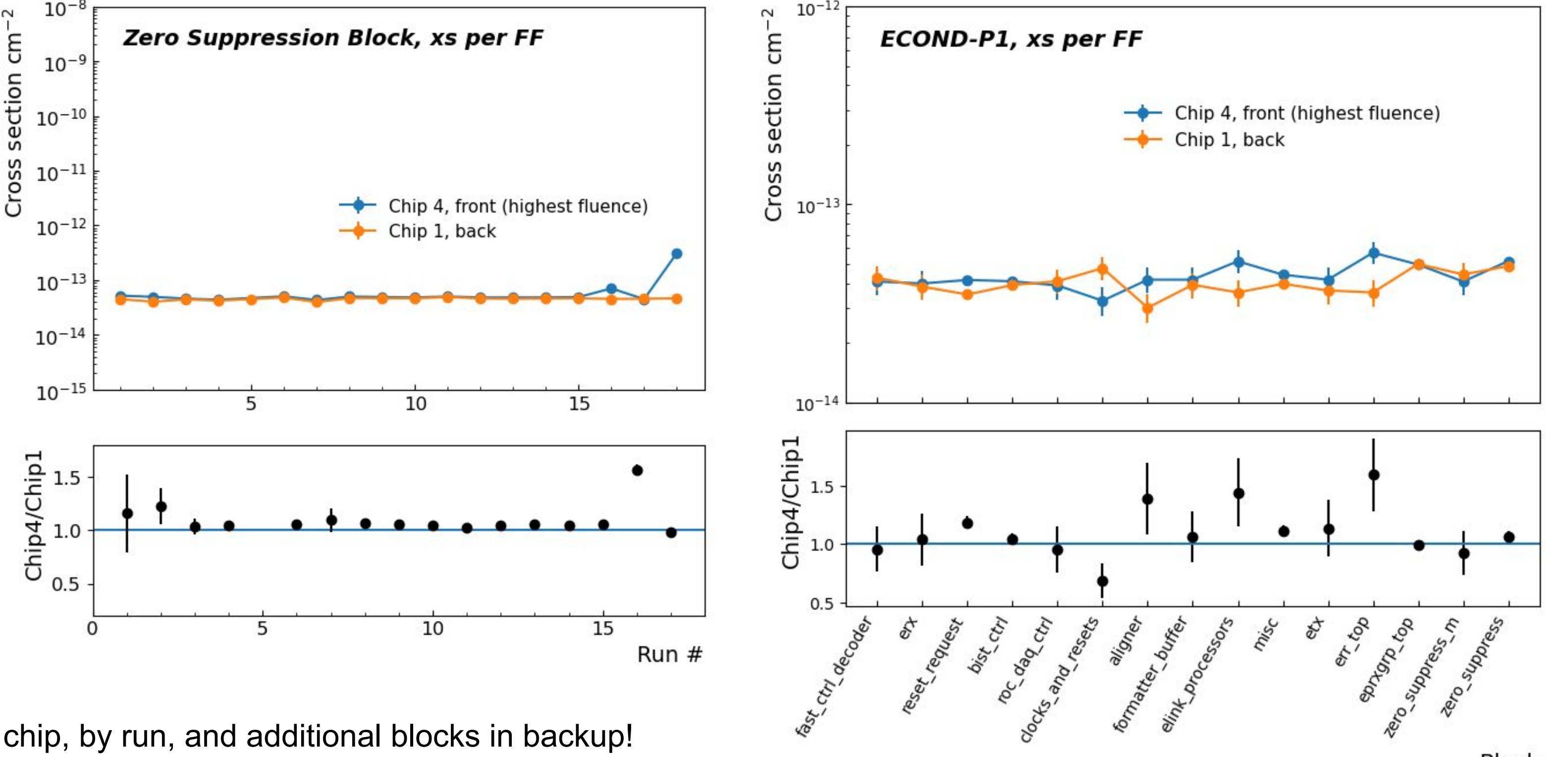
FPGAs for readout

PS for Chip 4

PS for Chip 1

Looking at Chip Comparisons

Cross section from counter of single bit flips that were then corrected!



By chip, by run, and additional blocks in backup!

Looking at Chip Comparisons

Differences in chips due to fluence, as expected!

Zero Suppression Block, xs per FF

Chip 4, front (highest fluence)
Chip 1, back

ECOND-P1, xs per FF

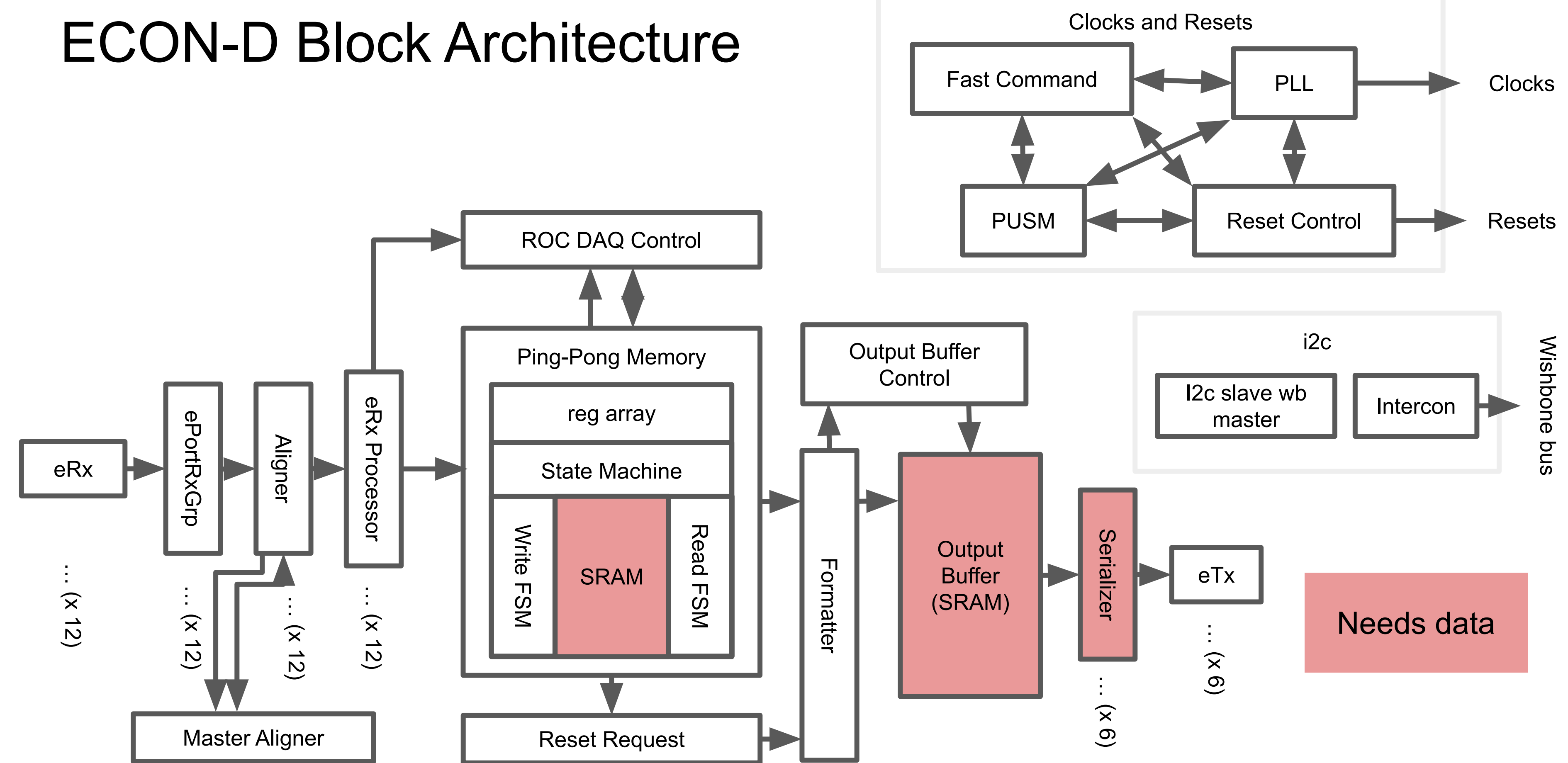
Chip 4, front (highest fluence)
Chip 1, back

Chip 4 Run 5 upset by SEE in FPGA controller

Chip 4 ZS all written to “0”

Clock A turned off

ECON-D Block Architecture



ECON-D Block Architecture

Clocks and Resets

Fast Command

PLL

Clocks

PUSM

Reset Control

Resets

ROC DAQ Control

Ping-Pong Memory

reg array

State Machine

Write FSM

SRAM

Read FSM

Output Buffer Control

i2c

I2c slave wb master

Intercon

Wishbone bus

eRx

ePortRxGrp

Aligner

eRx Processor

... (x 12)

... (x 12)

... (x 12)

... (x 12)

Formatter

Output Buffer (SRAM)

Serializer

eTx

... (x 6)

... (x 6)

IDLES

Master Aligner

Reset Request

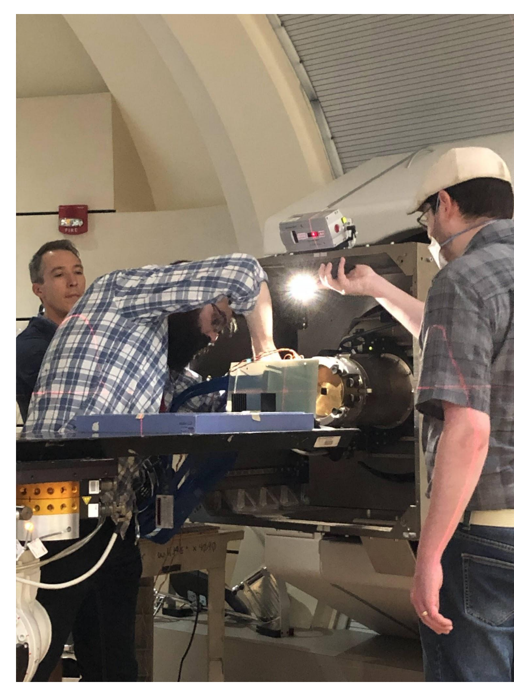
Bit error rate (BER) in eTx data

- Data errors taken from comparison of FPGA emulator and ASIC output
- BER observed in IDLE words ~ 4 x 10^{-10} errors/word
  - Tests *serializer* alone
- No bit errors observed in event packets → Cannot quote BER per trigger
  - **Trigger rate limited to 3 Hz for technical reasons****
  - Would test core logic + SRAMs + serializer
  - Use SRAM dwell time to compute cross section limit: $\boldsymbol{\sigma_{SRAM} < 1.1 \times 10^{-12}\ cm^2/bit}$
    - assume SEUs arise in SRAM
  - Upper limit on BER in “payload length” field of event packet $\boldsymbol{BER_{payload}}$ **< 0.5 Hz** for 27k ECON-D on entire HGCAL.
    - Computed using σ_{SRAM} and expected 750 kHz HL-LHC trigger rate
    - “Payload length” **protected by Hamming code for error correction in BE**, if necessary

**Low rate due to powering of chip-on-board → higher rates caused system instabilities that can be fixed with extra capacitance on the boards (discovered later)

SEE Testing Summary

- NO errors requiring reset observed
  - Upper Limit on XS on SEE requiring reset - 3×10^{-14} cm^2/ECOND
    - ~ 13 mins without reset
- Smooth and successful
  - Cross section for SEUs + Limits on errors requiring resets consistent with ECON-T-P1
- Cross section consistent across all measurements
  - Across runs
  - Chips
  - Blocks
- Infrequent L1As were a limitation in the results, but we are confident in the performance, and plan more testing



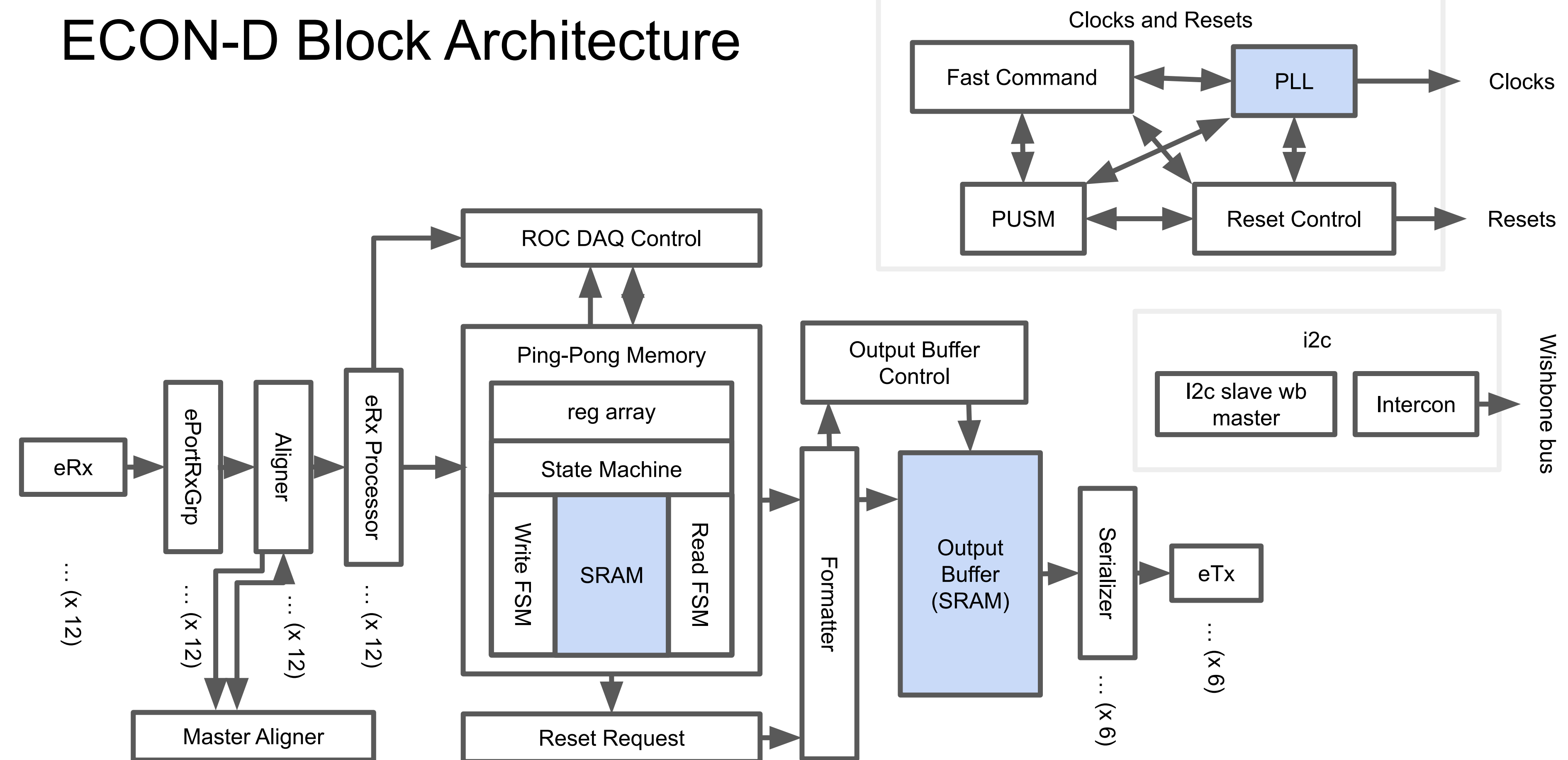
Done at the CERN EP-ESE ObeliX facility

Total Ionizing Dose Testing

Goals of Total Ionizing Dose (TID) Test

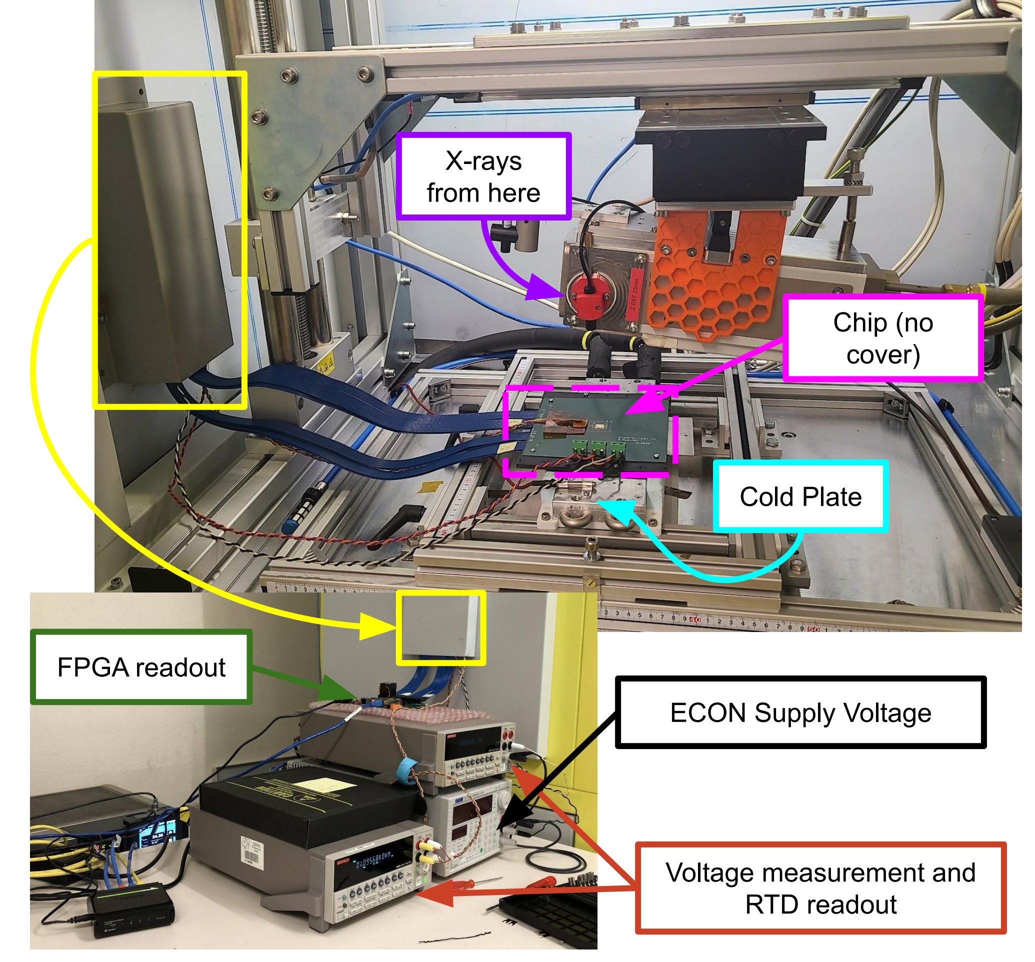
1. Characterize changes in behavior with dose ✓
   - PLL locking range and value
   - Automatic cap-bank setting
   - SRAMs
   - Data quality
2. Test operation at different operating voltages w/ dose ✓
3. Test operation at -30° C w/ dose ✓
4. Ensure ECOND will continue to function as expected at the end-of-life dose ✓
   - And at a factor of 3 over the expected HL-LHC dose

ECON-D Block Architecture



TID Testing Setup

- 3 Chips tested
- Cycled through supply voltages
  - 1.2 V ± 10%
- 660 MRad desired dose
  - ~9.2 MRad/Hour
  - 72 hours per chip
  - 3x safety margin
  - X-rays
    - Peak energy, 10 keV
- Cold plate held at -35°C
  - Dry gas continuously flowing



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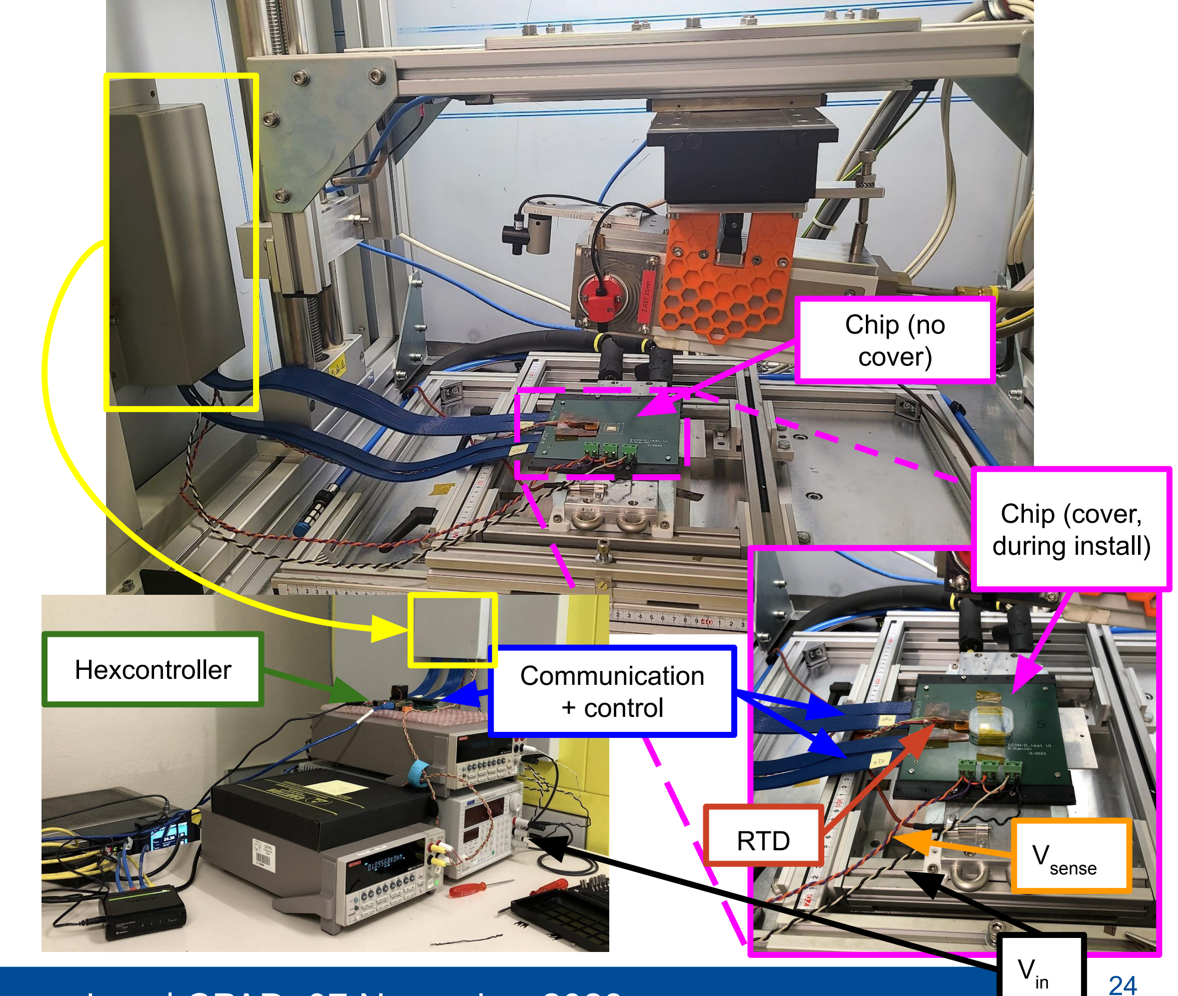


TID Testing Results - Phase, Delay, and Capbank Tests

Phase, delay, and capbank settings change with dose (as expected)

Phase Scan errors for eRx 11 at 1.2V Chip 7F

ECON-D-P1

Phase delay setting

TID (MRad)

PRBS error count in ~1 ms

Delay Scan errors for eTx 5 at 1.2V Chip 7F (40 MHz)

ECON-D-P1

Delay Scan Setting

TID (MRad)

Normalized word error count

Chip 7 (40 MHz)

Automatic Capbank Selection

1.08V
1.20V
1.32V

TID (MRad)

SRAM Tests - Ping pong

- At all nominal operation schemes (V_{in} > 1.1), **no errors**
- Writing/reading SRAM address in Ping pong failed in one chip at 1.08 V
- Reproducible in most chips w/out dose at voltages < 1 V

1.08V Chip 5 - 43 MHz
Chip 5
Ping Pong Bist Result
TID (MRad)

1.08V Chip 9 - 43 MHz
Chip 9
Ping Pong Bist Result
TID (MRad)

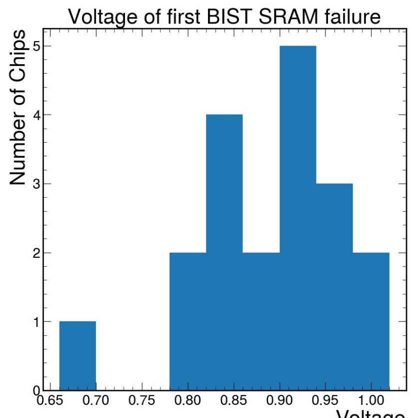
1.08V Chip 7F - 40 MHz
Chip 7F
Ping Pong Bist Result
TID (MRad)

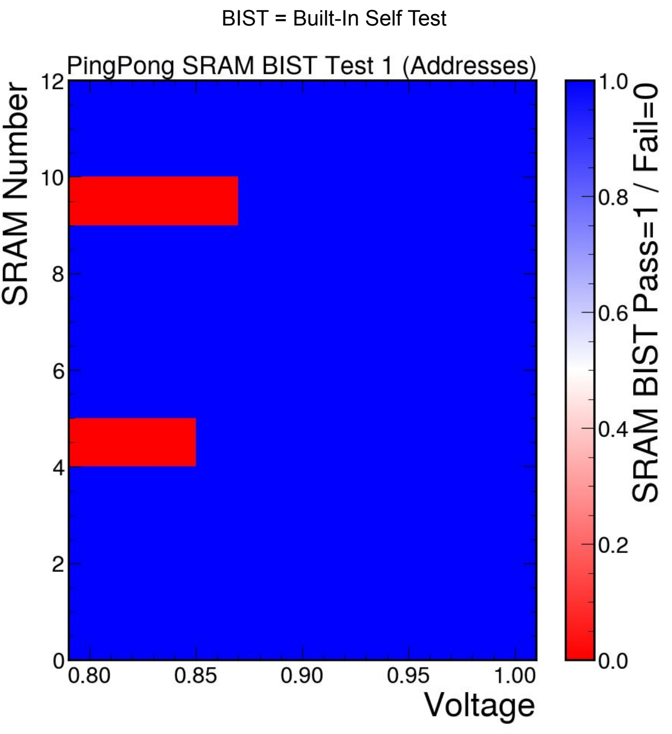
0 = Fail, 1 = Pass

SRAM Tests - Ping pong → Bench

- At all nominal operation schemes (V_{in} > 1.1 V), **no errors**
- Reproducible on bench at V_{in} < 1 V
  - Effected SRAM varies
  - Always happens in “test 1” → writing the SRAM address to the SRAM

BIST = Built-In Self Test





SRAM Tests - Output buffer

- At all nominal operation schemes (V_{in} > 1.1), **no errors**
- Chip 5 failed once we could no longer achieve lock - this is expected
- Can also see all 4 test failures in one SRAM at V_{in} < 1 on bench
  - Curious, but way out of specifications

1.08V Chip 5 - 43 MHz

OB Bist Result

TID (MRad)

Chip 5

1.08V Chip 9 - 43 MHz

OB Bist Result

TID (MRad)

Chip 9

1.08V Chip 7F - 40 MHz

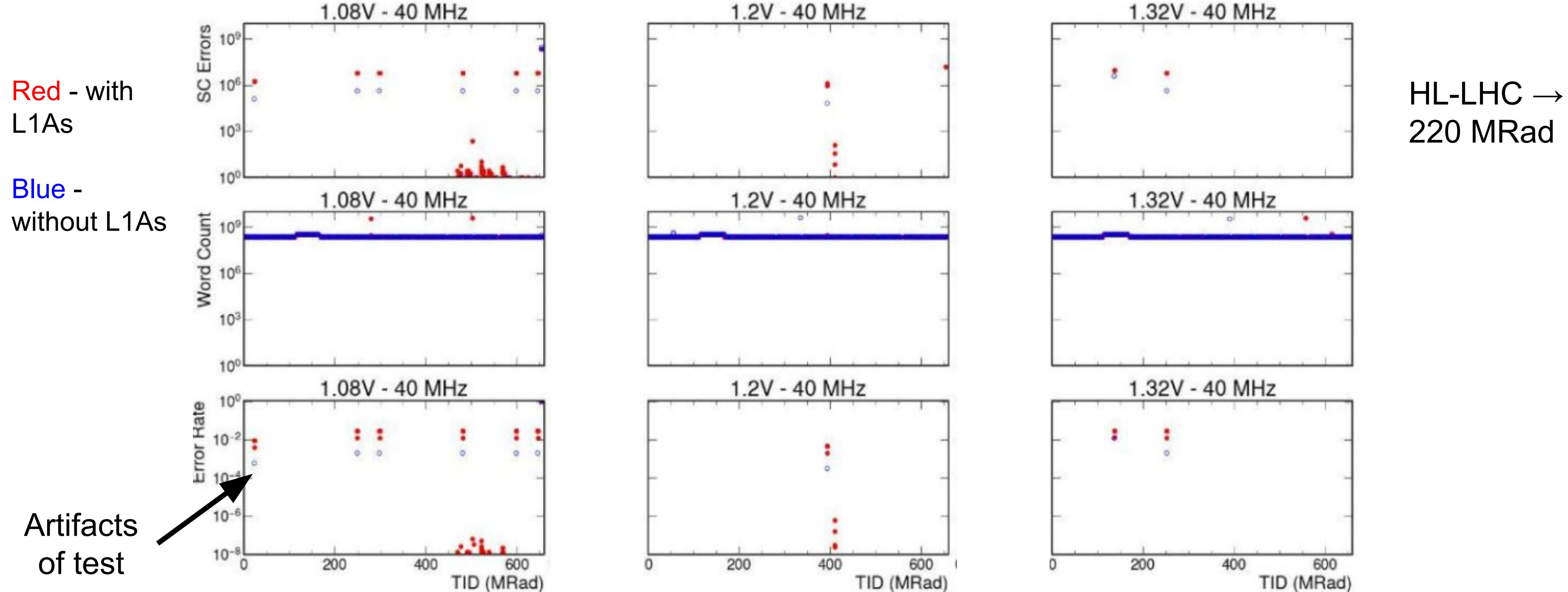
OB Bist Result

TID (MRad)

Chip 7F

Stream Compare Errors

- Only saw errors at low voltage in Chip 7F - 1.08 V and > 450 MRad



TID Testing Summary

- Expected behavior observed
  - Gradual changes with settings and PLL width
  - on par with ECON-T and lpGBT
- Operation OK at temperature and most voltages
  - 1.08 V a bit spotty above 450 Mrad for data errors
  - Ping pong issue in one out of the three chips at low voltage and dose
    - Though this can be triggered at very low voltage on bench

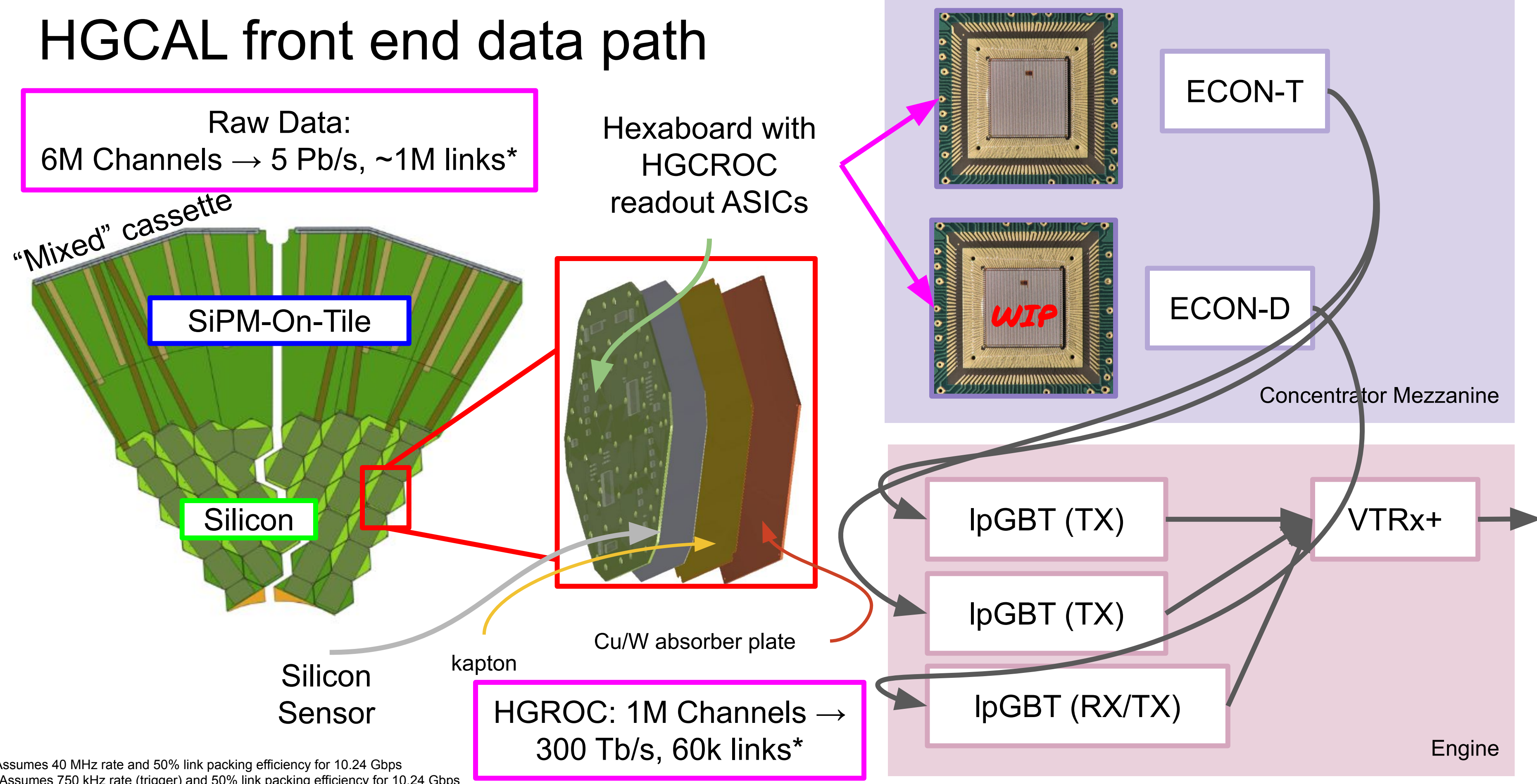
ECON-D-P1 Radiation Testing Summary

- All appears well!
  - All measurements align with expectations
- SEE Testing
  - SEE cross section tracks with ECON-T
  - Limit on errors requiring reset → 3 x 10^{-14} cm^2/ECON-D
  - ~ reset every 13 mins/per ECON-D
  - Potential limitation on data errors due to low L1A rate
- TID Testing
  - PLL and capbank behavior goes as expected
  - Discovered limitation of SRAM at low voltage - but all actual operation will be unaffected

Production versions of ECON-T and ECON-D arrive early next year! Production chips will undergo similar tests

back-up

HGCAL front end data path



*Assumes 40 MHz rate and 50% link packing efficiency for 10.24 Gbps
**Assumes 750 kHz rate (trigger) and 50% link packing efficiency for 10.24 Gbps

HGCAL front end data path

Hexaboard with HGCROC readout ASICs

ECON-T

“Mixed” cassette

SiPM-On-Tile

Silicon

Teststand DC/DC Converter

Wagon

V3 LD Engine

Optical Readout Fiber (to ZCU BE)

Concentrator Mezzanine with ECON-T

V3 LD Hexaboard with 3 HGCROCs

zzanine

+

Silicon Sensor

Kapton

Cu/W absorber plate

lpGBT (RX/TX)

Engine

*Assumes 40 MHz rate and 50% link packing efficiency for 10.24 Gbps

**Assumes 750 kHz rate (trigger) and 50% link packing efficiency for 10.24 Gbps

Tests completed

Run	Time [s]	Flux [p/cm2/s]	Fluence [p/cm2]	Tot Fluence [p/cm2]
1	52	2.55E+08	1.32E+10	1.32E+10
2	100	7.50E+08	7.50E+10	8.83E+10
3	159	1.68E+09	2.66E+11	3.55E+11
4	158	4.41E+09	6.96E+11	1.05E+12
5	117	8.60E+09	1.01E+12	2.06E+12
6	126	1.60E+10	2.01E+12	4.07E+12
7	30	4.58E+09	1.37E+11	4.20E+12
8	56	1.70E+10	9.50E+11	5.15E+12
9	180	1.59E+10	2.87E+12	8.02E+12
10	60	1.60E+10	9.60E+11	8.98E+12
11	609	1.58E+10	9.63E+12	1.86E+13
12	635	1.65E+10	1.05E+13	2.91E+13
13	194	1.63E+10	3.16E+12	3.22E+13
14	543	1.65E+10	8.94E+12	4.12E+13
15	354	1.64E+10	5.81E+12	4.70E+13
16	59	1.64E+10	9.66E+11	4.79E+13
17	58	1.64E+10	9.53E+11	4.89E+13
18	59	1.63E+10	9.65E+11	4.99E+13

Total Fluence: 4.99E13 protons/cm2

3 special tests:

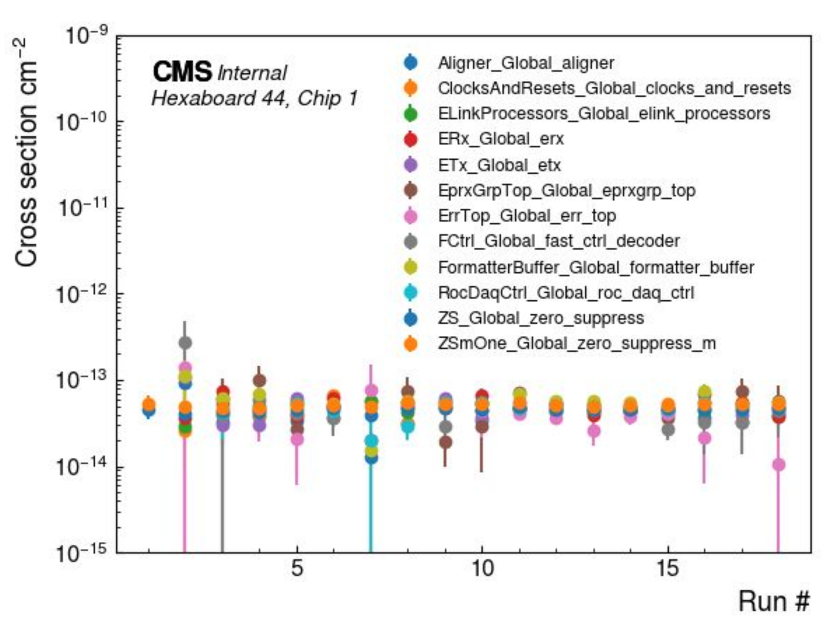
Run 16 → ZS written to all 0, ZSm1 written to all 1 (Chip 4)
Run 17 → ZS written to all 1, ZSm1 written to all 0 (Chip 4)
Run 18 → Clock A turned off (Chip 4)

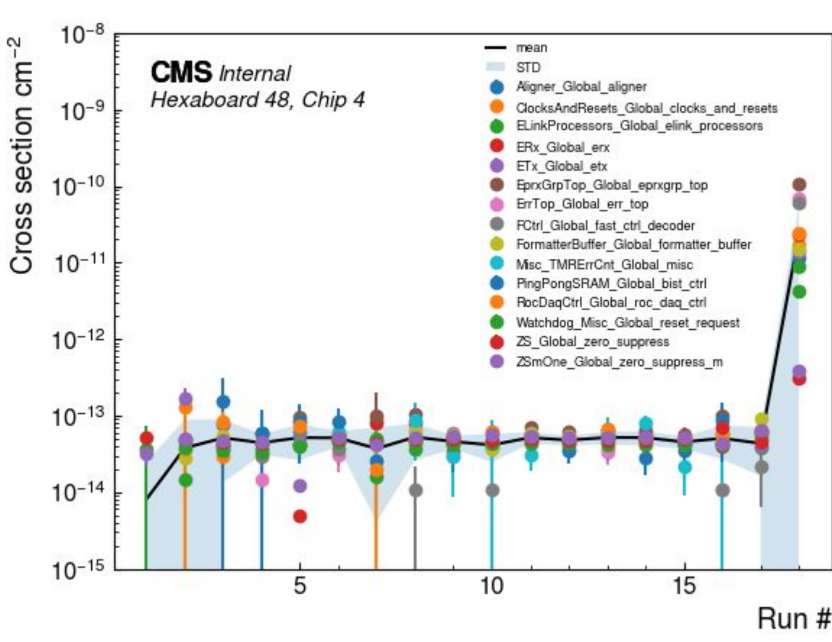
Difference in rate of SEU in 0 and 1's

Test triplication

Looking at SEU xs - All blocks but Channel Aligner

Consistent across runs and blocks





Looking at SEU xs - All ChAligner blocks - Chip1

CMS *Internal*
Hexaboard 44, Chip 1

Cross section cm^{-2} (axis: 10^{-15} to 10^{-8}); Run # (axis: 5, 10, 15)

- mean
- STD
- ChAligner_00_chan_aligner
- ChAligner_00_chan_err
- ChAligner_00_chan_eprxgrp
- ChAligner_01_chan_aligner
- ChAligner_01_chan_err
- ChAligner_01_chan_eprxgrp
- ChAligner_02_chan_aligner
- ChAligner_02_chan_err
- ChAligner_02_chan_eprxgrp
- ChAligner_03_chan_aligner
- ChAligner_03_chan_err
- ChAligner_03_chan_eprxgrp

CMS *Internal*
Hexaboard 44, Chip 1

Cross section cm^{-2} (axis: 10^{-15} to 10^{-8}); Run # (axis: 5, 10, 15)

- mean
- STD
- ChAligner_04_chan_aligner
- ChAligner_04_chan_err
- ChAligner_04_chan_eprxgrp
- ChAligner_05_chan_aligner
- ChAligner_05_chan_err
- ChAligner_05_chan_eprxgrp
- ChAligner_06_chan_aligner
- ChAligner_06_chan_err
- ChAligner_06_chan_eprxgrp
- ChAligner_07_chan_aligner
- ChAligner_07_chan_err
- ChAligner_07_chan_eprxgrp

CMS *Internal*
Hexaboard 44, Chip 1

Cross section cm^{-2} (axis: 10^{-15} to 10^{-8}); Run # (axis: 5, 10, 15)

- mean
- STD
- ChAligner_08_chan_aligner
- ChAligner_08_chan_err
- ChAligner_08_chan_eprxgrp
- ChAligner_09_chan_aligner
- ChAligner_09_chan_err
- ChAligner_09_chan_eprxgrp
- ChAligner_10_chan_aligner
- ChAligner_10_chan_err
- ChAligner_10_chan_eprxgrp
- ChAligner_11_chan_aligner
- ChAligner_11_chan_err
- ChAligner_11_chan_eprxgrp

Bit error rate in eTx data - Dwell Time

- 3 L1As 1000 BX apart each second
  - Low rate due to powering of chip-on-board → higher rates caused system instabilities that can be fixed with extra capacitance on the boards (discover later, Danny's talk)
- No errors observed in packets
  - Have to use dwell time weighted bits to get an upper limit on SEU cross section in SRAMs

$$N_{\text{bits}} \cdot t_{\text{dwell}} \cdot \phi_{\text{test}} = (780k \text{ bits} \cdot \text{BX/evt}) \cdot (2933 \text{ s}) \cdot (3 \text{ evts/s}) \cdot (1.63 \times 10^{10} \text{ cm}^{-2} \text{ s}^{-1})$$
$$= 2.8 \times 10^{12} \text{ cm}^{-2} \text{ bits}$$

  - 1.1×10^{-12} cm^2/bit upper limit on cross section of errors in SRAMs
  - Upper limit on errors in packet length for the entire detector at event rate of 750 kHz is 0.5 Hz
    - Protected by Hamming code
  - "Error" → comparison between ASIC and emulator