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From ETROC to VTROC (Vertically integrated Timing ReadOut)

Tuesday, 7 November 2023 13:45 (15 minutes)

The Endcap Timing ReadOut Chip (ETROC) is designed to process LGAD signals with time resolution down to about 40-50ps per hit, to reach 30-35ps per track with two detector layers. The ETROC2 is the first full size (16x16) prototype design and is fully compatible with the final chip specifications in terms of functionality. The ETROC2 has been extensively tested recently. In this talk, the testing results of the ETROC2 will be presented first, including performance study using charge injection, laser and beam, as well as TID testing and wafer probe testing to study the yield. In addition, future challenges of precision position and timing ASIC design will be discussed, based on what we have learned from the ETROC development, and how the challenges could be addressed in the VTROC, Vertically integrated Timing ReadOut chip (funded as SBIR phase 2) for precision position and timing detector R&D.

Early Career

No

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