From ETROC to VTROC

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CPAD at SLAC
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Higher luminosity means higher pile-up events

Silicon tracker with position information alone will not be enough to separate the pile-up events, precision timing detector can help: **CMS Endcap Timing Layer (ETL) is designed for this purpose**
Low gain is the key ingredient to excellent temporal resolution

- Low Gain Avalanche Detectors (LGADs)
  - Basic unit:
    - 2x2 cm$^2$ LGAD bump-bonded to ETROC ASIC mounted on two sides of cooling plates
    - Two layers/disks per endcap (~2 hits per track)
    - 1.6 < $|\eta|$ < 3.0, surface ~14 m$^2$; ~9 M channels
    - Nominal fluence: $1.7 \times 10^{15}$ $n_{eq}$/cm$^2$ (@ 3000 fb$^{-1}$)
  - LGAD gain modest: 10-30
    - LGAD Landau contribution: ~30ps
    - Front-end contribution should be kept < 40ps
    - < 50ps per hit, or 35ps per track (with 2 hits)

- Extract precision timing from
  - Small LGAD signal (typical 10-20 fC)
    - With low power: < 4mW/channel on average

**Challenges:**

- Low power and fast/precision timing,
- Precision clock distribution,
- Minimizing readout digital activities
ETL ASIC:

A System design Including a Chip
ETROC2 design strategy: most building blocks have been silicon proven

Front-end:
Charge injection/DAC
Preamp,
Discriminator
TDC

All tested in ETROC0/1, and reused in ETROC2

- PLL
  - PLL is based on lpGBT and validated with PLL test chip (+SEU)
- I2C
  - I2C design validated with I2C test chip, including SEU
  - In-pixel I2C register expanded and verified
- TS (Temp Sensor)
  - TS validated with I2C test chip
- Efuse
  - Efuse validated with I2C test chip
- VREF
  - VREF validated with I2C test chip
- GRO
  - Reusing the GRO in ETROC1
- Tx and Rx
  - Reusing Tx in ETROC1
  - Reusing Rx in ETROC1 (from lpGBT)
- WS (Waveform Sampler)
  - Rad-hard version tested and works well
  - In-pixel threshold calibration
    - tested with ETROC0 via FPGA emulator

All critical analog building blocks have been silicon proven in testing chips, and the digital building blocks have been emulated in FPGA and tested with the downstream readout board with backend.
ETROC2 digital readout: pixel and global

What’s new & time consuming:
Pixel readout & Global digital
ETROC2 key features: from testing/user point of view

Initial testing done, chip is functional well

- **Self-test pattern generator (works well)**
  - Can be used to test the digital data flow and link interfaces. Users can dial the occupancy of pixels and change patterns
    - This feature has been used extensively to simulate and verify the readout design of ETROC2, at RTL level and post layout stage
    - First thing user can test with ETROC2 emulator, the same test can then be done for bare ETROC2 and bump bonded ETROC2
    - At chip level (as build in self-testing capability), board level, and system level (with DAQ backend)

- **Testing with charge injection (works well)**
  - *Test the full path from charge injection to preamp to discriminator to TDC to circular buffer to event buffer to global digital readout*
  - Discriminator threshold scan and jitter measurements (bare ETROC2 first, then bump bonded ETROC2)
  - User can define the window for TOA, TOT and CAL to filter/suppress hits before readout
  - User adjustable TOA measurement window (up to 12.5ns, 11.4ns effective)
  - Each pixel can be enabled or disabled for DAQ readout
  - The relative phases adjustable between the TDC clock, pixel readout clock and global readout clock

- **ETROC2 testing with LGAD sensor, laser, source and then beam (on going)**
  - Full path timing performance study including LGAD

- **Auto-threshold scan within pixel (single pixel scan works)**
  - This new feature will be studied first by dedicated ETROC2 chip level testing

- **Trigger path (used in beam testing and cosmic as self-triggering)**
  - Can be used for monitoring purpose initially, a coarse map of user defined hits continuously sent out every BC
  - Can be used for self triggering for beam test if so desired, user can define the window for TOA, TOT and CAL for triggered hit
  - Use flashing bits in empty BCID (beam gap), defined via I2C. Can be used as cross check and monitoring purpose.

- **Waveform Sampler (initial test works)**
  - Able to record waveform of one pixel up to 16 bunch crossing (400 ns), start and stop controlled via fast command, readout via I2C
  - power-down when not used, intend to use for monitoring purpose during detector operation

- **Power consumption estimate is ~1W per chip, confirmed with ETROC2 chips (initial testing looks good)**

*six months into testing so far, a lot has been done*
**ETROC2 is a learning chip, need to learn as much as we can to guide ETROC3 design, and also better prepared for the full validation of ETROC3**

**ETROC2 chip level testing road map**

- **ETROC2 chip level testing**
  - **Bare ETROC2 testing**
    - Single pixel scan
    - Torture testing
    - TID
    - **SEU**
  - **Single pixel scan**
    - **Charge Injection noise study**
    - **laser beam**
    - **Temp vs Voltage vs TID to scan operation phase space**
  - **TID**
    - **Wafer probing yield study**

**System level testing**

- **With Bare ETROC2**
  - **2x2 LGAD + ETROC2 wire bonded**
    - **Charge Injection noise study**
    - **laser beam cosmic**
  - **16x16 LGAD + ETROC2 bump bonded**
    - **prepare for**
      - **Charge Injection noise study**
      - **laser beam cosmic**

**ETROC2 chips received in late April 2023**

Blue: done
Green: on going
Red: not yet

**Passed 200 MRad TID test**

- works with voltage (1.3V to 1.0V) vs temperature (-30C to +30C) before and after TID.

**First beam test at CERN in Sept 2023: commissioning run**

**Second beam test at DESY (Dec): two weeks beam**

**More beam tests reserved at DESY early 2024**

**Only few highlights in this talk**

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**ETROC**  **T. Liu**  **11/6/23**
Testing with 2x2 sensor wire bonded

Bare Pixels

Wire bonded pixels
Bump bonded case

Noise level very promising, better than wire bonded with 2x2 sensor.
CAL ~207
TOA bin=15ps

40ps line
30ps line
15ps line
**ETROC2 Telescope: a full sub-system**

Fully self contained, self triggered system for precision timing characterization of the ETROC chips

3-4 ETROC2 boards with master clock and FPGA boards

Modular suitcase makes the telescope portable for cosmics data taking and test beams at FNAL/CERN/DESY etc

*Packed inside a big suitcase travel to CERN on Sept 16*

At Fermilab: Sept 11th week
2 bump bonded chips arrived the week before
CERN trip... assembled the bump bonded ETROC2s into the telescope very quickly and took some cosmic rays
Beam Test at CERN in Sept: telescope DAQ worked on the very first try

Top board: 2x2 sensor wire bonded

Middle board: bump bonded

Bottom board (bump bonded)

Event display look similar to cosmics

Beam spot seen by ETROC2

Cosmic
First set of beam data: ~5k events with exactly one hit per board in these pixels

We didn’t have time to test the newly bump bonded boards before beam, as they arrived few days before beam.

The very first CERN beam test was just for testing the new ETROC2 telescope operation, and it was successful.

First set of data taken: Sept 24 at CERN
The very first CERN beam test was just for testing the telescope operation hardware, firmware and software (online & offline), to better prepare for DESY beam test in Dec 2023. not meant for performance study.

Nevertheless, we performed some data analysis to check the data integrity, even though the setup was not optimized.

The derived time resolution of DUT (Board 3): 39 ps

**The usual analysis procedure:**

1. Convert TOA and TOT in [ns] from TOA code and TOT code
2. Construct the pairwise differences $T_{ij} = TOA_i - TOA_j$
3. Perform time walk corrections
4. Extract widths $\sigma_{ij}$
5. Time resolution $\sigma_i = \frac{1}{\sqrt{2}} \sqrt{\sigma_{ij}^2 + \sigma_{ik}^2 - \sigma_{jk}^2}$
First look at bump bonded ETRO2C performance with a double pulse IR laser at CERN-SSD

\[ \sigma_{\text{ToA}}^2 = \sigma_{\text{laser}}^2 + \sigma_{\text{Clock}}^2 + \sigma_{\text{sensor}}^2 + \sigma_{\text{ETROC2}}^2 \]

As seen by monitoring photodiode

Jitter is calculated as:

\[ \frac{\sigma(\text{TOA}_1-\text{TOA}_2)}{\sqrt{2}} \]

ETRO2C bump bonded with 16x16 sensor

Two pulse “timing” configuration

Preamp at high power with ~1 MIP laser signal

9ps
Noise width of 16x16 array

Inclusive TOT vs TOA without any offline cut

Single newly bump bonded ETROC2 board with 15 hours of exposure to cosmic: occupancy

Fresh raw data on Oct 30
Waveform sampler is intended for monitoring purpose only, power down if not in use.

Passed 200MRad TID.

400ns of waveform recorded in WS memory
ETROC system interfaces

Our system development strategy:
use ETROC2 emulator to speed up system development

ETROC2 has been recently tested successfully with the module and readout and power board prototypes together with the back-end electronics.
ETROC: pixel size vs design block size

**Future challenges:** how to reduce the pixel size from 1.3mm x 1.3mm to say 250µm x 250µm?
Towards the future: What can 3DIC VERTICAL INTEGRATION help?

à repartition the design blocks into multi-tiers ➔ VTROC

Phase II SBIR (EPIR-Fermilab) award:

For Proof-of-principle demonstration:

- 250µm x 250µm pixel
- 8×8 pixels

"Versatile, high-density, high-yield, low-capacitance 3D integration for nuclear physics detectors" (phase 2)

3DIC providing separation of low-noise analog circuitry from digital blocks.
Interconnections made by TSVs and Direct Bond Interconnect (DBI).
From CMS ETROC to future R&D

CMS ETL ETROC: from Concept (2019) to full chip design ETROC2 submission (Oct 2022)

VTROC R&D: From Concept to first demonstration for proof-of-principle

"Versatile, high-density, high-yield, low-capacitance 3D integration for nuclear physics detectors" (phase 2)

Phase 1 done
Phase 2 awarded this year

Ted Liu, ETROC Project
ETROC Team/collaboration is growing fast

ETROC2 poster for TWEPP Oct 2-6 2023

ETROC2: the first full size, full functionality Precision Timing ASIC prototype for LGAD-based CMS Endcap Timing Layer (ETL) Upgrade

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ABSTRACT

The ETROC (Endcap Timing Readout Chip) is being developed for the LGAD-based CMS Endcap Timing Layer (ETL) at HL-LHC. The ETL on each side of the interaction region will be instrumented with a two-disk system of MIP-sensitive LGAD (Low Gain Avalanche Diodes) silicon devices, read out by ETROCs for precision timing measurement with down to ~35 ps timing resolution. The ETROC is designed to handle a 16 x 16 pixel cell matrix, with each pixel being 1.3 mm x 1.3 mm to match the LGAD sensor pixel size. Approximately 15% of the sensors near the highest eta region will experience hadron fluence above 1e+15 neq/cm² towards end of operation of HL-LHC, resulting in small signal amplitude with reduced LGAD gain. For this reason, the front-end design for preamplifier and discriminator has been specifically optimized for the reduced LGAD signals, with enough flexibility to meet the ETL specific needs for time resolution, power budget and radiation profile.

The ETROC chip is implemented in a commercial 65nm CMOS process. Each channel consists of a preamplifier, a discriminator, a TDC used for TOA (Time Of Arrival) and TOT (Time Over Threshold) measurements, and a memory for data storage and readout. An in-pixel auto threshold calibration is included, along with a self-testing pattern generator. The TOT is used for time-walk correction of the TOA measurement. The detailed hit information (TOA and TOT) from each cell will be read out from a local circular buffer after each Level-1 Accept (about 1 MHz). In addition, a charge injection circuit is implemented to allow for testing and calibration. For more detailed monitoring of signal pulses as radiation dose increases, waveform sampling circuits are included for one pixel. The clock distribution is based on the ETROC1 4x4 H-tree design, scaled up to 16x16 with a new shielding structure added to alleviate potential interference. The global peripheral circuits include a PLL, a phase shifter, an I2C slave controller, a fast control block, a global readout, and a data driver along with an efuse and temperature sensor. The ETROC builds event data frames for each L1A selected event and is also capable of providing L1 trigger information for user-defined delayed hits. The main design challenge is how to extract precision timing information from the small LGAD signals in the presence of high irradiation fluence, while keeping the power consumption and digital activity low. The ETL design goal for the time resolution of 50 ps per hit is required to achieve a 35 ps arrival time measurement for a MIP particle, which has its track registered in two ETL disk layers. The LGAD contribution is known to be about 30 ps, this means that the jitter from the ETROC has to be kept below 40 ps.

The ETROC2 is the first full size (16x16) and full functionality prototype and its dimension is 21mm x 23mm, making it one of the largest chips in HEP.
Baseline and noise width from in-pixel automatic threshold scan (very fast to map out 16x16 array)

https://iopscience.iop.org/article/10.1088/1748-0221/16/09/T09006

Noise Width (NW):
- Bare ETROC2: ~ 3-4
- Wire bonded: ~ 6-9
- Bump bonded: 4-6
2021 vs 2022 Test Beam test results

* Testing team (UIC/SMU/FNAL + students from KSU/KNU/CNU)

120 GeV proton Beam

Ch 1 (pixel 5)

Ch 2 (pixel 5)

Ch 3 (pixel 5 or 9)

Three ETROC1 Boards telescope

Clock distribution

~42.0/42.7/41.3 ps (2021 beam test)

~41.3/38.0/41.3 ps (2022 beam test)

(with LGAD HV=230V for all three channels)

**ETL Time resolution**

<table>
<thead>
<tr>
<th>Simulation /expectation vs spec</th>
<th>LGAD+ preamp/discriminator + TDC bin</th>
<th>35 ps</th>
</tr>
</thead>
<tbody>
<tr>
<td>Time-walk correction residual</td>
<td>&lt; 10 ps</td>
<td></td>
</tr>
<tr>
<td>Internal clock distribution</td>
<td>&lt; 10 ps</td>
<td></td>
</tr>
<tr>
<td>System clock distribution</td>
<td>&lt; 15 ps</td>
<td></td>
</tr>
<tr>
<td>Per hit total time resolution</td>
<td>41 ps</td>
<td>50 ps</td>
</tr>
<tr>
<td>Per track (2 hits) total time resolution</td>
<td>29 ps</td>
<td>35 ps</td>
</tr>
</tbody>
</table>

The measured time resolution includes all four contributions in the table

Single-hit timing resolution (ps) with TWC:

\[
\sigma_i = \sqrt{0.5 \cdot \left( \sigma_{ij}^2 + \sigma_{ik}^2 - \sigma_{jk}^2 \right)}
\]

~ 42.0/42.7/41.3 ps (2021 beam test)

~ 41.3/38.0/41.3 ps (2022 beam test)

reproduced 2021 beam test results, with new ETROC1 boards and independent analysis

(2022 beam test mostly done by 4 graduate students)
A simple ETROC0 Beam Telescope (with 3 ETROC0 boards)

Jan-Feb 2020

Simple "suitcase" setup in parasitic mode running at FNAL MTest

$\sigma_2 = \sqrt{0.5 \cdot (\sigma_{21}^2 + \sigma_{32}^2 - \sigma_{31}^2)}$

$\approx 33 \text{ (ps)}$

At room temperature

Ch1/2/3 waveforms

120 GeV proton Beam

preamp waveform
ETROC TDC

hitFlag: discriminator is fired or not

- bin = T3/Cal_code
- TOA = 12.5 - bin*TOA_code

T3 is programable with, 3.125 ns by default.