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Pebbles: paving the way toward 4D Pixel detectors in 28nm CMOS

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Detectors at future colliders will rely on the ability to perform 4D tracking with $O(10\text{ps})$ resolution. As a stepping stone towards these future detectors we have developed a prototype ASIC, Pebbles, that contains the Big Rock analog front-end and embedded testing circuits. The Big Rock front-end aims to achieve 50ps timing resolution while maintaining all other requirements from the current generation RD53 Pixel readout chips (50um x 50um pitch, 1000e threshold, 5uW per pixel, 50fF input capacitance). This kind of pixel front-end could serve as an interesting stepping stone towards future 4D trackers, as it could be deployed during the potential replacement of innermost layers of the ATLAS ITk Pixel detector. We will present the analog-front and test bed architecture design and the summarize the bench top test results from the prototype ASIC.

Early Career

Yes

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