

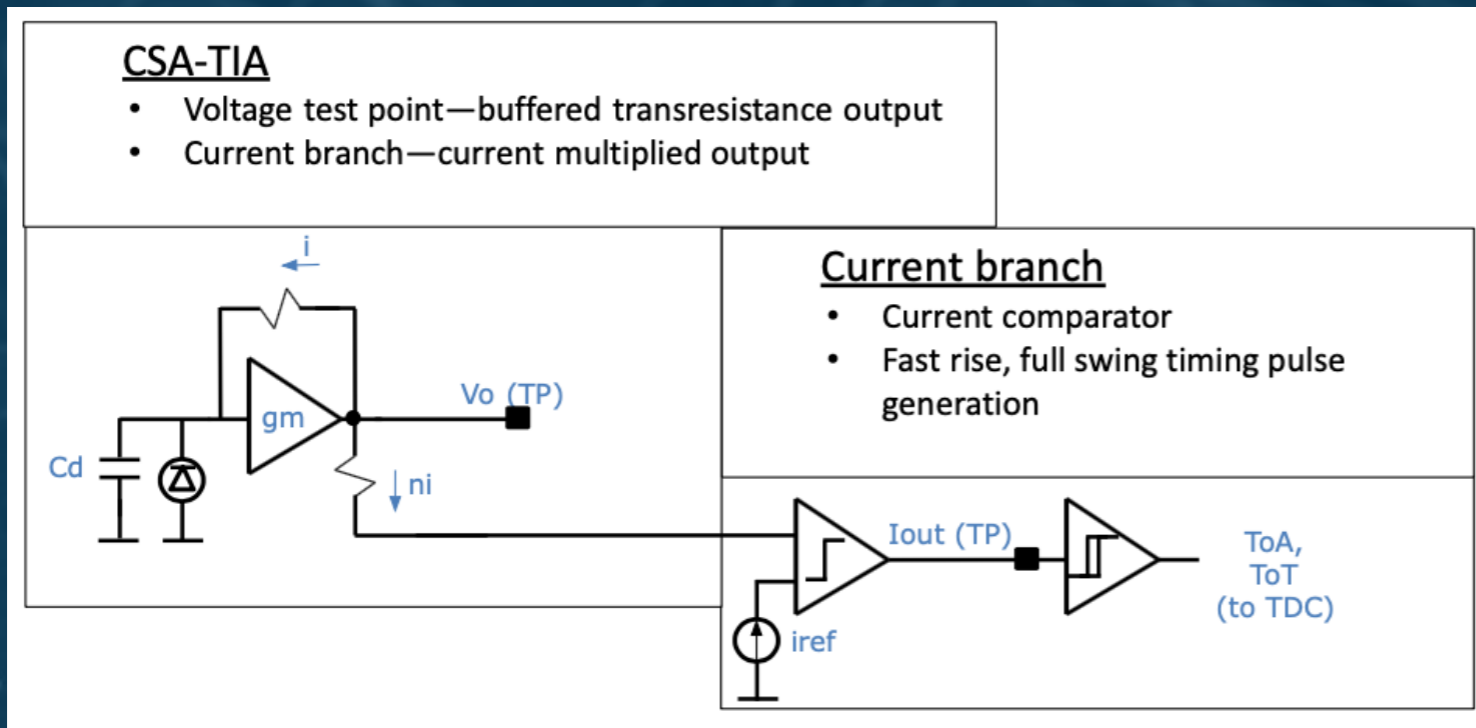
Pebbles: paving the way towards 4D Tracking detectors

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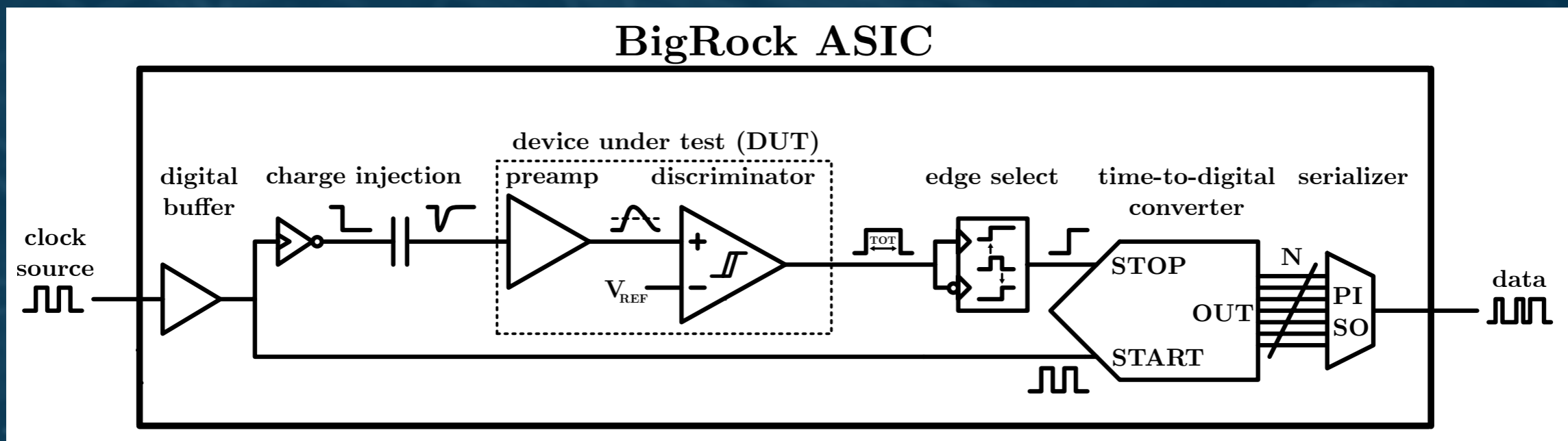
- ATLAS ITk Pixel inner system **designed for half of the original HL-LHC run time** → **planned to be replaced** half-way through HL-LHC era
- Final opportunity for more than a decade to test and operate a **real 4D tracker** in the flesh, but have to set achievable specs
 - Maintain current ITk specs:
 - 50um by 50um pixel pitch
 - Analog front-end: <100e noise, <1000e threshold, <5uW, 30um x 30um
 - Add:
 - ~50ps timing resolution (AFE, TDC, readout logic) (3D sensor technology)
- 65nm technology fully exploited with current needs (>90% routing density in ITkPix pixel)
- Any additional logic requires miniaturization → 28nm CMOS
- LBNL has started effort in 28nm CMOS chip design with **focus on analog front-end and time-to-digital converter**



	Specs
Idc	4uA
sigma(ToA)	~50ps
Threshold	<1000e
ENC	<100e
Area	10x30um ²
Cin	50fF

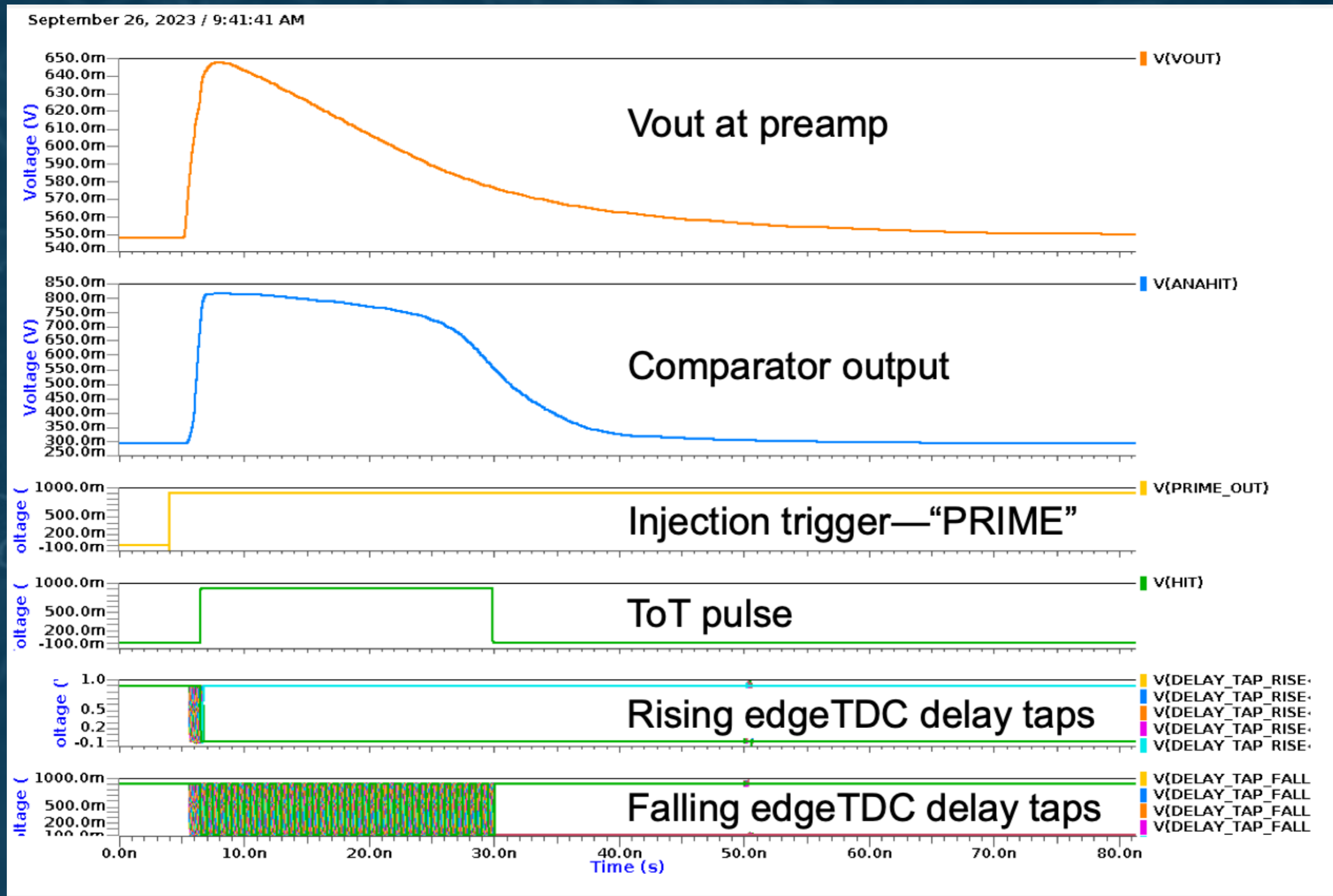
- Typical cascode CSA design
 - “Pseudo TIA” with fast peaking time (3-10ns) to optimize for low jitter
- Input current charge pulse mirrored to current comparator
- Mirror factor controllable through biases

Based on: Pierre Jarron, et. al, A transimpedance amplifier using a novel current mode feedback loop, 1996

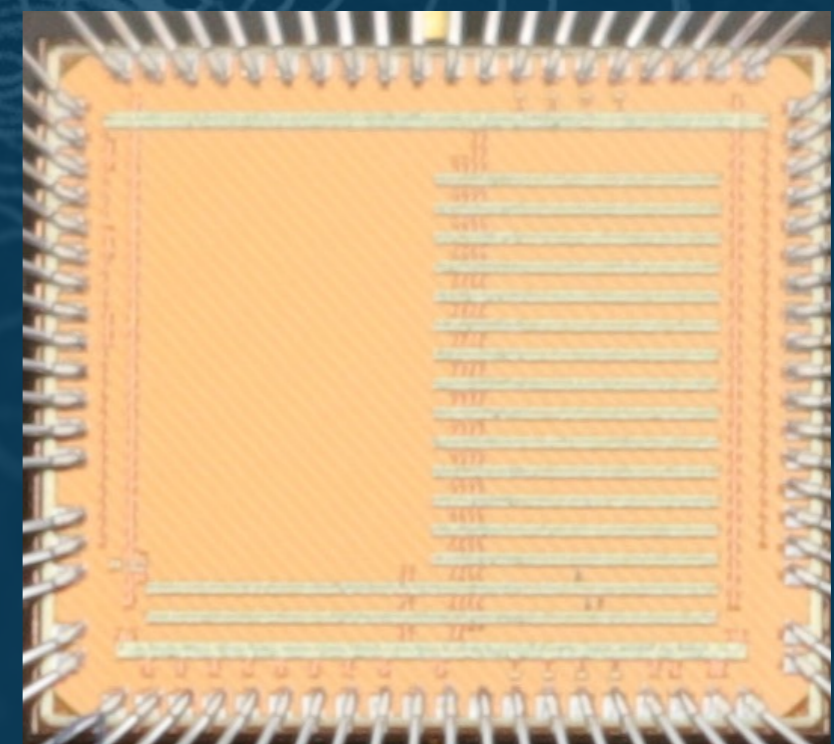
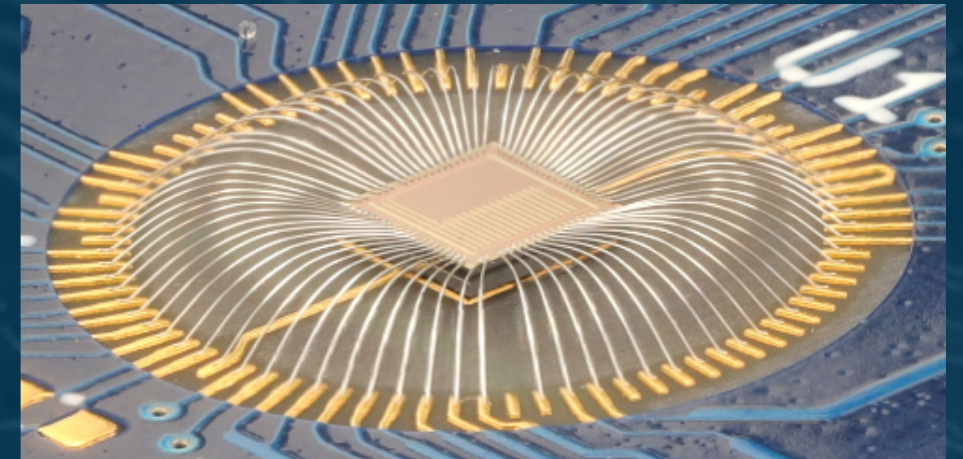


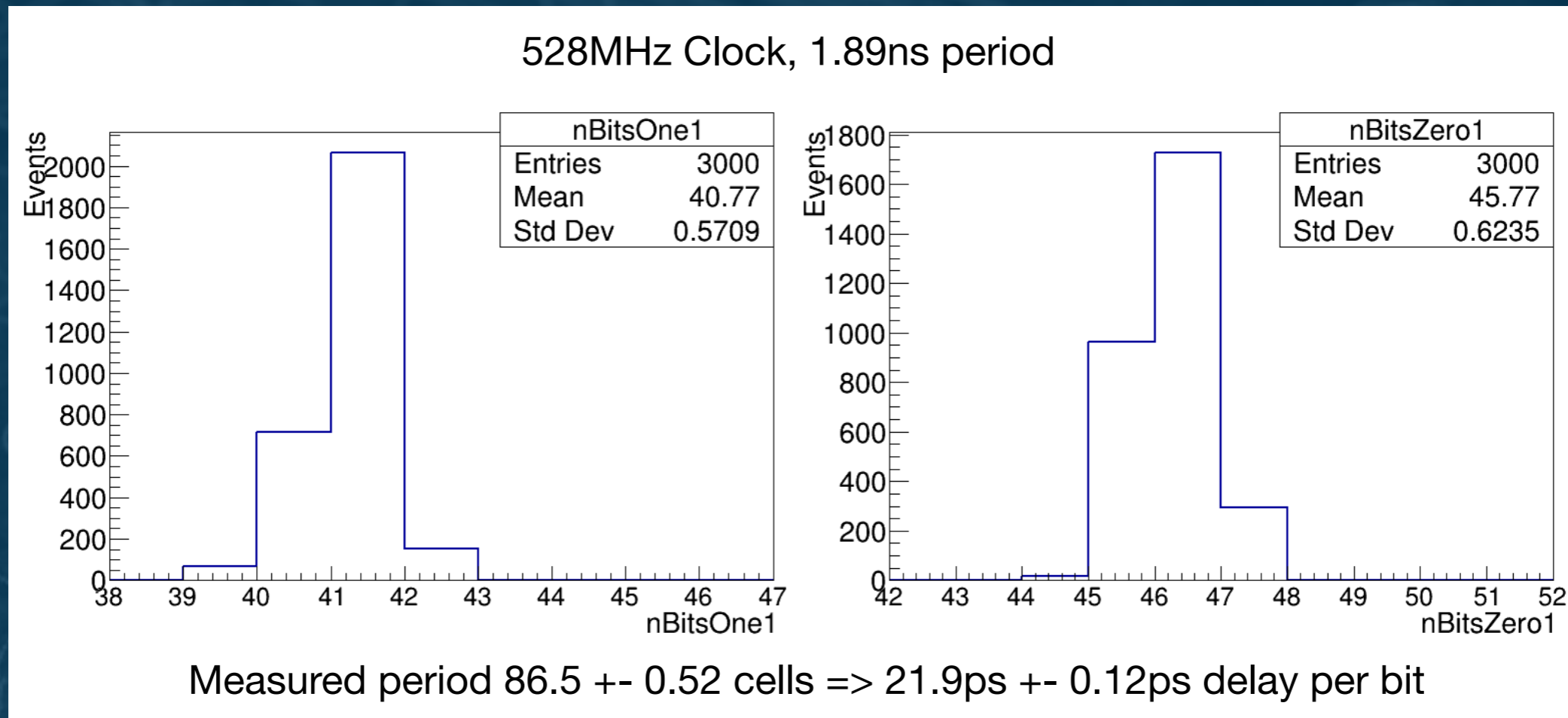
TDC concept:

- Only meant for characterization not for usage in real pixel chip (too large, too much power)
- Differential delay-element chain
 - ~10ps resolution
- External precision 1GHz clock issues injection and simultaneously ripples through delay chain
 - Coarse counter at output of delay chain (Clock period resolution, 1ns)
- Stop signal from front-end freezes delay chain
 - Readout as fine count (~10ps resolution)
- By making delay chain slightly longer than one clock period have intrinsic calibration for each each measurement
- Two TDCs per front-end, one to measure rising edge, the other for falling edge -> very precise ToT measurement

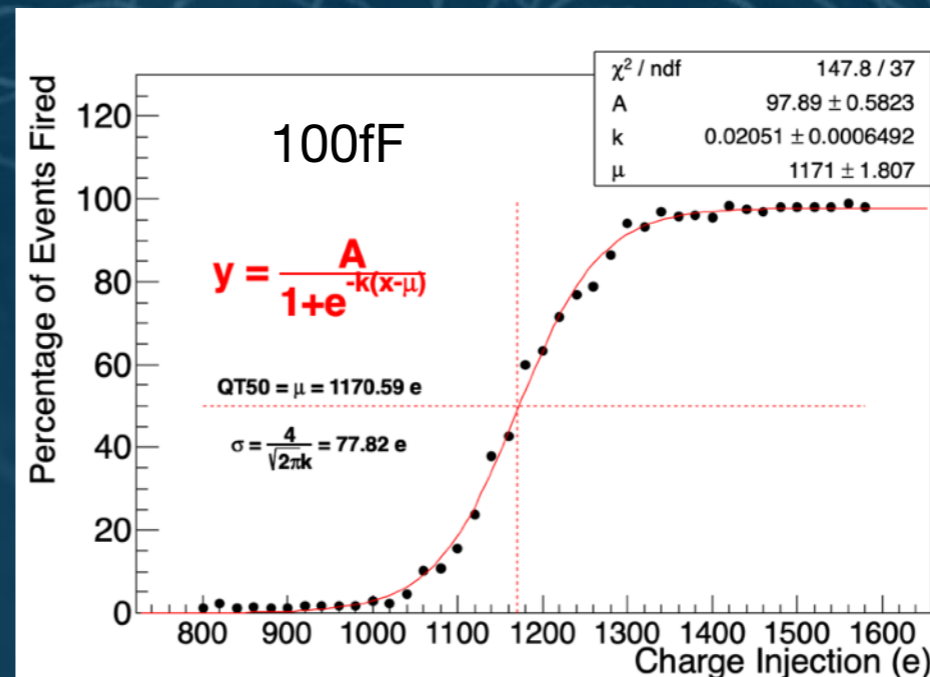
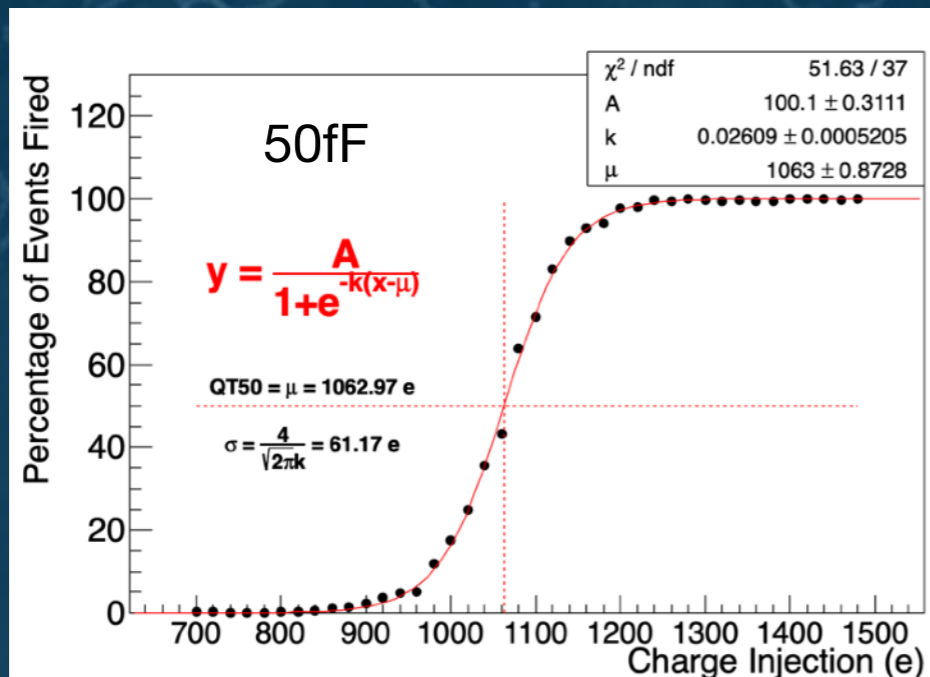
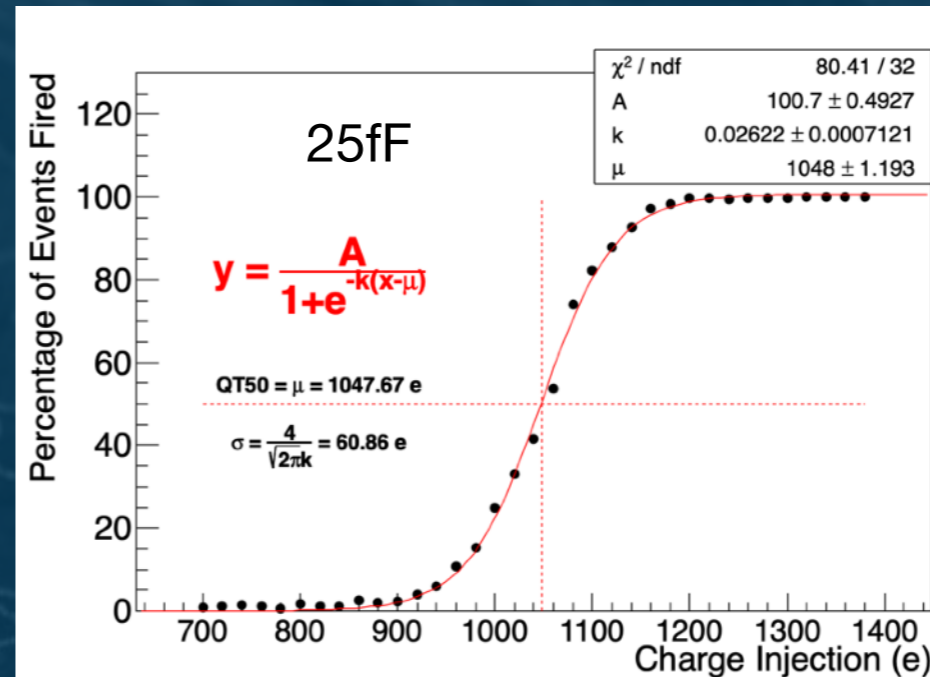
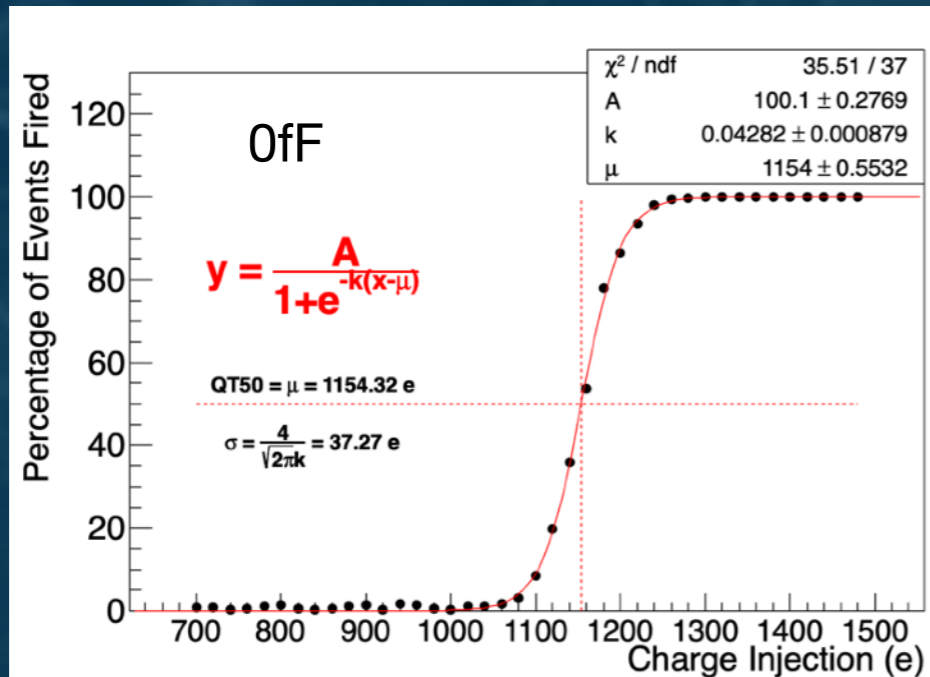


- 2mm x 2mm mini-ASIC submissions
- Pebbles (submitted May 2022)
 - 17 Big Rock AFE channels (4 different Cin Off, 25fF, 50fF, 100fF)
 - High speed CML output driver (10Ghz)
 - LVDS clock receiver
- Metarock (submitted Jul 2023)
 - Improved Big Rock AFE (same channel setup)
 - Added realistic pixel TDC (small area, low power, 40MHz driven) in parallel to characterization TDC
 - PAM-4 driver

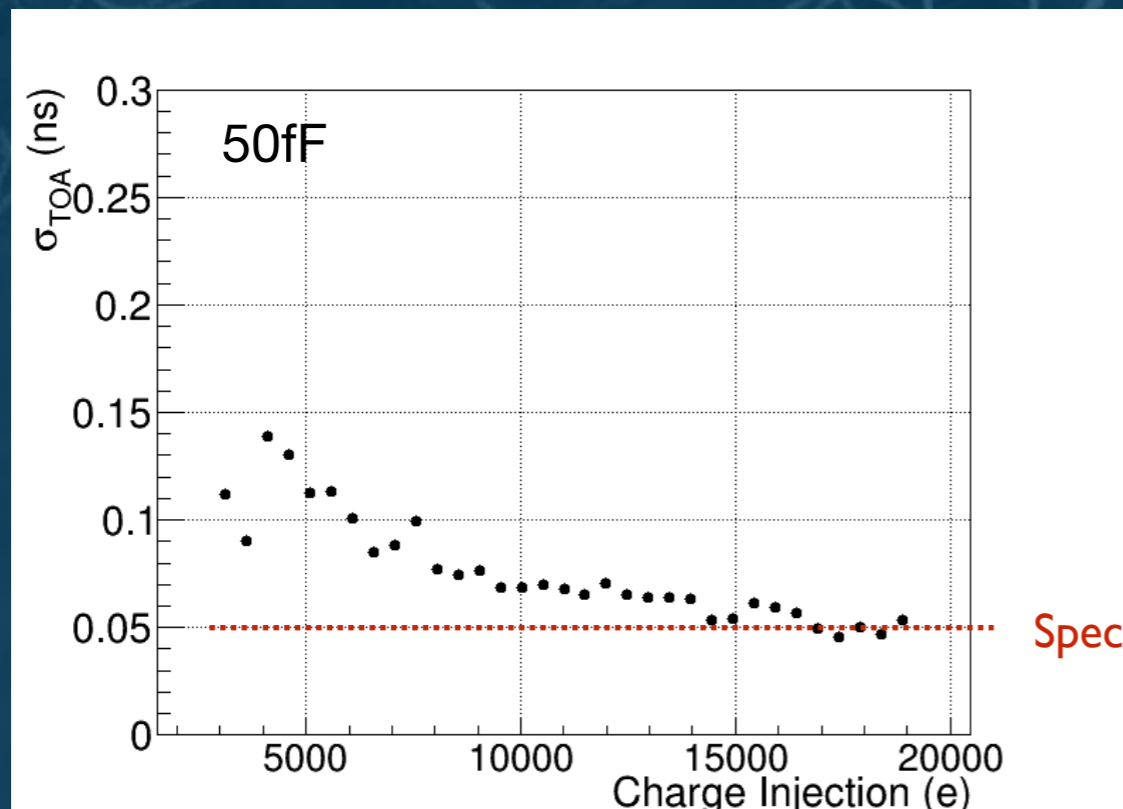
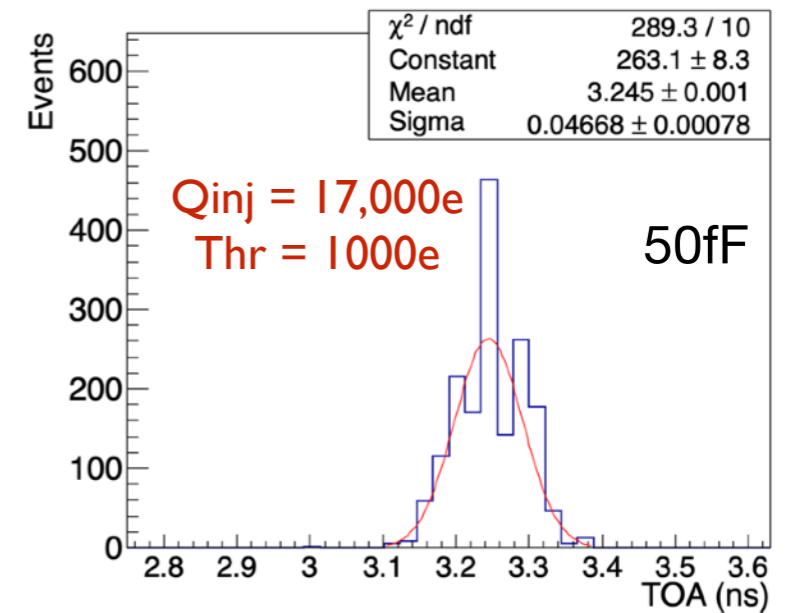
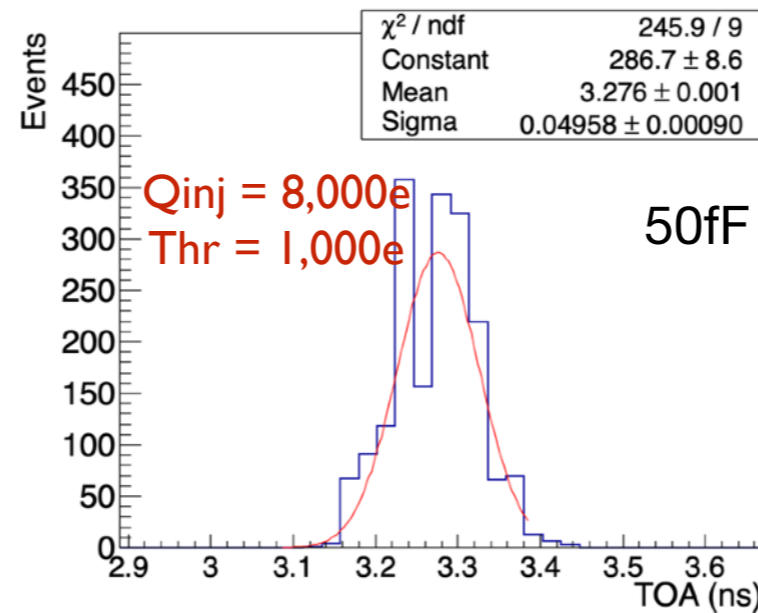
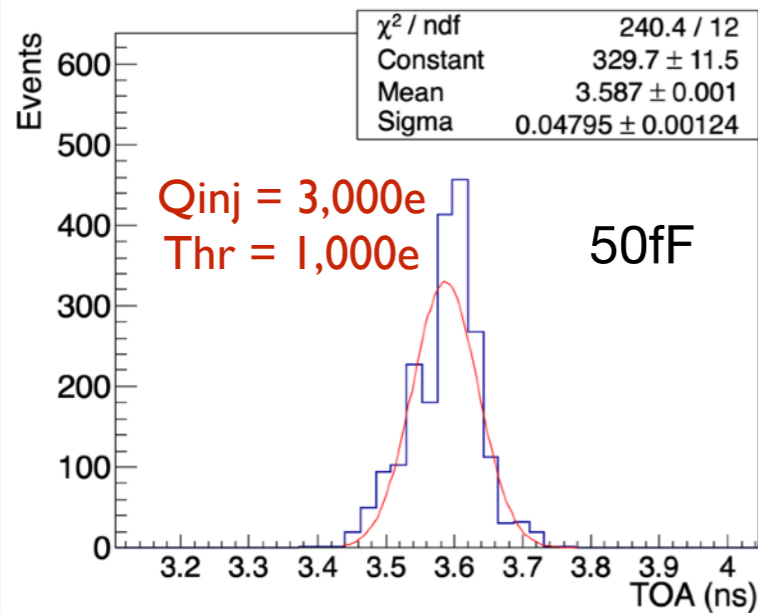




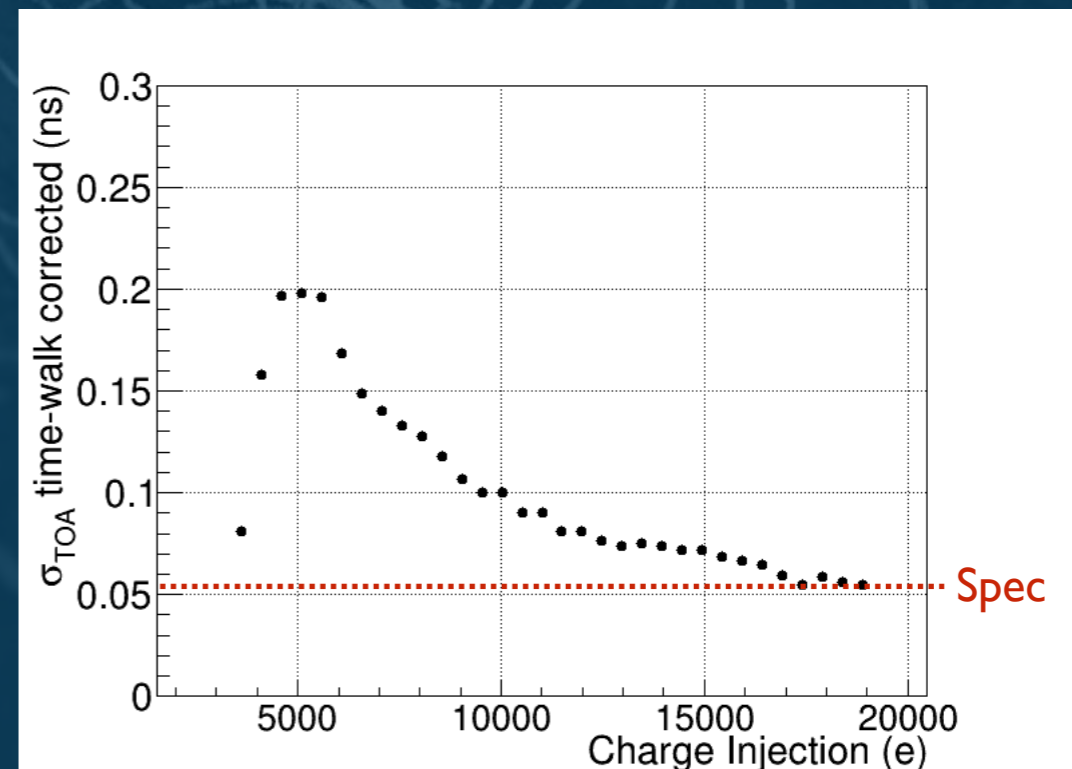
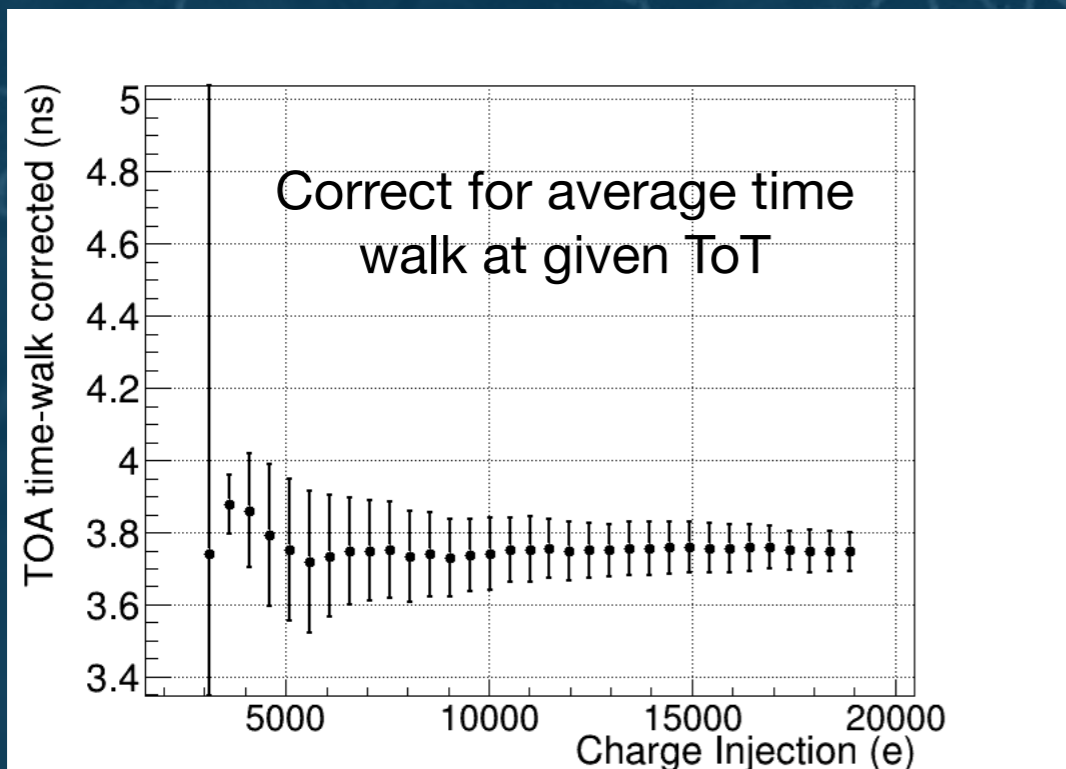
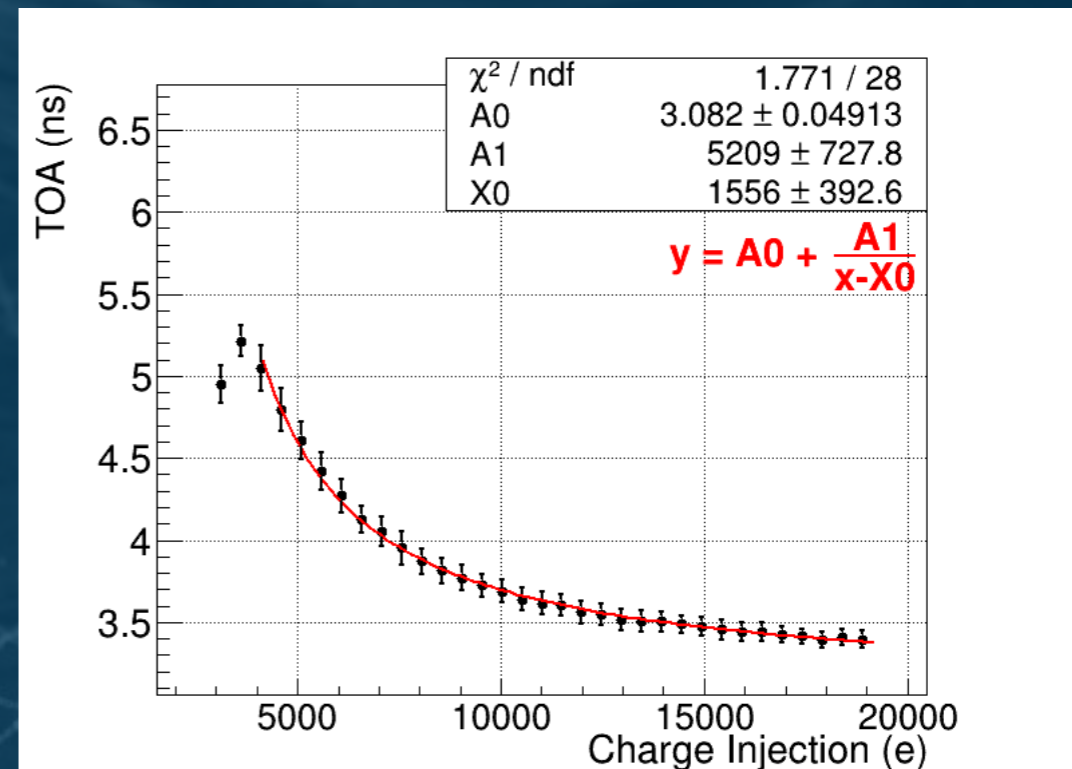
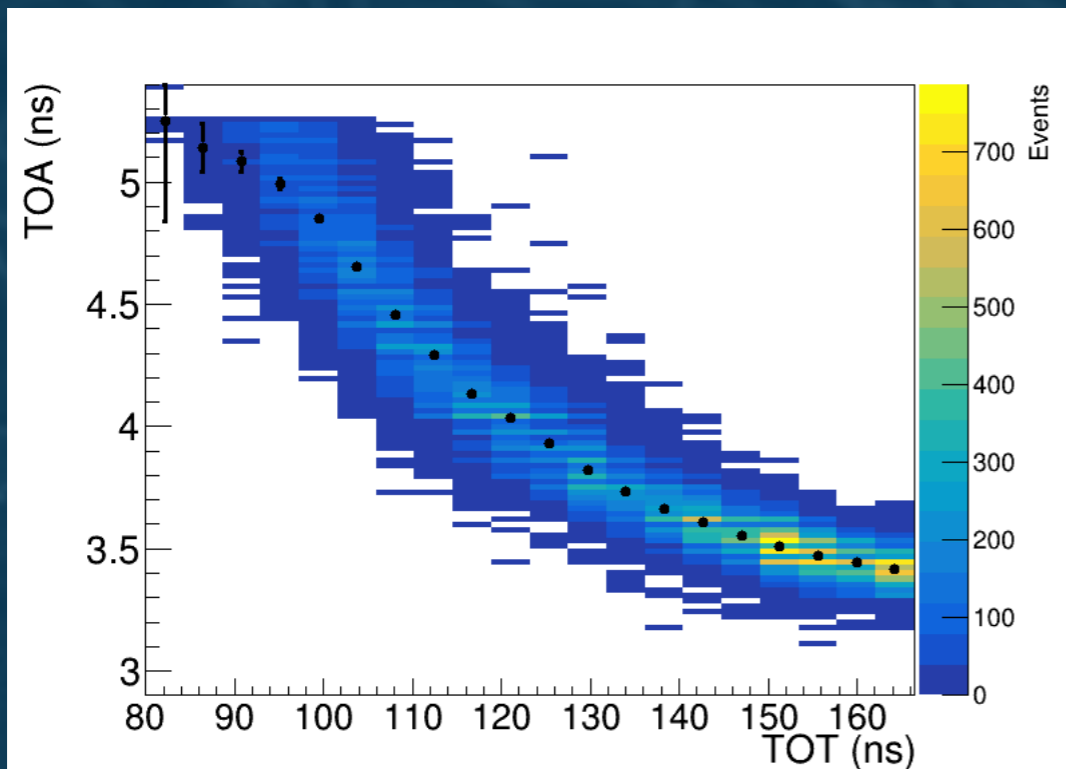
- 128-bit deep delay chain
- 6-bit coarse counter (driven by external clock)
- Rising/Falling edge from AFE freeze delay chain
- If delay chain longer than clock period can calibrate time resolution of TDC



Input Cap (fF)	0	25	50	100
ENC (e)	37	61	61	78



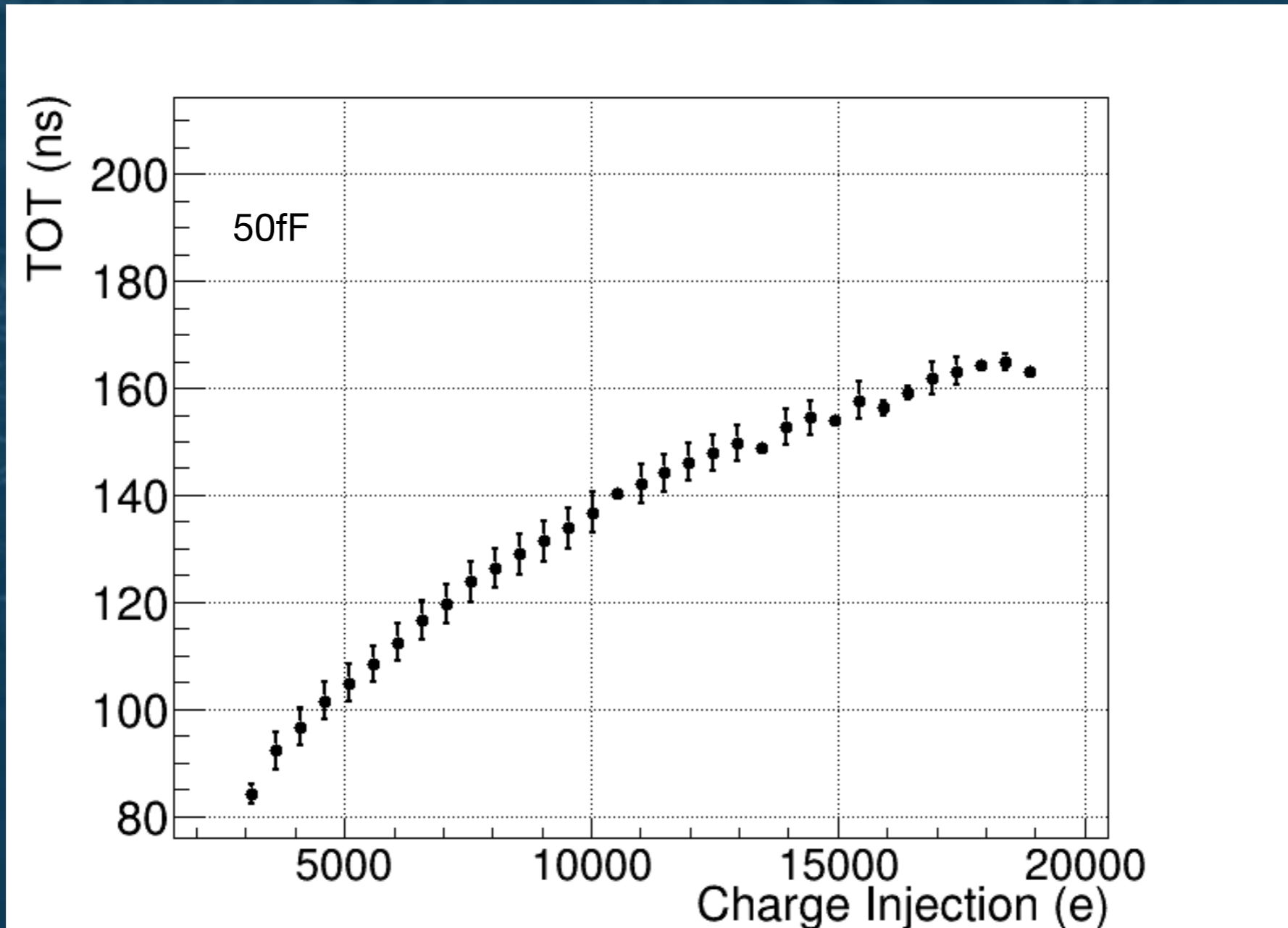
- Room temperature
- Default parameters, not further optimized
- Not corrected for timewalk!
- Meet spec with 0fF C_{in}



- Received first 28nm chip, Pebbles, that implements analog front-end, Big Rock, suitable for a 4D Pixel detector
- Pebbles has on-chip test bench with characterization TDC measured to have ~20ps resolution
- Test results high encouraging, close to meeting spec with out of the box settings
 - Achieved on average 75ps RMS timing resolution with 50fF C_{in}
 - Big Rock AFE has been improved for next submission in Metarock chip
- Excited to see performance of new pixel TDC based on time-stretching once we receive Metarock back from fabrication
 - New pixel TDC is ultra low power (~1uW) and small <math><15\mu\text{m} \times 15\mu\text{m}</math> and driven with 40MHz clock



Backup



Tunable via CSA feedback current