Contribution ID: **63** Type: **Oral**

SiGe integrated chip readout for fast timing

Tuesday, 7 November 2023 14:30 (15 minutes)

Advances in timing detector technology require new specialized readout electronics. Applications demand high rep rates, below 10 ps time of arrival resolution and, low power. A possible path to achieve O(10 ps) time resolution is an integrated chip using Silicon Germanium (SiGe) technology. Using DoE SBIR funding, Anadyne, Inc. in collaboration with UC Santa Cruz has developed a prototype SiGe front end readout chip optimized for low power and timing resolution (0.6 mW/channel, 10 ps of timing resolution for 8 fC). In this contribution the ASIC performance simulation and the results from the first prototype run will be shown.

Early Career

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Session Classification: RDC4

Track Classification: RDC Parallel Sessions: RDC4: Readout and ASICs