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Front-end Application Specific Integrated Circuits (ASICs) in 65 nm CMOS for Charge and Light Readout

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In this talk, we present the progress on development of CMOS-based front-end application-specific integrated circuits (ASICs) for charge and light readout undertaken at Brookhaven National Laboratory. This design evolves from the LArASIC chip manufactured in 0.18 μm, that has been selected for charge readout in the liquid argon time protection chamber (LArTPC) in the phase I of DUNE. LArASIC is the first component in a 3-ASIC readout chain, realizing amplification with transformation of charge to a pulse-shaped voltage waveform. DUNE explores neutrino oscillations, interactions and transformations and is carried out at liquid argon temperatures (i.e., 87 K). The efforts aim at translation and introduction of the required modifications of the legacy design to a scaled CMOS technology, i.e., 65 nm, that can be used in future experiments. The front-end ASIC is designed to have two amplification stages with a programmable gain followed by a 5th order semi-gaussian filter for pulse shaping, suitable to operate at cryogenic temperatures, while it also suits testing at room temperature. We will discuss the design choices we make for the 65 nm chip that enable readout with variable pulse peaking times in the long, i.e., 0.5-2 μs, and short 10 ns-100 ns range within a power budget of 10 mW with an ENC less than 500 electrons RMS with the input capacitance on the order of tens to hundreds of pico farads. Along with exploiting the benefits of transistor scaling and improved transistor f_T to achieve the above-mentioned goals, we make use of I^2C based programmability to create a more robust and flexible design. The targets for this development are such as light/charge readout in Far Detector (FD) 3/4 in phase II of DUNE, silicon based active target and LXe calorimeter in PIONEER, light readout in nEXO, etc.

Early Career

Yes

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