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U.S. DEPARTMENT OF ENERGY

# Front-end Application Specific Integrated Circuits (ASICs) in 65 nm CMOS for Charge and Light Readout

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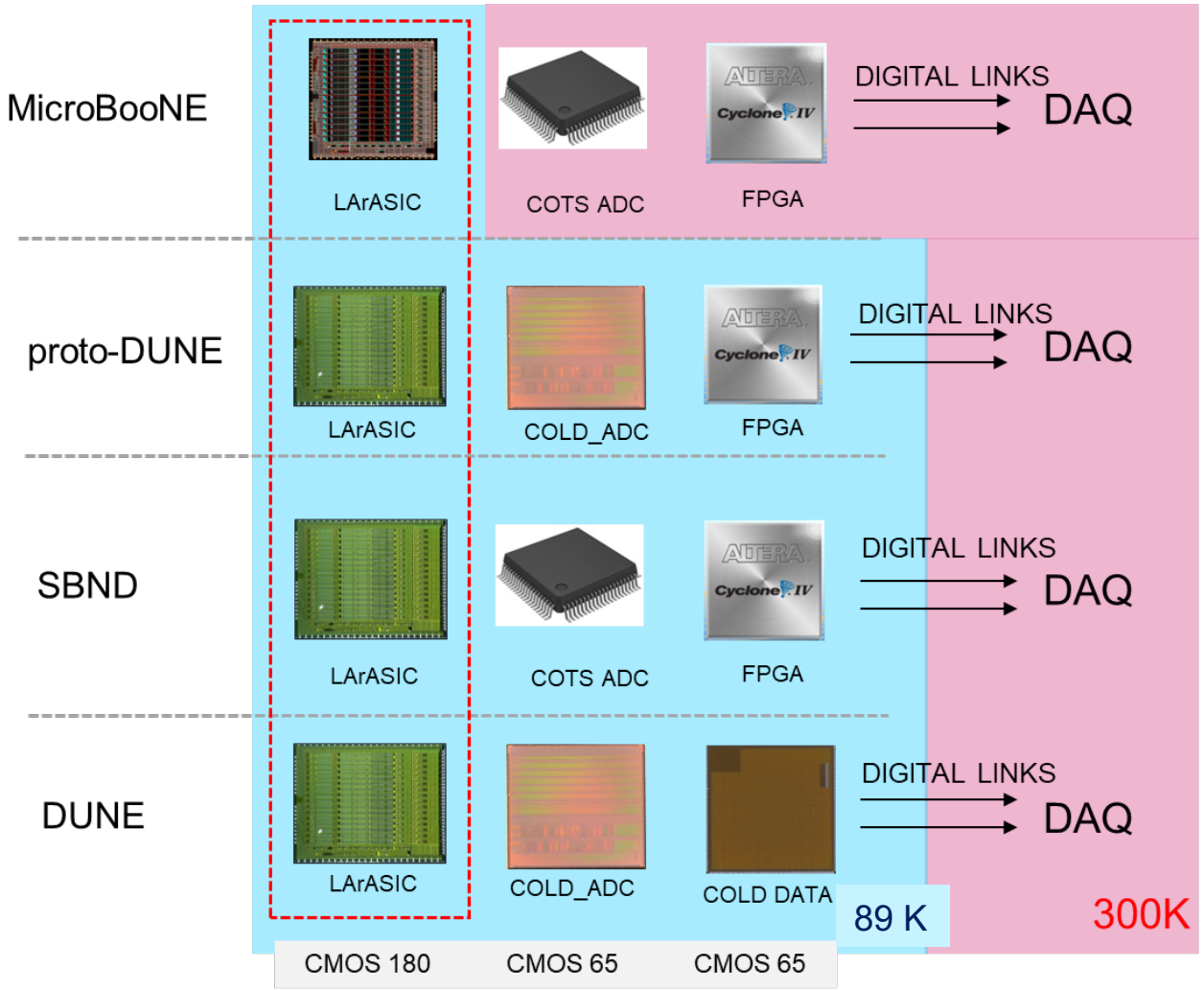
# Status of Front-end ASICs




**3 ASICs vs. 1 ASIC solution:**

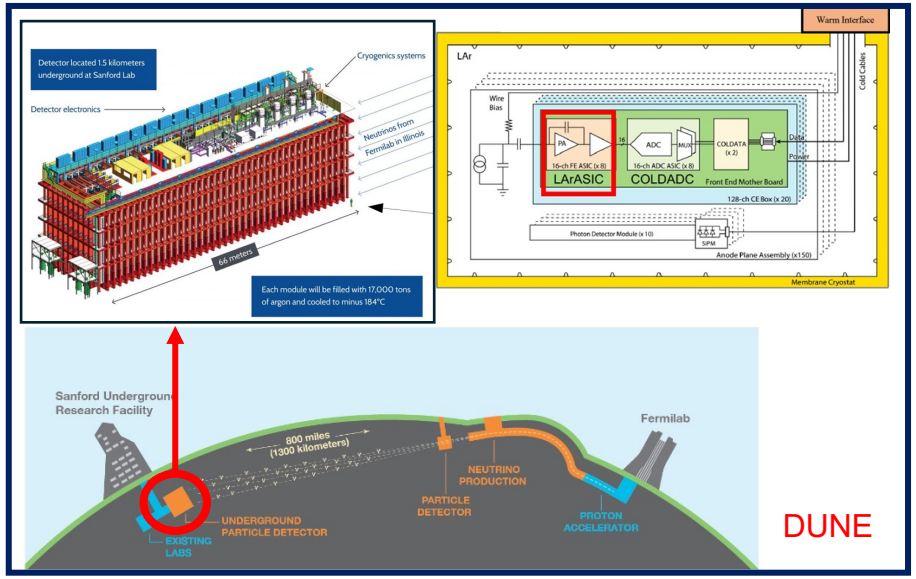
- Initially two readout options were proposed:
  - 3 ASICs vs. 1 ASIC
    (idea of building 1 ASIC, combining FE/ADC/transmission brought in 2016 and included as parallel path of development)
- Evolutionary development MiCroBooNE → DUNE led to the 3 ASIC solution that:
  - Helped perfect the FE (through multiple iterations)
  - Allowed debugging (procedure for ADC calibration)
  - Allowed optimization

**Currently in development: CHAMPS (CHarge AMPlifer + Shaper -> LArASIC translated to 65 nm + additional features)**

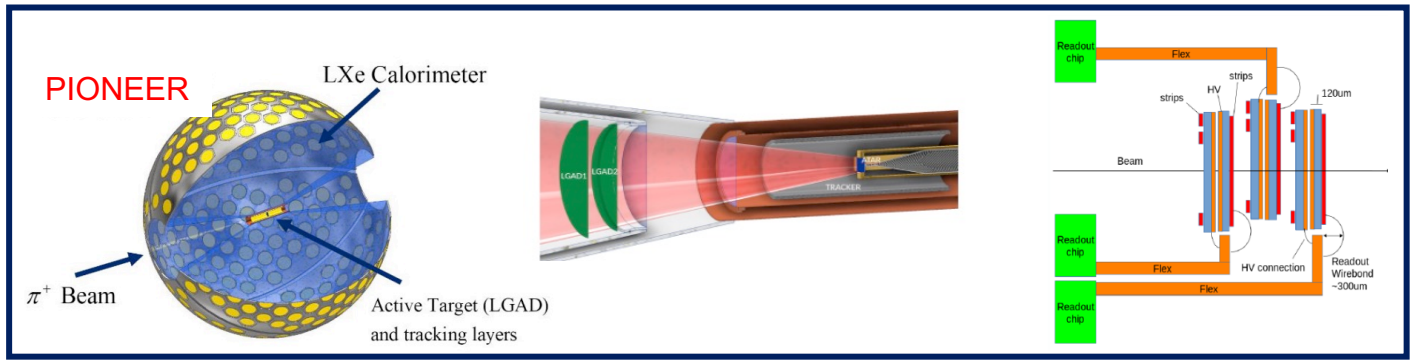
*About a decade of development*

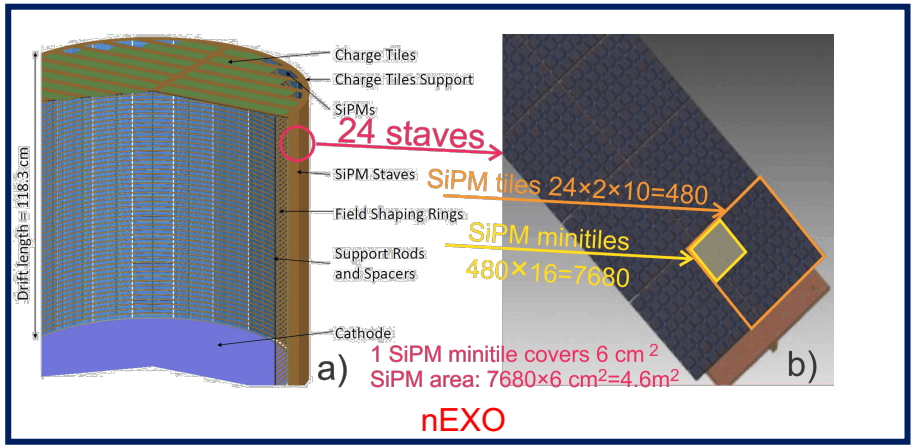
# Targets for CHAMPS

| Experiment | Temperature | Detector Capacitance | Shaping Time | Noise | Dynamic Range |
|---|---|---|---|---|---|
| **DUNE FD 3/4 charge readout** | 89 K – 300 K | 150 pF – 200 pF | 250 ns – 2 µs | 500 $e^-$ at 87 K | 10 bits |
| **nEXO light readout** | 160 K – 300 K | 5 nF | 1 µs | 0.1 $pe^-$ at 160 K | 10 bits |
| **PIONEER** | 160 K – 300 K | 20 pF | 20 ns | 570 $e^-$ at 160 K | 10 bits |



DUNE



nEXO

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# Planned specifications

| | LArASIC (P5B) | | | | CHAMPS250 | CHAMPS10 |
|---|---|---|---|---|---|---|
| Technology | 180 nm CMOS – 1-poly, 6-metal, MiM cap, sil blk resistors | | | | 65 nm CMOS: 1-poly, 9-metal | 65 nm CMOS: 1-poly, 9-metal |
| Supply Voltage | 1.8 V | | | | ✓ | ✓ |
| Temperature Range | 77 – 300 K | | | | ✓ | ✓ |
| Number of Channels | 16 | | | | ✓ | ✓ |
| Max Single-Ended Output Swing | 1.4 V peak to peak (0.2 – 1.6 V) | | | | ✓ | ✓ |
| Gain Selection (mV/fC) | 4.7 | 7.8 | 14 | 25 | ✓ | ✓ |
| Full-Scale Input Charge (fC) | 300 | 180 | 100 | 56 | ✓ | ✓ |
| Baseline selection | 200 mV (collection mode) | | 900 mV (induction mode) | | ✓ | ✓ |
| Charge Preamplifier Polarity | Negative (collection mode) | | Bipolar (induction mode) | | ✓ | ✓ |
| Adaptive-Reset Current Selection (nA) | 0.1 | 0.5 | 1 | 5 | ✓ | ✓ |
| Shaper Peaking Time Selection (µs) | 0.5 | 1 | 2 | 3 | 250 ns – 2 µs | 10 ns – 250 ns |
| Output Coupling | AC (100 µs HPF time-constant) | | DC | | ✓ | ✓ |
| Output Selection | Shaper | SE buffer | SEDC buffer | | ✓ | ✓ |
| Total Channel Settings | 1024 | | | | TBD | TBD |
| Integrated Test Capacitor | 200 fF | | | | TBD | TBD |
| Temperature Sensor | 0.8728 V @ 25°C + 2.868 mV/°C | | | | ✓ | ✓ |
| Integrated Pulse Generator | 6-bit DAC based | | | | ✓ | ✓ |
| Configuration Control | SPI interface with 144 register bits | | | | I²C interface | I²C interface |

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# LArASIC – status

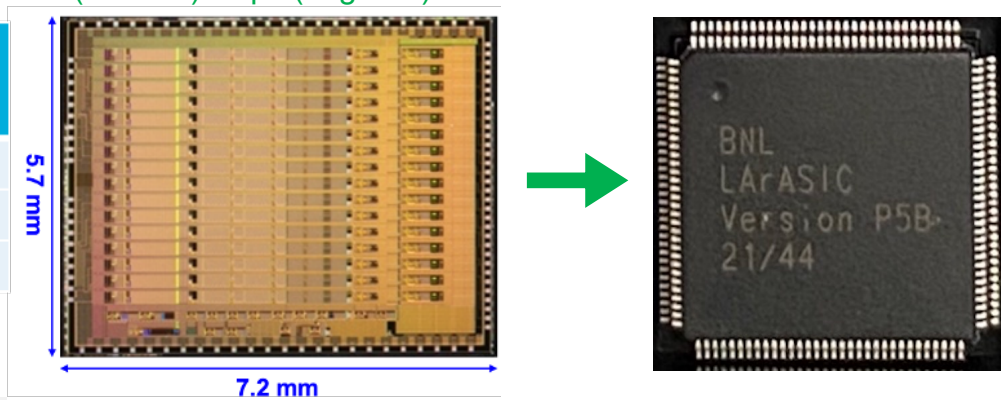
LArASIC MPW met all the DUNE requirements → fabricated ~1800 P5 and 1800 P5B (180 nm) chips (eng. run) for ProtoDUNE II

| LArASIC Chips | Temp. | Tested Chips# | Good # (All channels are normal) | Yield |
|---|---|---|---|---|
| P5 | RT | 49 | 49 | 100 % |
| **P5B** | **RT** | **1642** | **1635*** | **~99.57 %** |
| **P5B** | **LNT** | **317** | **317** | **100 %** |

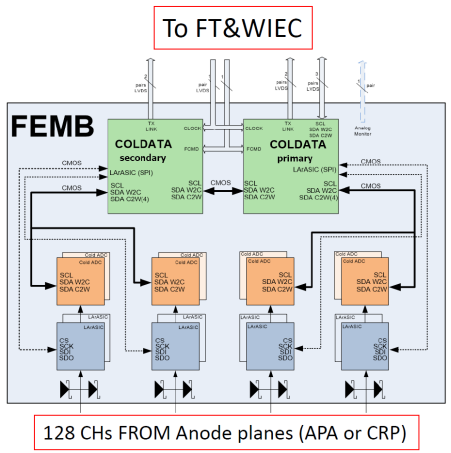
P5B has improved input ESD protection compared to P5

*Only 1 out of 16 channels in each of the two chips are non-functional

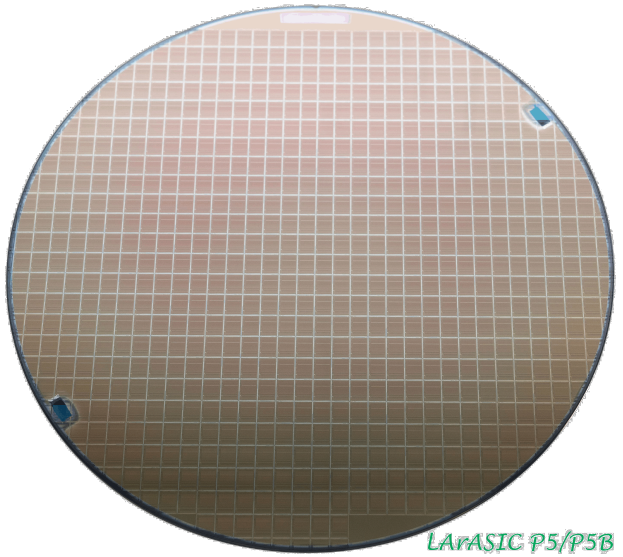
>6 months ago, now more statistics is available




**LArASIC performance with differential interface**




24 FEMBs arrived at CERN for ProtoDUNE-II installation




250 wafers LArASIC production run for DUNE 75k P5 and 75k P5B chips

8” wafer with 610 LArASICs P5 and P5A(B) w. increased ESD protection

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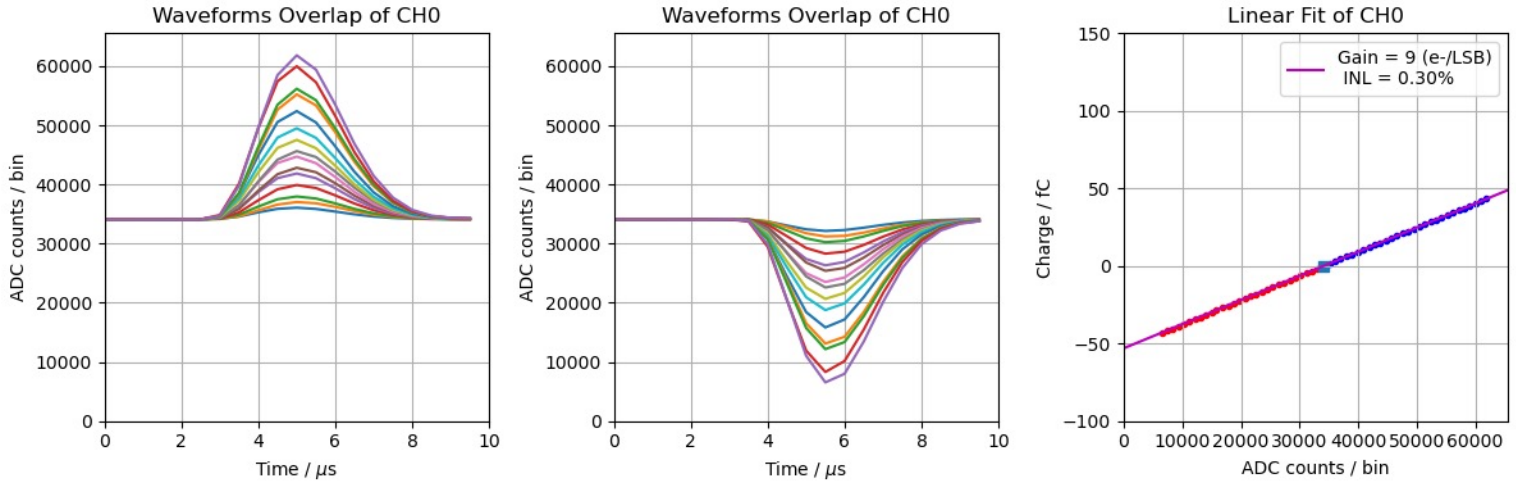
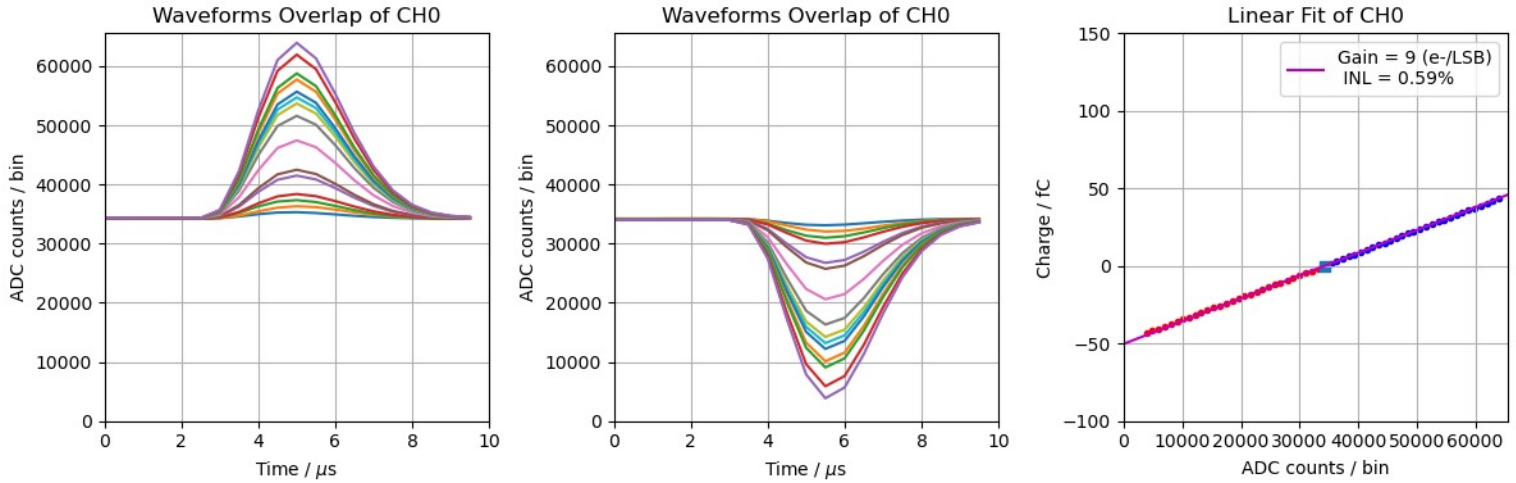
# Measured characteristics (LArASIC P5)

Charge gain = 9, 900mV baseline, 500pA, $T_p$ = 2 $\mu$s, ADC 16-bit mode

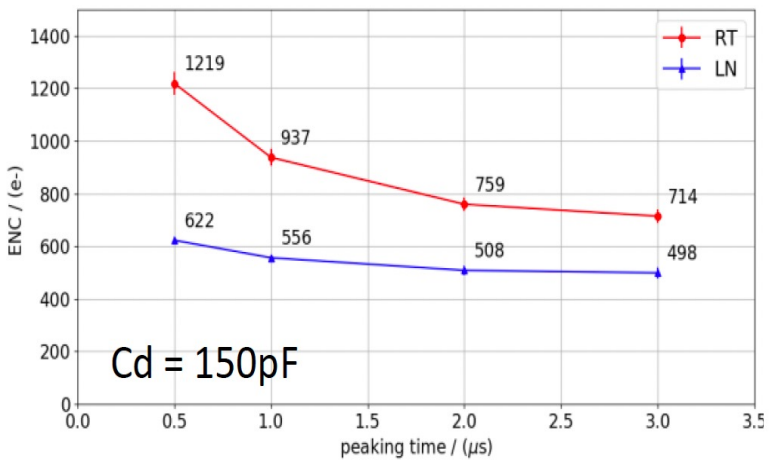
RT



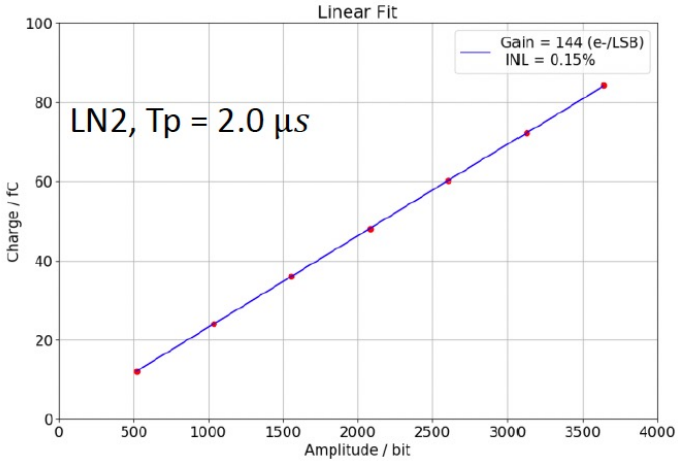

LN2



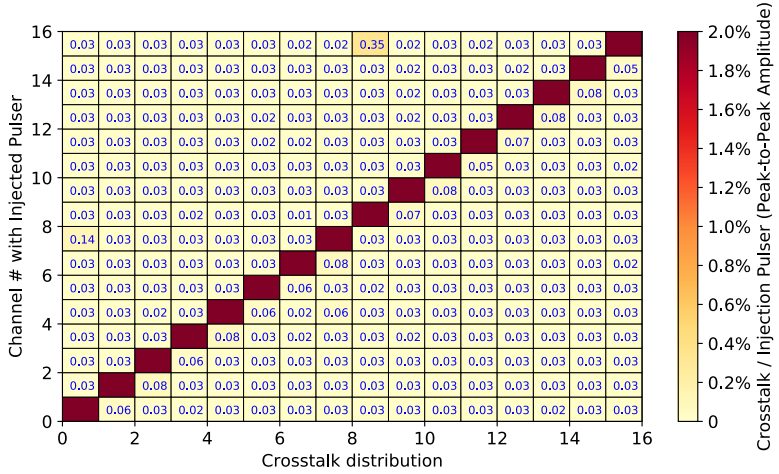
# Measured characteristics (LArASIC P5)




Low Noise

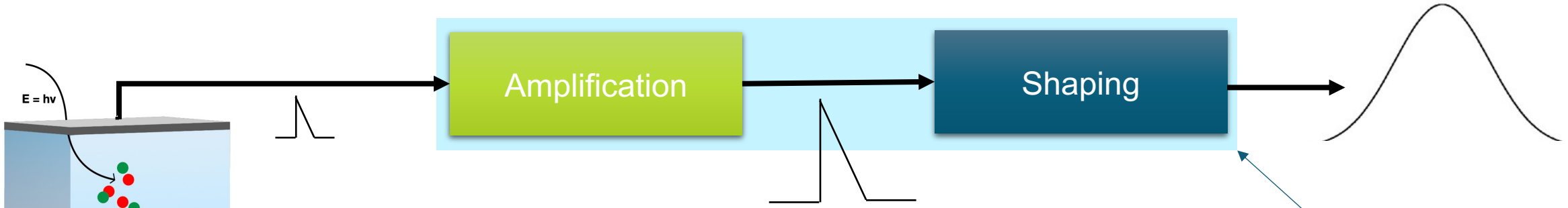



High Linearity



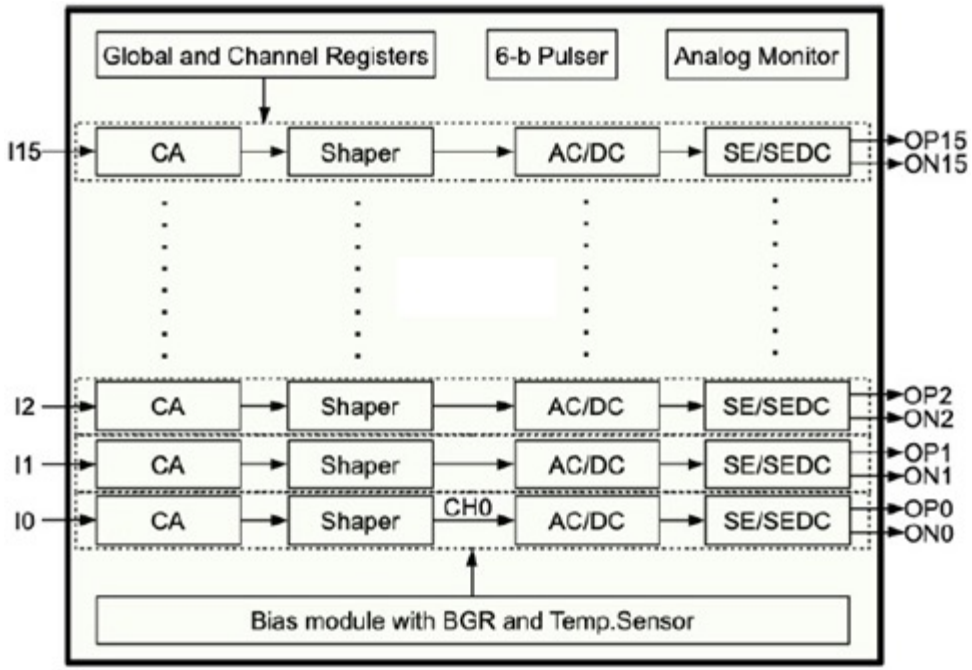

Low Crosstalk

# CHAMPS status & overview




- Input charge converted to output voltage
- Output voltage amplitude proportional to particle energy

**Schematic level design in 65 nm completed with 3 mW power consumption**

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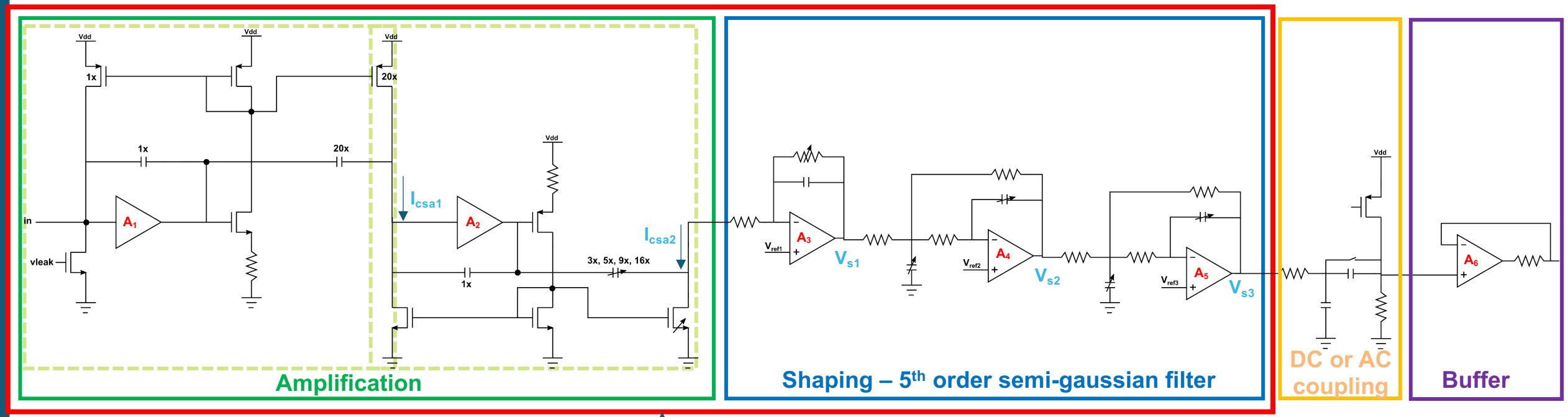
# Circuit implementation




**Schematic level design in 65 nm completed with 3 mW power consumption and programmable shaping times of 250 ns, 500 ns, 1 µs and 2 µs**

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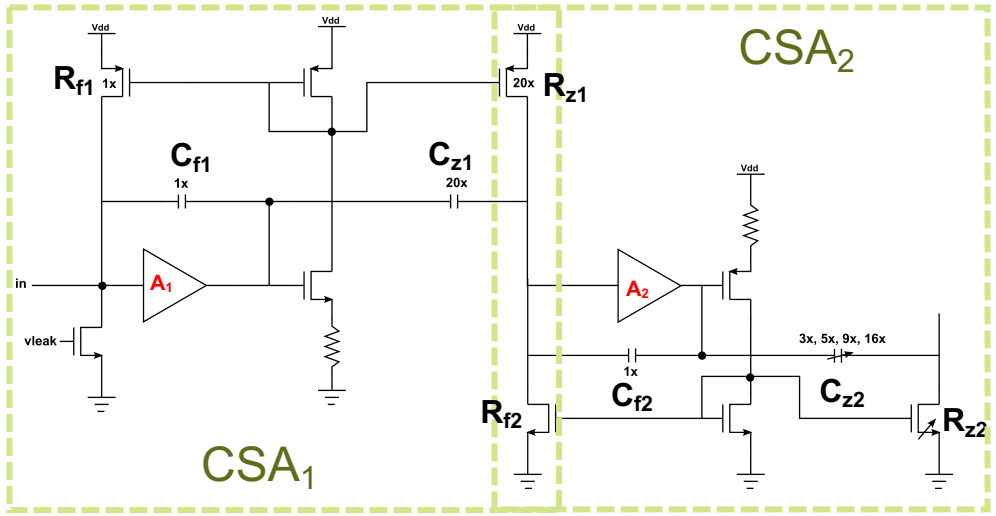
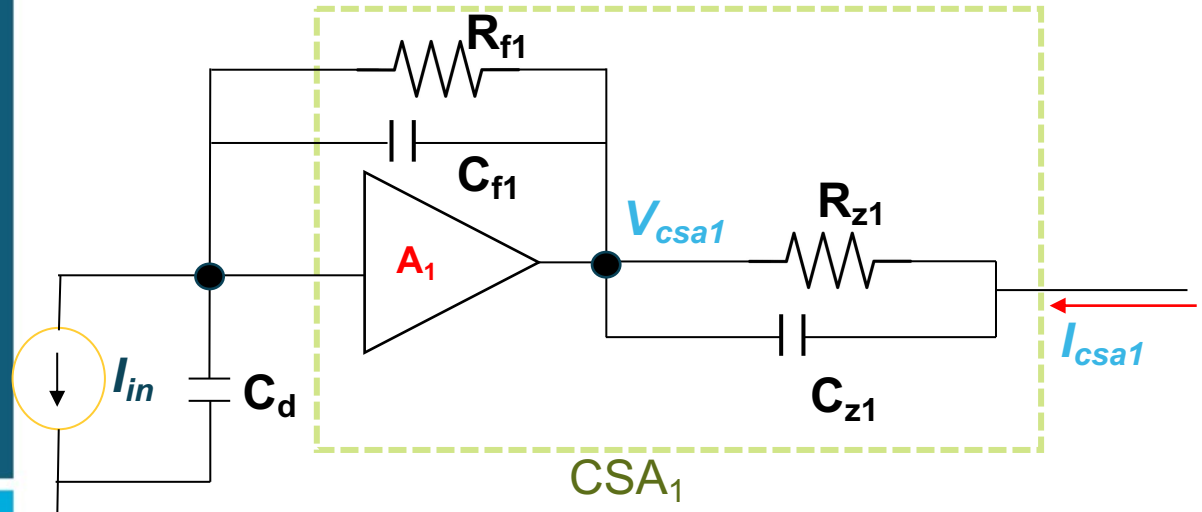
# Charge Sensitive Amplifier design




- Charge amplifiers use current-mirror based adaptive continuous reset
- $A_1$ and $A_2$: 3-stage amplifiers (> 100 dB gain each, bandwidths of 10 MHz and 20-50 MHz)
- Pole zero cancellation ($C_fR_f = C_zR_z$) ensures fast $I_{csa1}$ pulse and prevents baseline drift

$$I_{csa1}(s) = \underbrace{I_{in}(s)\frac{R_{f1}}{(1+sC_{f1}R_{f1})}}_{V_{csa1}}\frac{(1+sC_{z1}R_{z1})}{R_{z1}}$$

- $C_{z1} = 20C_{f1}$ , $R_{z1} = (1/20)R_{f1}$ , charge gain provided by $CSA_1 = 20$
- $C_{z1} = (3 \text{ or } 5 \text{ or } 9 \text{ or } 16)C_{f1}$ , $R_{z1} = (1/3 \text{ or } 1/5 \text{ or } 1/9 \text{ or } 1/20)R_{f1}$ , charge gain (programmable) provided by $CSA_2 = 3$ or 5 or 9 or 16

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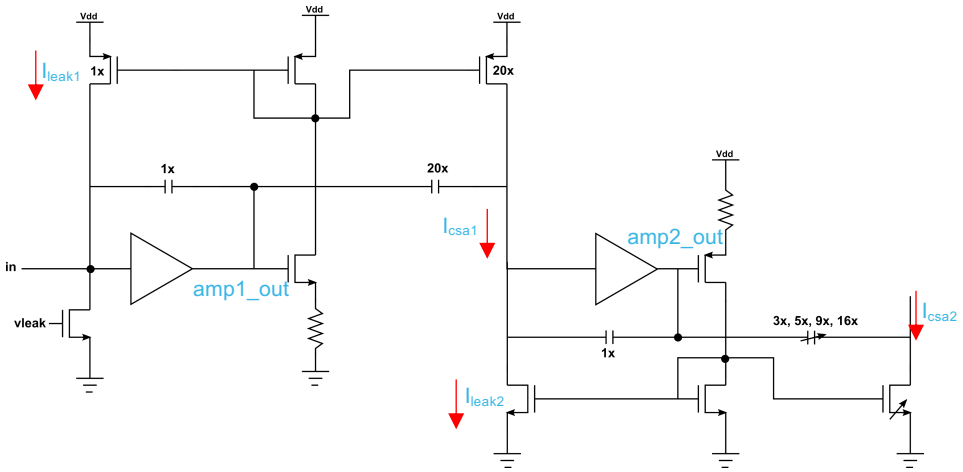
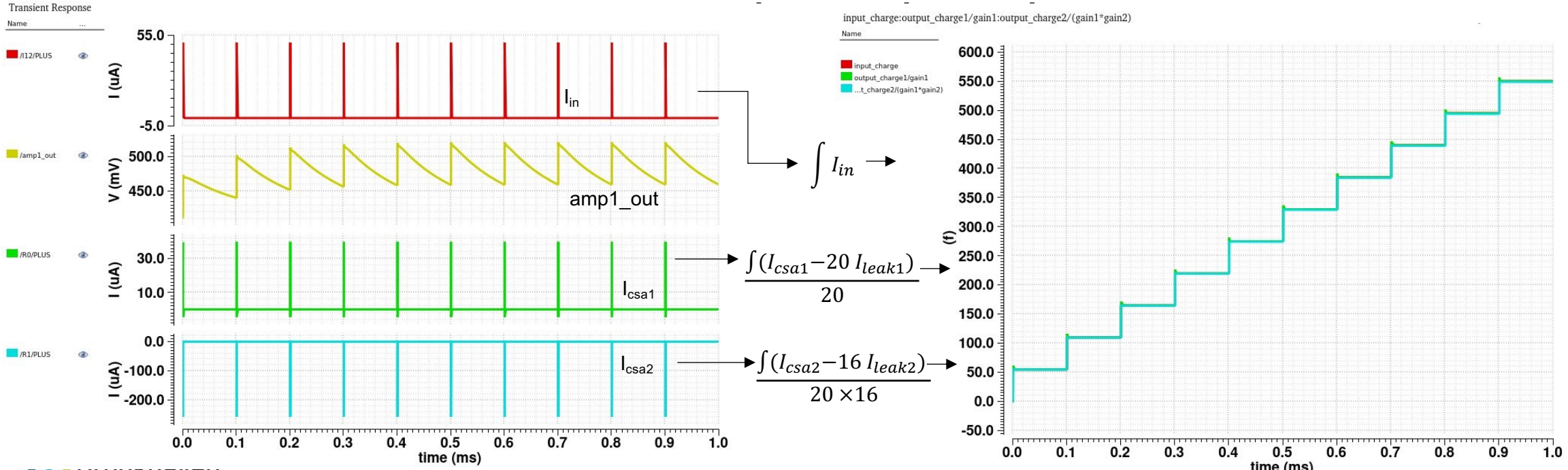
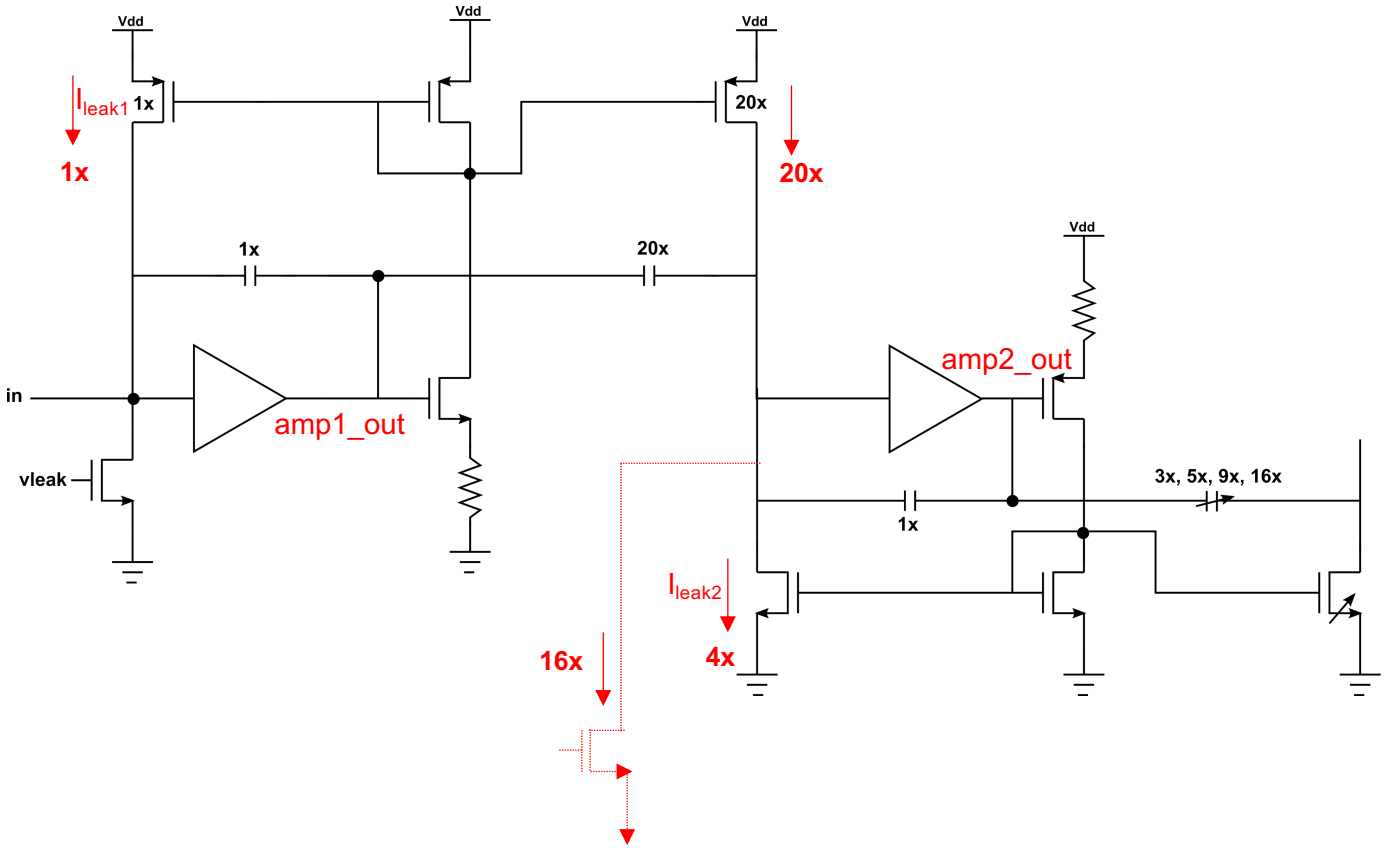
# $CSA_1$ and $CSA_2$ charge multiplication check



# $CSA_2$ reset current subtraction




- Reset Quiescent Current (RQI) subtraction for $CSA_2$ to be implemented in CHAMPS
- Prevents propagation of leakage current and corresponding baseline shift
- To be made programmable (2-3 bits) with digital assistance independently for each channel
- Suitable for applications that have high leakage current and involve DC coupling

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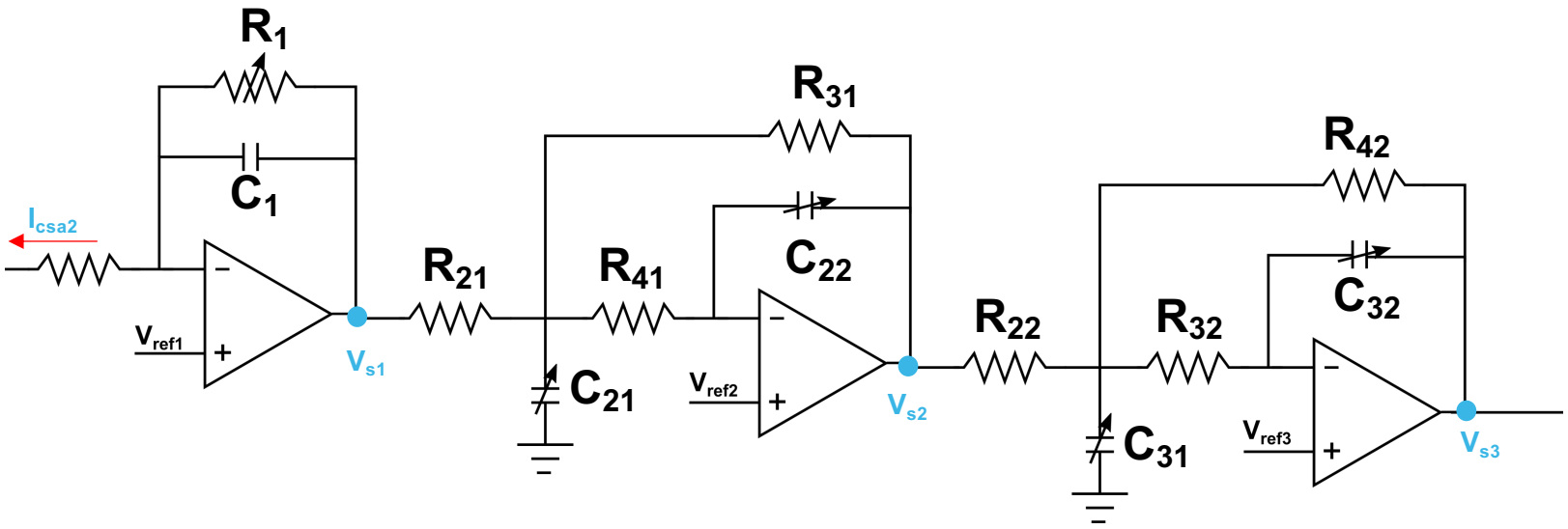
# Shaper design




- Implemented shaper is a 5th order semi-gaussian filter with complex conjugate poles
- $V_{csa2}$ output is a fast pulse, poses stringent requirements on peak capturing circuit (must be fast and accurate)
- Shaper slows down the variations near signal peak
- (Nearly) equal rise and fall times maximize the output signal amplitude for a given pulse duration

$$V_{s1}(s) = I_{csa2}(s)\frac{R_1}{(1+sC_1R_1)}$$

$$V_{s2}(s) = V_{s1}(s)\frac{\frac{1}{R_{21}R_{41}C_{21}C_{31}}}{s^2 + s\left(\frac{1}{R_{21}C_{21}} + \frac{1}{R_{31}C_{31}} + \frac{1}{R_{41}C_{21}}\right) + \frac{1}{R_{31}R_{41}C_{21}C_{31}}}$$

$V_{s3}(s)$ is similar……

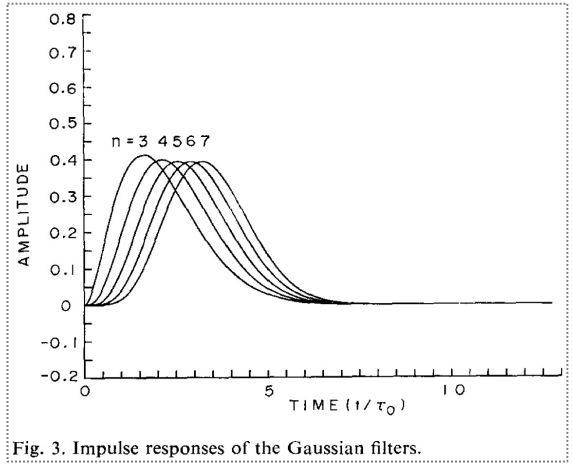


Fig. 3. Impulse responses of the Gaussian filters.

S. Ohkawa, M. Yoshizawa, K. Husimi,
*Direct synthesis of the Gaussian filter for nuclear pulse amplifiers*.

# Noise minimization strategy

$$ENC^2 = (C_d + C_{in})^2 \left( A_w v_n^2 \frac{1}{T_p} + A_f K_f \right) + A_p i_n^2 T_p$$

(Sum of white series noise, 1/f series noise and parallel noise components)

**Input stage transistors for $A_1$ implemented using thick oxide (2.5 V) devices in 65 nm to limit leakage current and associated parallel noise**

$$ENC_f^2 = K_f \frac{(C_d + C_g)^2}{C_g} N_f \Rightarrow C_g = C_d$$

$$ENC_w^2 = 4k_B T n \gamma \alpha_w \frac{(C_d + C_g)^2}{g_m(C_g)} N_f \Rightarrow C_g = \frac{1}{3} C_d$$

Input stage transistor sized to have $C_g$ ~ 40 pF, optimal choice for minimizing noise with $C_{det}$ ~ 150 pF with given power budget

| | Minimum allowable transistor length | Input transistor length | Input transistor width |
|---|---|---|---|
| **180 nm** | 180 nm | 270 nm | 20 mm |
| **65 nm** | 280 nm | 400 nm | 24 mm |

Noise in 65 nm (simulated) about 10 % lower than 180 nm

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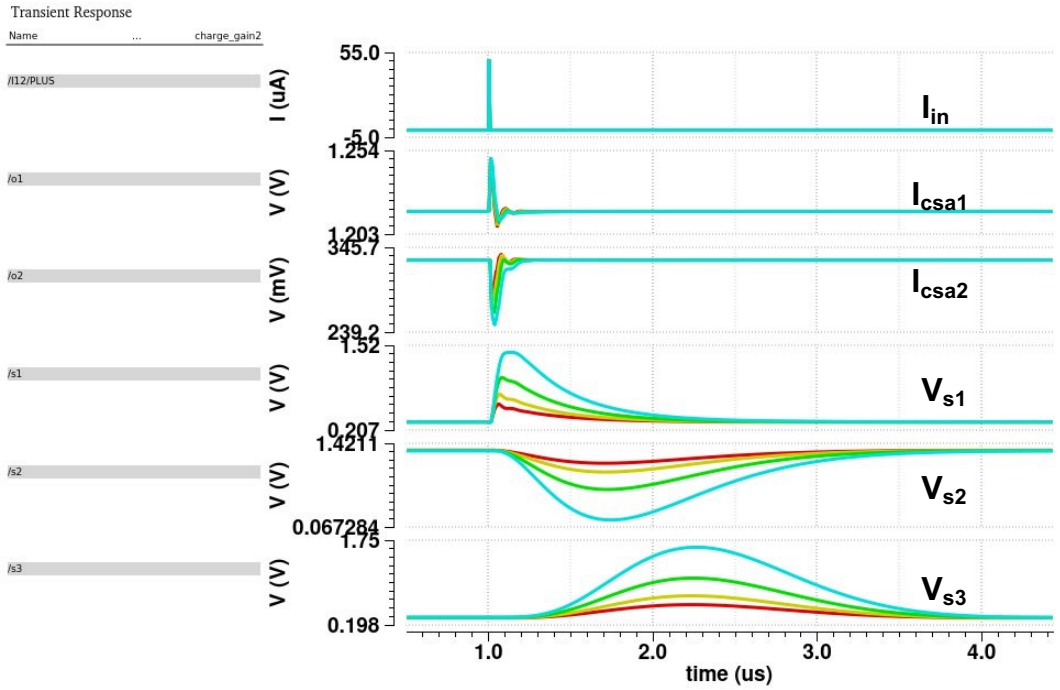
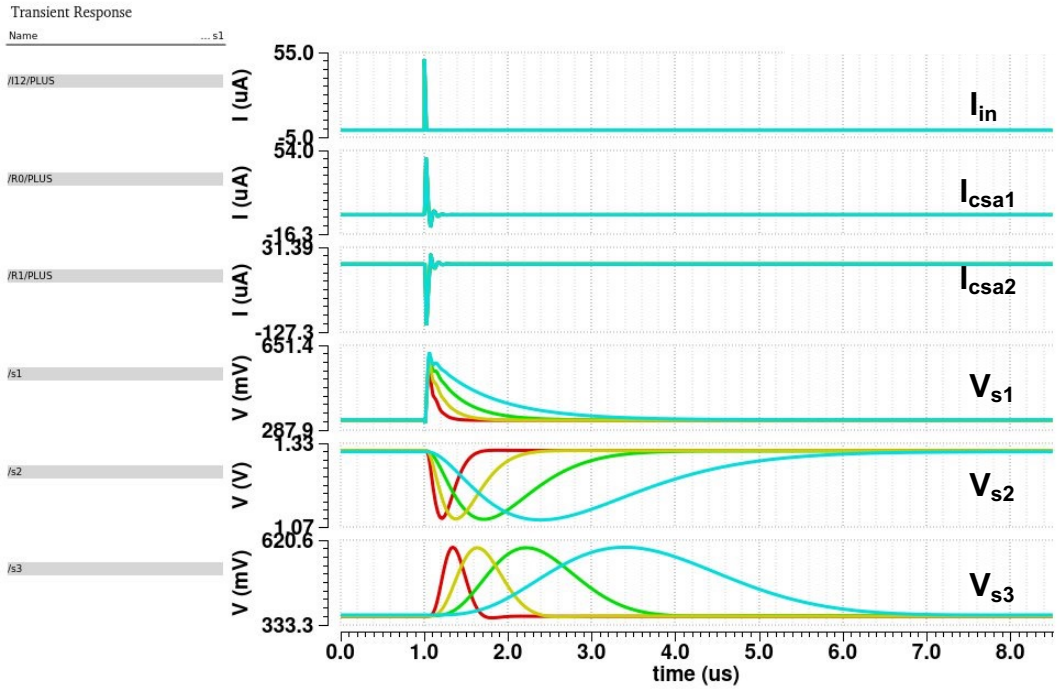
Ref: Angelo Rivetti, Front-End Electronics for Radiation Sensors

# Transient responses

## Variable charge gain (3, 5, 9, 16)




## Variable peaking time (250 ns, 500 ns, 1 µs, 2 µs)

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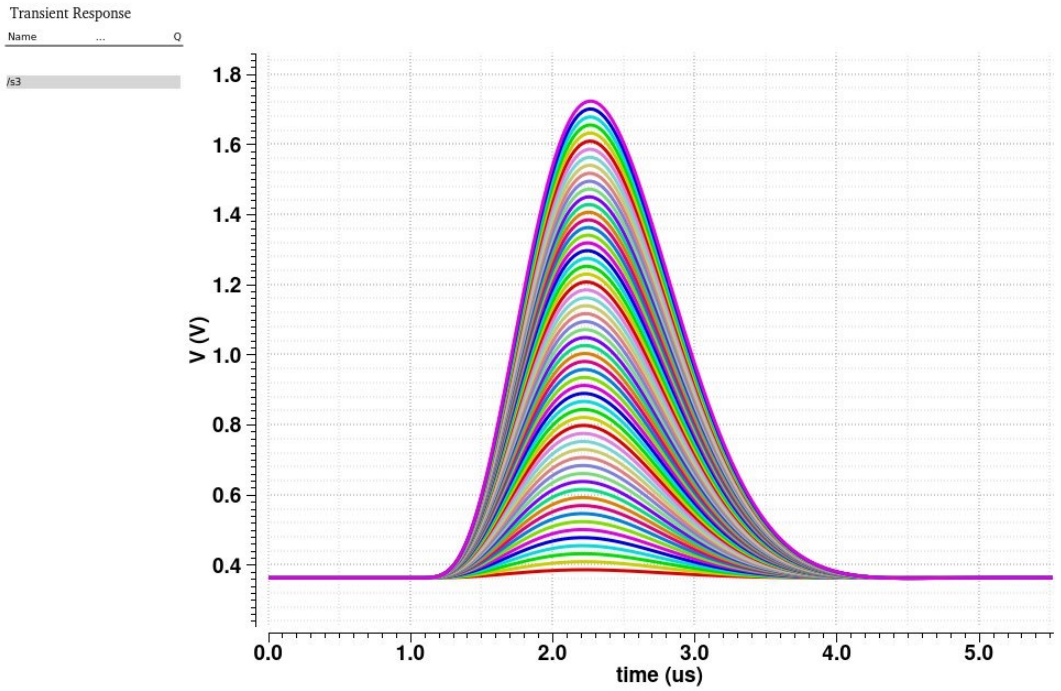
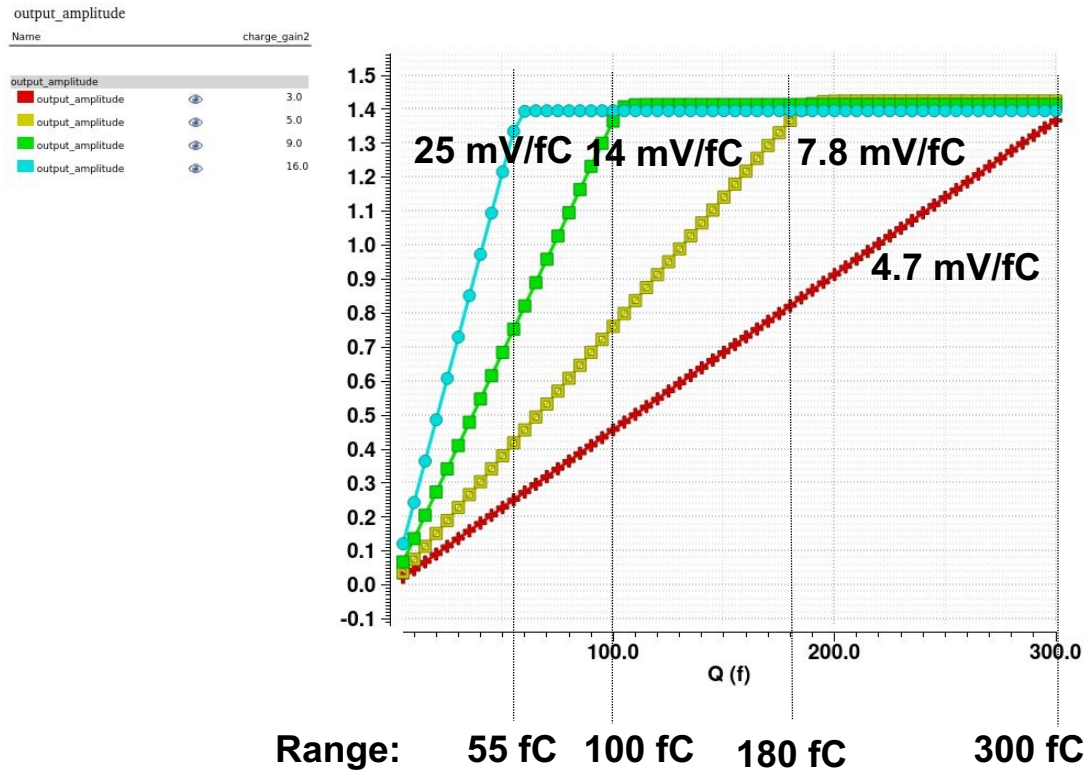
# Linearity characteristics

## Shaper response for charge gain = 3, $T_p$ = 1 $\mu$s




## Output amplitude Vs. input charge




Range: 55 fC 100 fC 180 fC 300 fC



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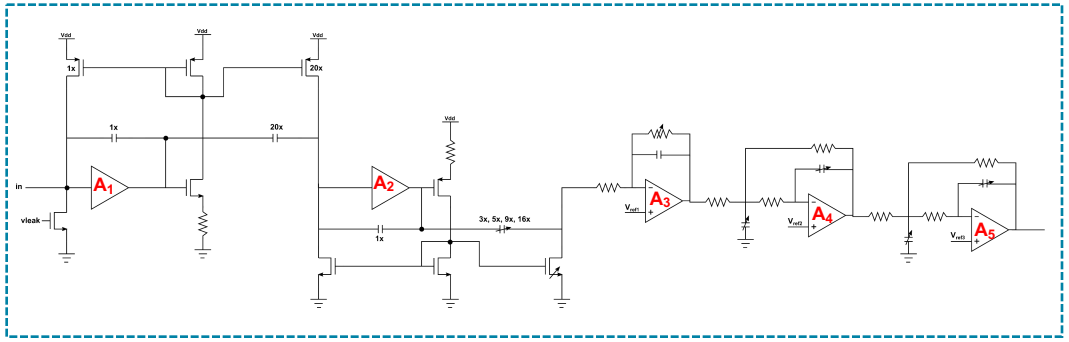
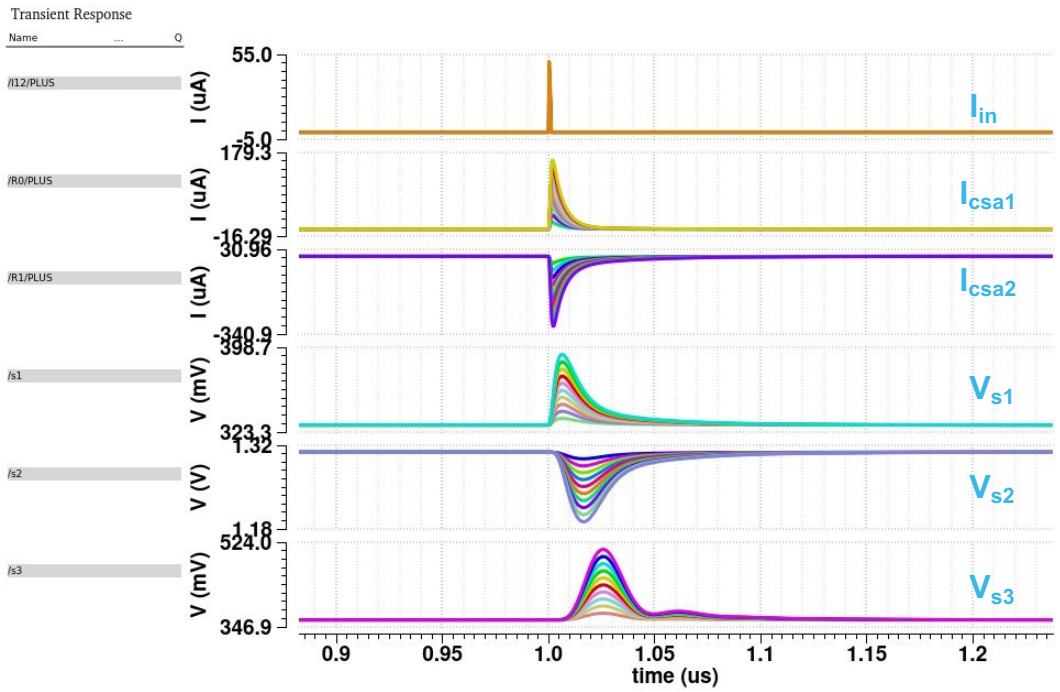
# Plan for CHAMPS10 ( 10 ns ≤ $T_p$ ≤ 250 ns)




- Limited bandwidth of $A_1$ and $A_2$ disallows shaping times < 250 ns
- Currently, amplifiers $A_1$ and $A_2$ implemented as 3-stage amplifiers
- Difficult to achieve higher bandwidth without sacrificing stability
- CHAMPS10 will incorporate topology modification for $A_1$ and $A_2$

Transient response for variable input charge (50 fC – 300 fC) with $A_1$, $A_2$, $A_3$ modeled as ideal VCVS



# Thank you