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Towards 4D tracking: 28nm sub-10ps TDC ASIC design and characterization setup

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4D trackers with ~10ps timing will be transformative at future collider experiments. Timing is crucial for reducing the combinatorial challenge of track reconstruction at extremely high pileup densities, it offers completely new handles to detect and trigger on long-lived particles (LLP), expands the reach to search for new phenomena, and enables particle-ID capabilities at low transverse momentum. At the Muon Collider, the timing information will be essential for reduction of the beam-induced background (BIB).
As one of the critical blocks necessary to enable 4D operation in trackers, we developed a 4-channel sub-10ps Time-to-Digital Converter (TDC) ASIC in the 28nm CMOS technology node. The developed TDC is based on a novel 2D Vernier ring-oscillator structure with embedded sliding-scale technique for conversion linearity improvement that will simplify calibration of the TDCs, especially useful in high-channel count implementations such as 4D trackers.
The core of the TDC architecture is composed of differential voltage-controlled delay cells set at 50ps propagation delay and assembled in a 4-cell ring-oscillator with enable/disable function with programmable starting state. The ring-oscillator, enabled with a START trigger, coupled with a counter and a series of flip-flops that sample the oscillator's state at a STOP-trigger, can perform time-interval quantization with 50ps time-steps and a range of 1.6ns. The feature of having the oscillator starting condition programmable, coupled with pseudo-random selection of the starting point at each measurement cycle, performs the sliding-scale function thus improving the conversion linearity beyond the limits set by mismatches between the delay cells of the ring-oscillator. To reach a sub-10ps resolution, the 50ps time-step of the previous structure is interpolated by a factor of 8 using a second ring-oscillator with delay cells set to 56.25ps propagation delay and enabled by a second STOP signal. Each step of the first ring-oscillator is sampled in correspondence of both rising and falling edges of the second ring-oscillator by a 2D array of flip-flops. This 2D Vernier structure reaches a resolution equal to the difference of propagation delays of cells in the two oscillators, i.e. 6.25ps. Compared to a traditional Vernier TDC, the 2D configuration allows faster conversion times and easily extendable measurement range. Both ring-oscillators implement the programmable starting state, i.e. sliding-scale, thus improving the linearity of the overall conversion.
The ASIC is composed of 4 measurement channels, each receiving one common START and two STOP signals (one common to all channels and one channel specific), simultaneously performing a 6.25ps and a 50ps measurements of the two time-intervals, for example a time-of-arrival (TOA) and a time-over-threshold (TOT) measurement. The 1.6ns measurement range of the prototype can easily be extended to match experiment requirements in future iterations by simple addition of a flip-flop to the counter. The TDC core area is 45µm x 20µm, conversion time after receiving the time-interval is less than 2ns, and average power consumption is 18.4µW for 10% occupancy and 2.9µW for 1% occupancy.
The ASIC design, test setup development and performance, and ASIC characterization challenges will be presented at the workshop.

Early Career

No

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