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Design and characterization of sub-10ps TDC ASIC in 28nm CMOS technology for future 4D trackers

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Stanford University | U.S. DEPARTMENT OF ENERGY

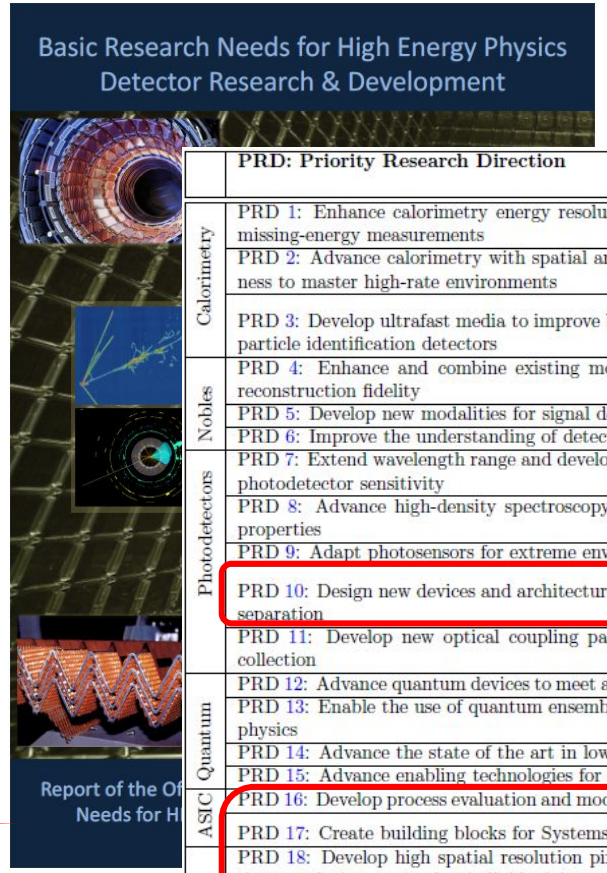
Motivation

2019 DOE Basic Research Needs Study on High Energy Physics Detector Research and Development

- Future high energy, high luminosity hadron colliders will present much higher levels of pileup and extreme radiation environments
- Future detectors will require higher segmentation (3D position resolution) and additional time resolving capabilities while sustaining higher radiation doses (Instrumentation BRN – Science Driver: Higgs and the energy frontier - PRD10, PRD16, PRD17, PRD18, PRD19, PRD20)*
- To satisfy requirements front-end sensors and readout ASICs will need to be compatible with:
  - Larger channel density – Low power, Smaller feature size (Deep sub-micron technologies)
  - Unprecedented radiation levels (dose of up to 30 GRad and 10^{18} neutrons/cm^2)
  - Precision timing resolution – fast sensors, in pixel high precision timing circuits

28nm CMOS

~~TDC design~~

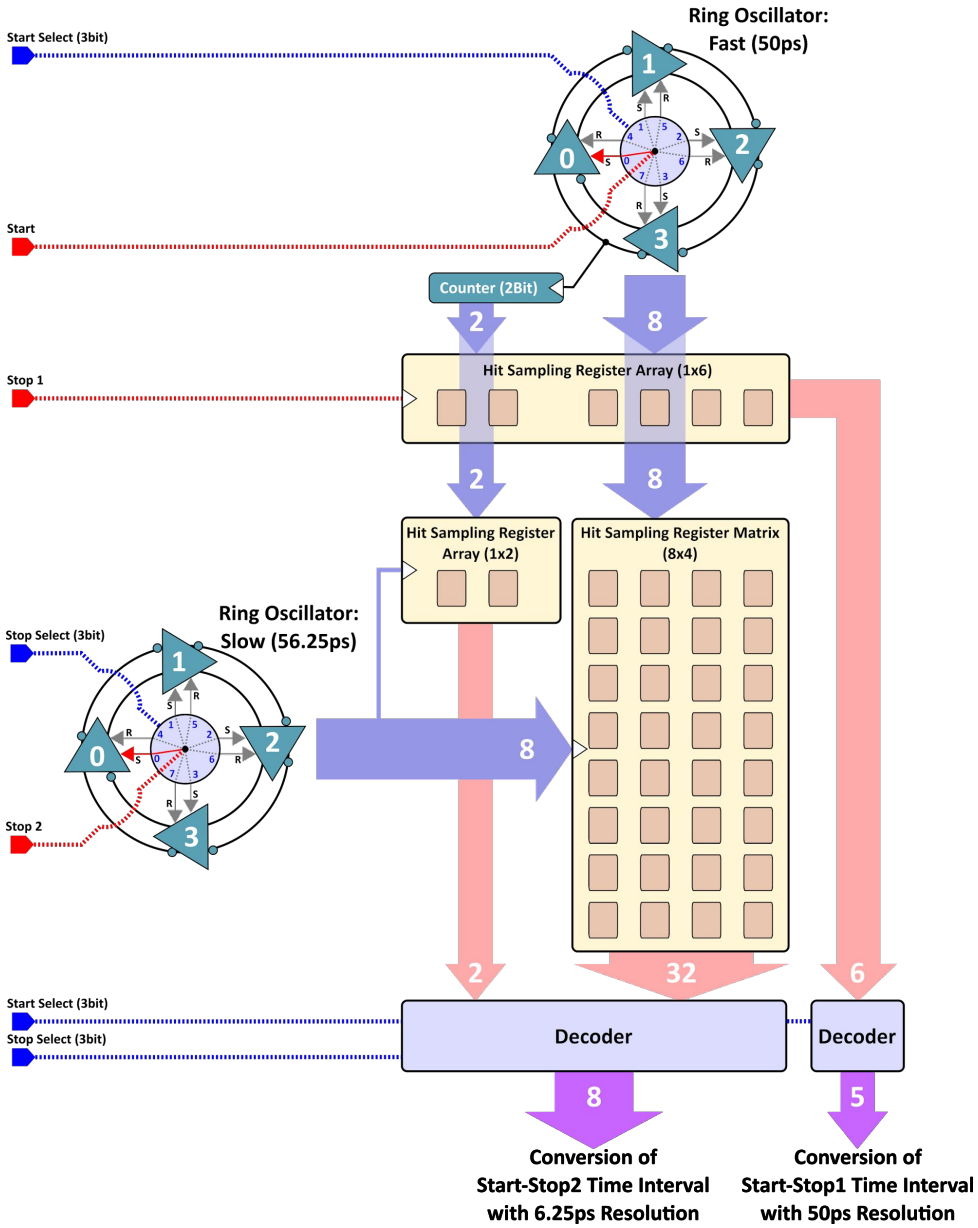


	PRD: Priority Research Direction	Grand Challenge
Calorimetry	PRD 1: Enhance calorimetry energy resolution for precision electroweak mass and missing-energy measurements	1
	PRD 2: Advance calorimetry with spatial and timing resolution and radiation hardness to master high-rate environments	1,4
	PRD 3: Develop ultrafast media to improve background rejection in calorimeters and particle identification detectors	1,3,4
Noble	PRD 4: Enhance and combine existing modalities to increase signal-to-noise and reconstruction fidelity	1,2
	PRD 5: Develop new modalities for signal detection	1
	PRD 6: Improve the understanding of detector microphysics and characterization	1
Photodetectors	PRD 7: Extend wavelength range and develop new single-photon counters to enhance photodetector sensitivity	1,3
	PRD 8: Advance high-density spectroscopy and polarimetry to extract all photon properties	2,3
	PRD 9: Adapt photosensors for extreme environments	2,4
	PRD 10: Design new devices and architectures to enable picosecond timing and event separation	1,2,4
	PRD 11: Develop new optical coupling paradigms for enhanced or dynamic light collection	1,2,3
Quantum	PRD 12: Advance quantum devices to meet and surpass the Standard Quantum Limit	1,3
	PRD 13: Enable the use of quantum ensembles and sensor networks for fundamental physics	1,2
	PRD 14: Advance the state of the art in low-threshhold quantum calorimeters	1,3
	PRD 15: Advance enabling technologies for quantum sensing	1,2,3
ASIC	PRD 16: Develop process evaluation and modeling for ASICs in extreme environments	3,4
	PRD 17: Create building blocks for Systems-on-Chip for extreme environments	1,4
SolidState	PRD 18: Develop high spatial resolution pixel detectors with precise high per-pixel time resolution to resolve individual interactions in high-collision-density environments	1,4
	PRD 19: Adapt new materials and fabrication/integration techniques for particle tracking	2,3
	PRD 20: Realize scalable, irreducible-mass trackers	2,3
TDAQ	PRD 21: Achieve on-detector, real-time, continuous data processing and transmission to reach the exascale	2,4
	PRD 22: Develop technologies for autonomous detector systems	2
	PRD 23: Develop timing distribution with picosecond synchronization	1
Xcut	PRD 24: Manipulate detector media to enhance physics reach	1,3
	PRD 25: Advance material purification and assay methods to increase sensitivity	1,2,3,4
	PRD 26: Addressing challenges in scaling technologies	2,3

*Similar Detector Research and Development Themes (DRDTs) are identified in the 2021 European Committee for Future Accelerators (ECFA) Detector R&D (DRD) Roadmap

28nm TDC Architecture

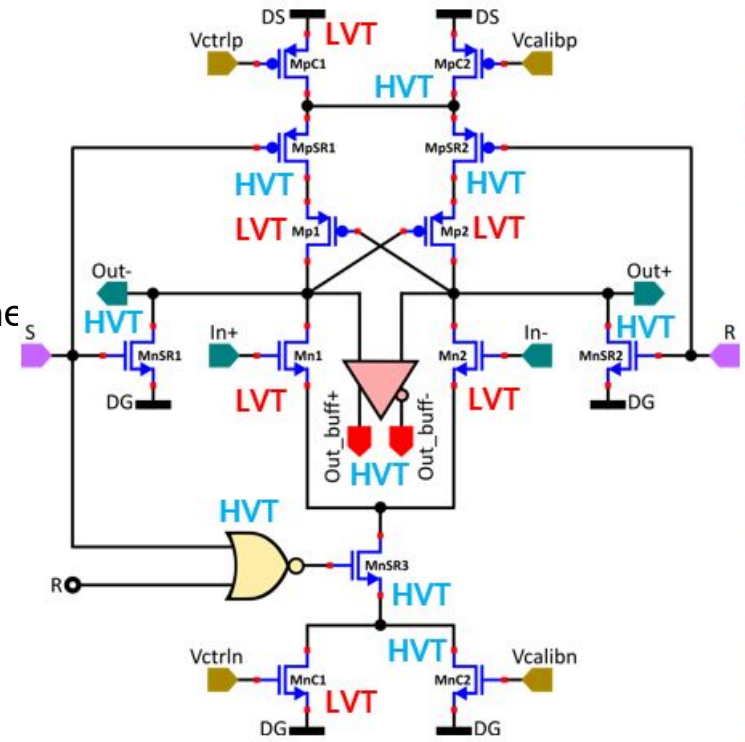
- **2D Vernier Architecture:**
  - Fast Ring Oscillator with 50ps propagation delay cells;
  - Slow Ring Oscillator with 56.25ps propagation delay cells;
- START + two STOP signal for simultaneous Time-Of-Arrival (TOA) and Time-Over-Threshold (TOT) measurements;
- Start-Stop1 - Coarse time resolution (TOT): 50ps;
- Start-Stop2 - Fine time resolution (TOA): 56.25ps - 50ps = 6.25ps;
- **Sliding scale technique for improvement of conversion linearity:**
  - Both ring oscillators have programable starting conditions via delay cell set/reset function;
  - Starting conditions randomly selected each measurement cycle and corresponding values subtracted from the conversion result;
  - Same time intervals converted with different parts/bins of the TDC conversion characteristics;
  - Sliding scale transforms the non-linearities into stochastic variable thus effectively improving the conversion linearity at the expense of worsening single-shoot precision.



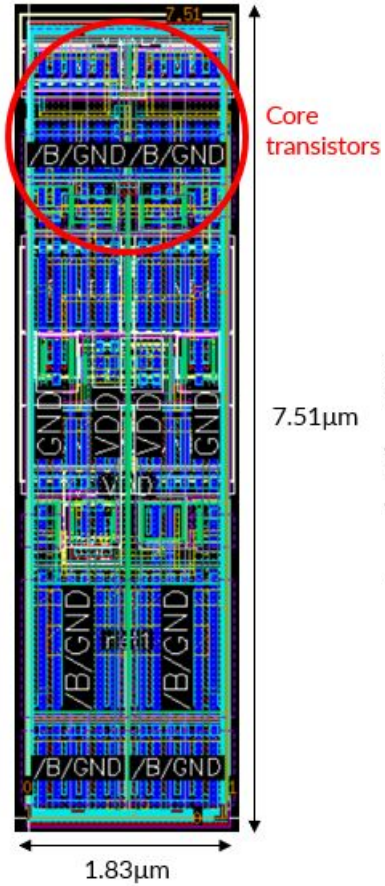
Voltage-Controlled Delay Cell (VCDC)

- Differential Cascode Voltage Switch Logic (DCVSL) implementation
- Current-starved approach for propagation delay control
- Calibration / Trimming
- Output buffer for driving the state-sampling registers
- Set/Reset logic controls
- Leakage reduction*:
  - Non-minimum length (35nm) used for all transistors
  - **Low Voltage Threshold (LVT) used for speed-critical transistors**
  - **High Voltage Threshold (HVT) transistors in series between supply and ground**

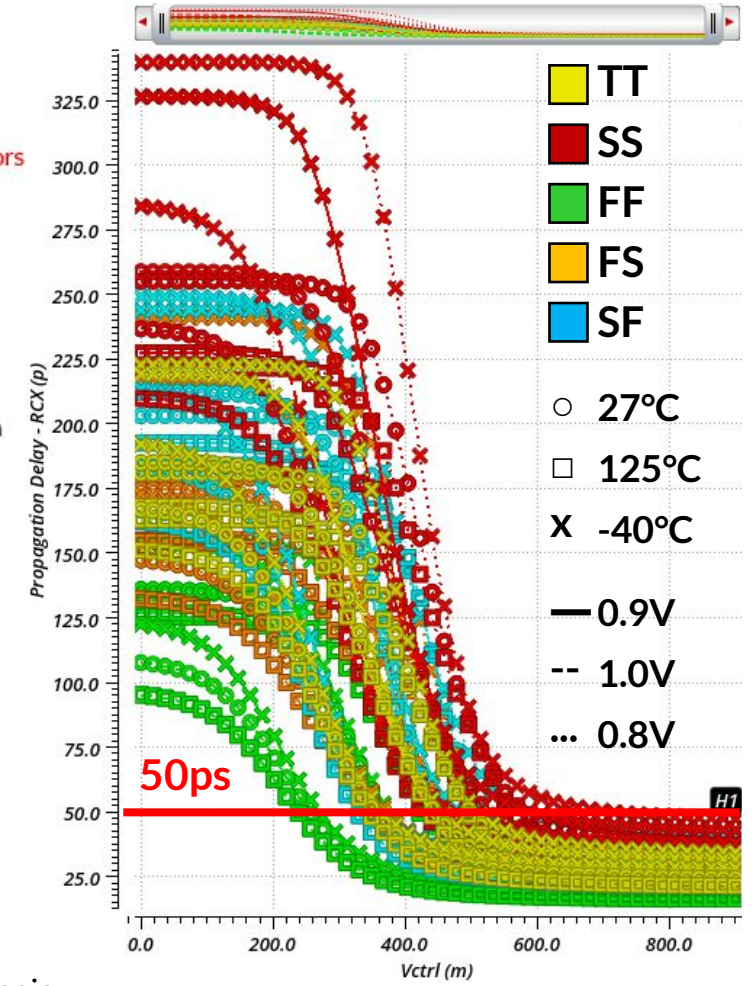
- Schematic:



- Layout:

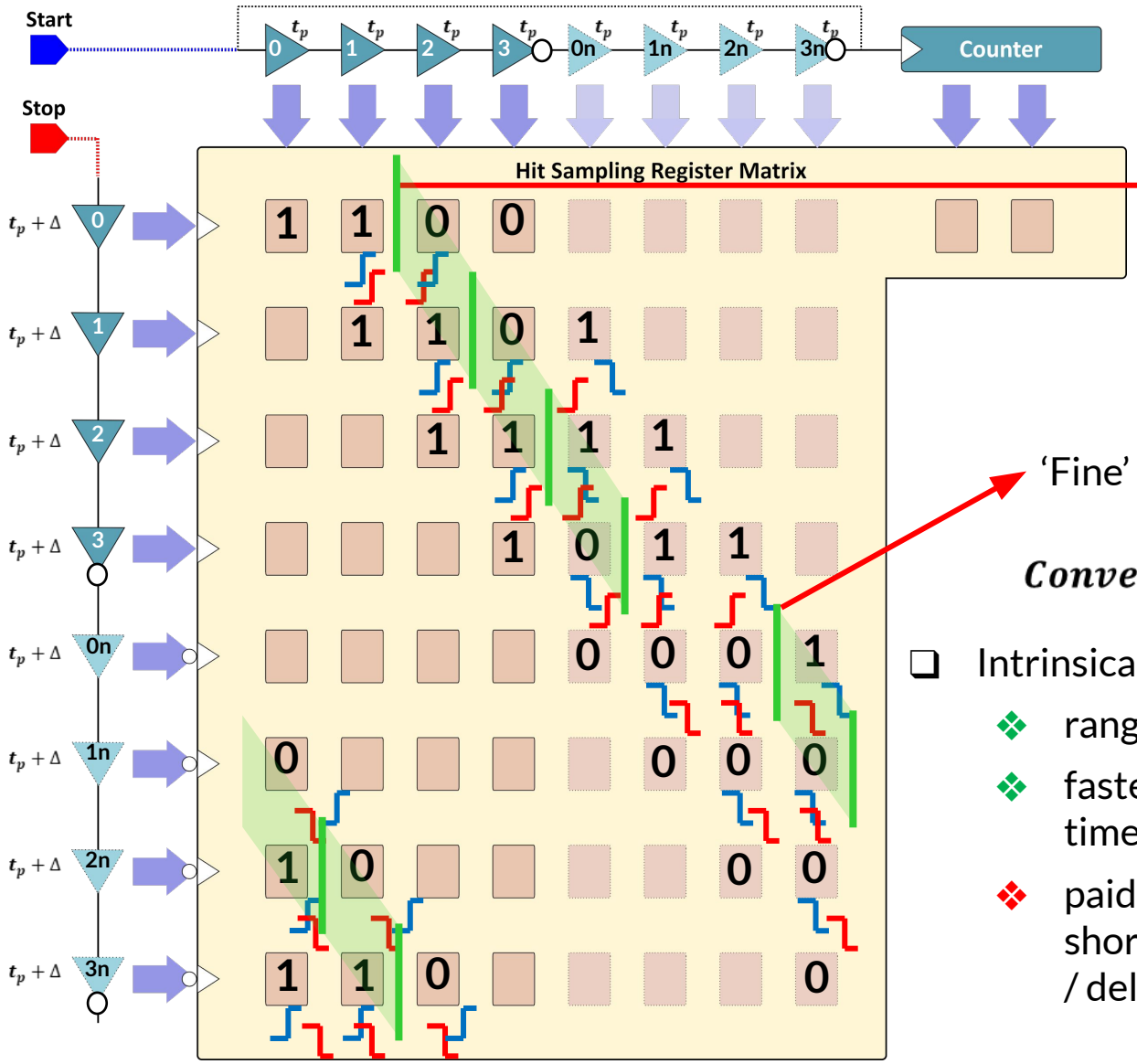


- Delay-Voltage Characteristics (RCX):



*technology simulations show significant leakage currents, making the logic static power consumption not negligible (especially at higher temperatures)

2D Vernier TDC - Operation



'Coarse' (50ps resolution) conversion = 2

$$t_p = 50ps \qquad t_p + \Delta = 56.25ps$$

$$\Delta = 6.25ps$$

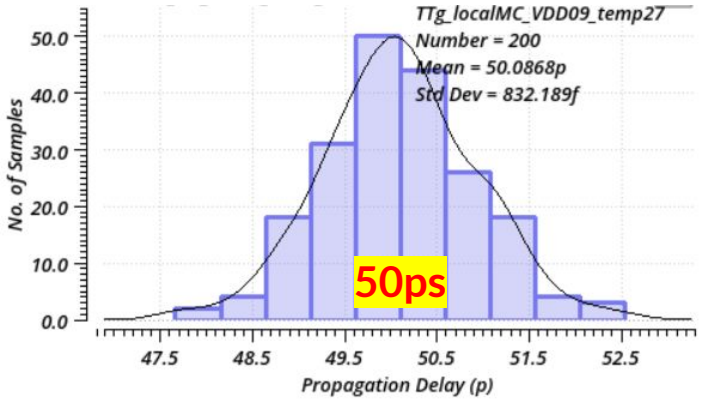
'Fine' (6.25ps resolution) conversion = 3

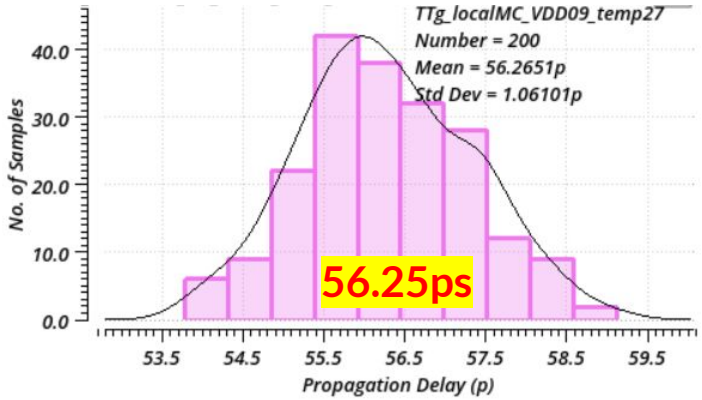
$$\boldsymbol{Conversion\ Result} = (N_{Course} + 1) \cdot 50ps - N_{Fine} \cdot 6.25ps$$

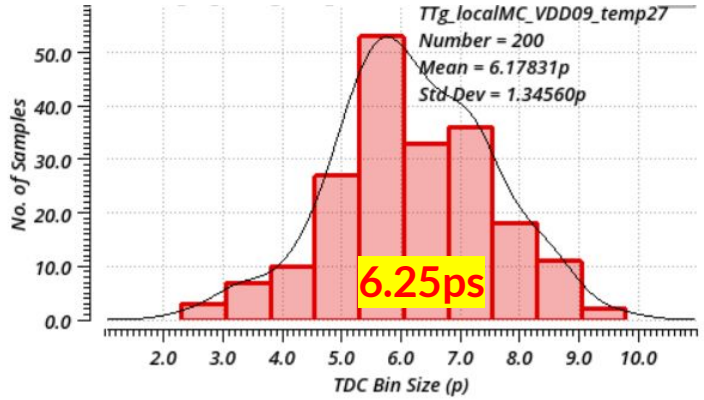
- Intrinsically a coarse-fine conversion. Compared to regular Vernier:
  - range easily extendable by adding bits to the counter
  - faster conversion (lower power consumption for larger time-intervals)
  - paid by larger register area (higher power consumption for shorter time-intervals); less pronounced for shorter oscillators / delay lines

2D Vernier TDC – Mismatch (sliding scale disabled)

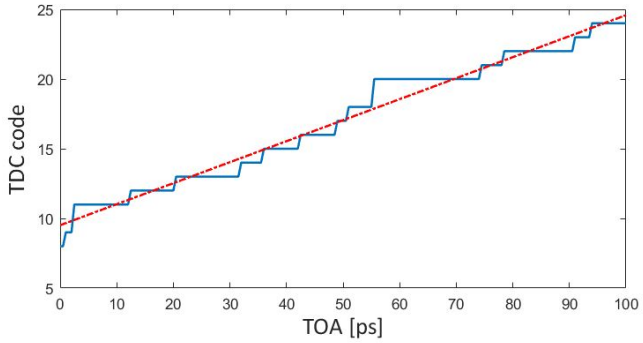
- Delay Cell Mismatch (RCX, Global Corner + Local MC, N° of runs: 200):

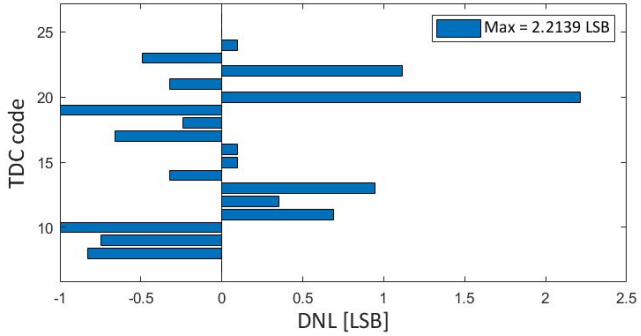


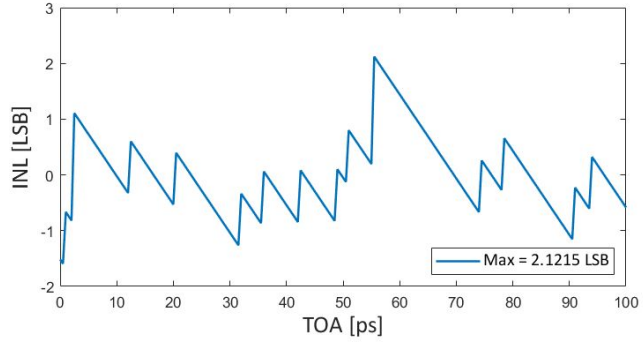




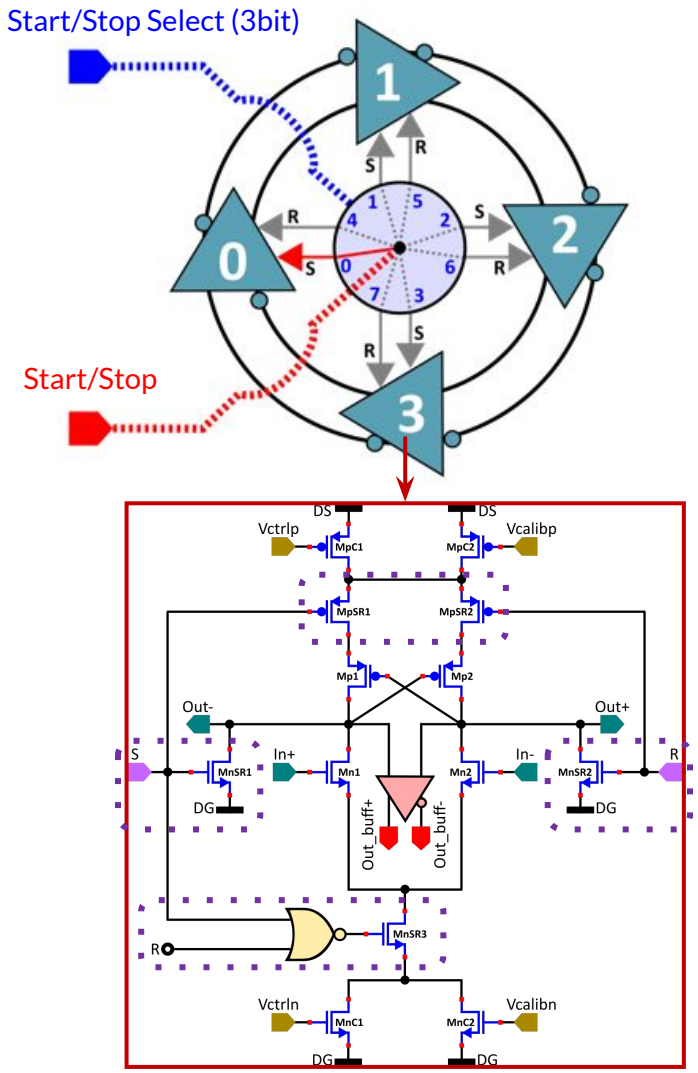
- 2D Vernier TDC characteristics with mismatch (Global Corner + Local MC, one iteration):







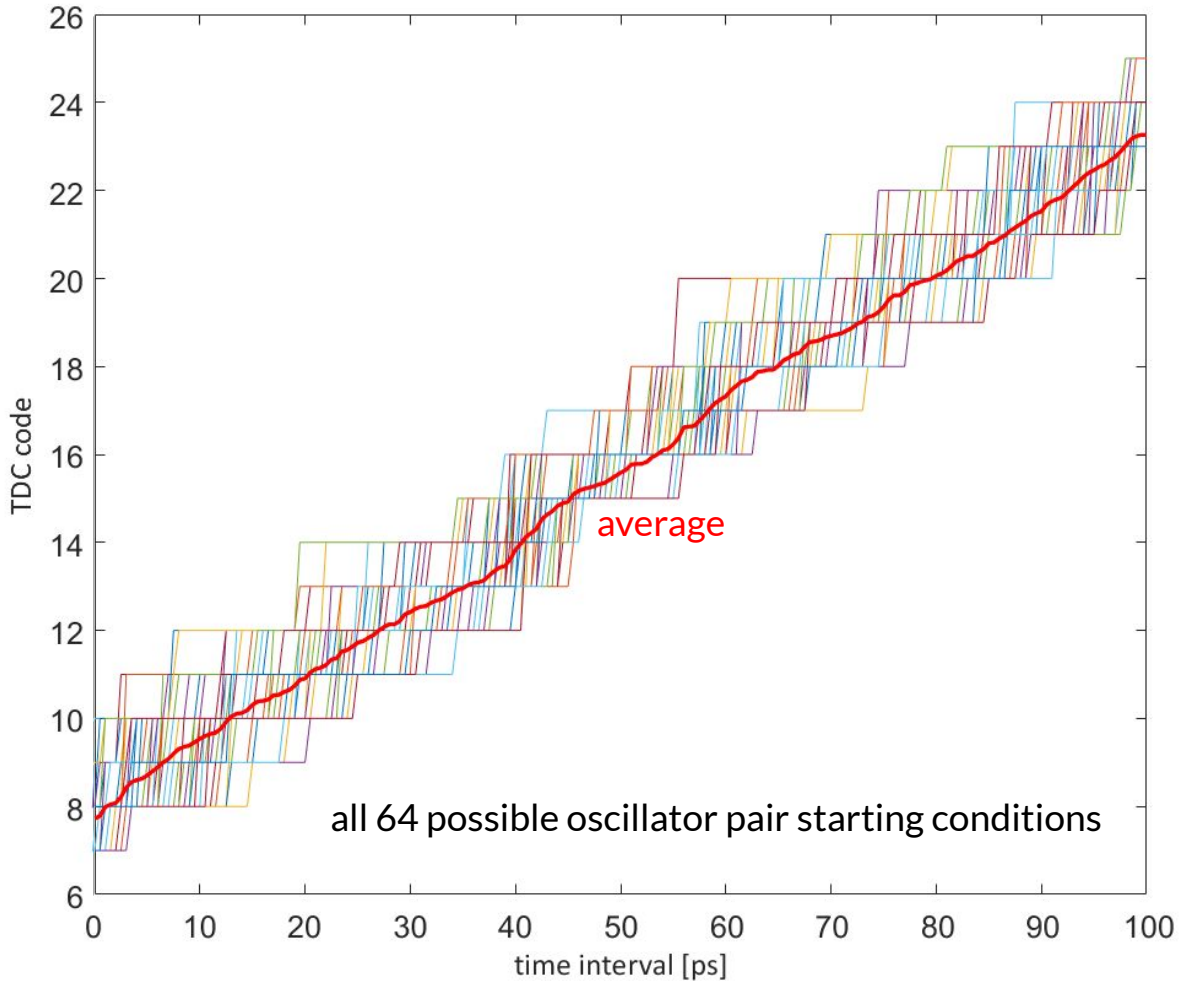
Sliding-Scale Implementation



Sliding-Scale technique [1,2]:

- Both ring oscillators have programable starting conditions via delay cell **set/reset** function;
- Starting conditions randomly selected each measurement cycle and corresponding values subtracted from the conversion result;
- Same time intervals converted with different parts/bins of the TDC conversion characteristics;

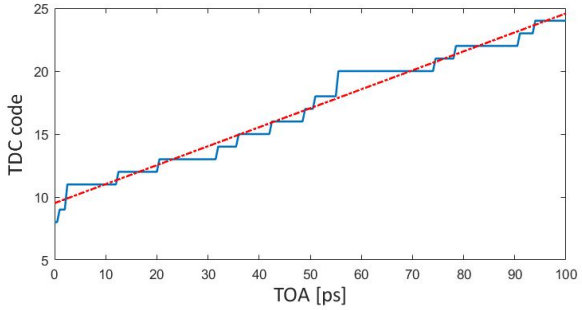
❑ TDC characteristics with mismatch:

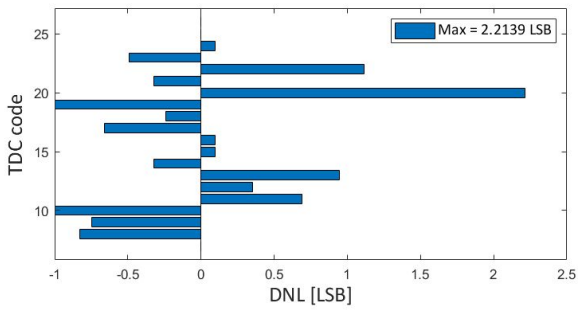


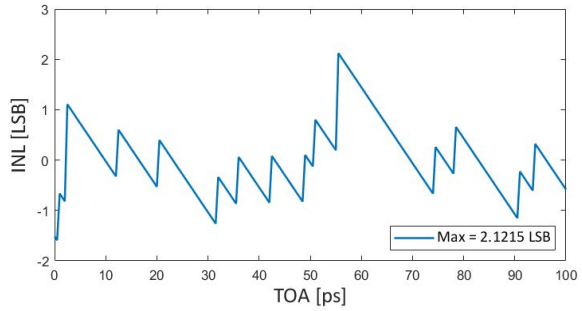
[1] C. Cottini, **E. Gatti**, and V. Svelto, "A new method for analog to digital conversion," Nucl. Instr. Meth., vol. 24, p. 241, Aug. 1963.
[2] **E. Gatti**, P. F. Manfredi, and D. Marino, "Analysis and characterization of cyclic-scale compensated analog-to-digital converters," Nucl. Instrum. Methods, vol. 165, no. 2, pp. 225–230, Oct. 1979.

28nm TDC Architecture – Sliding Scale

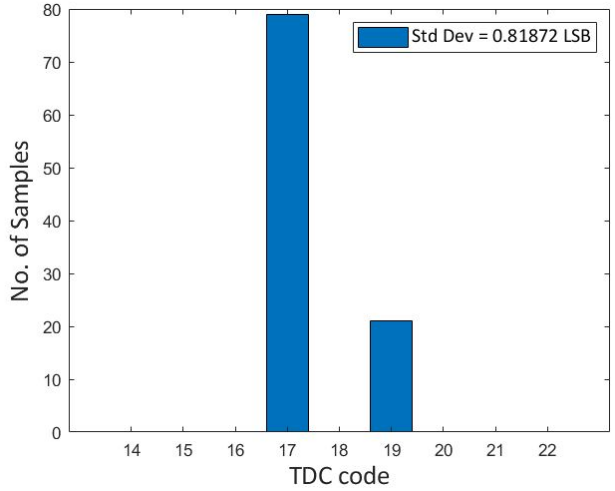
- TDC characteristics with sliding scale disabled



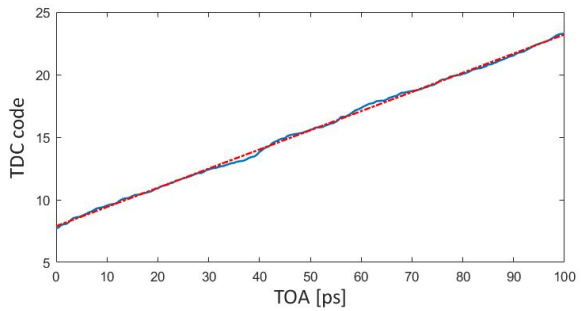


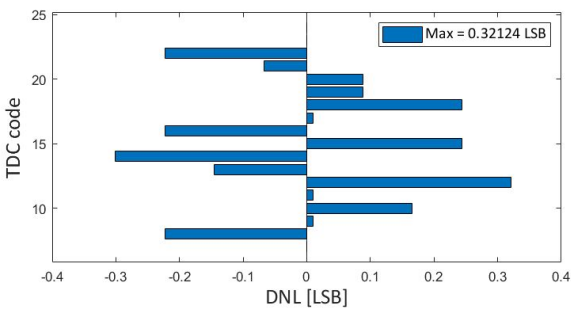


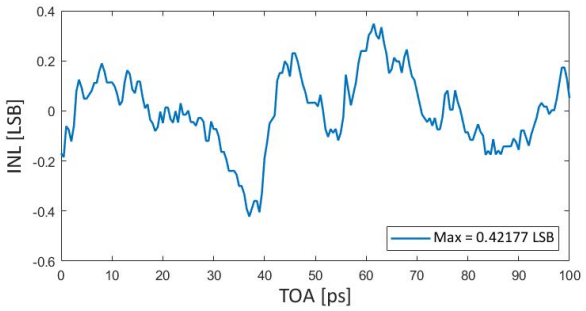
- Transient noise simulation – sliding scale disabled:



- Equivalent TDC characteristics with sliding scale enabled

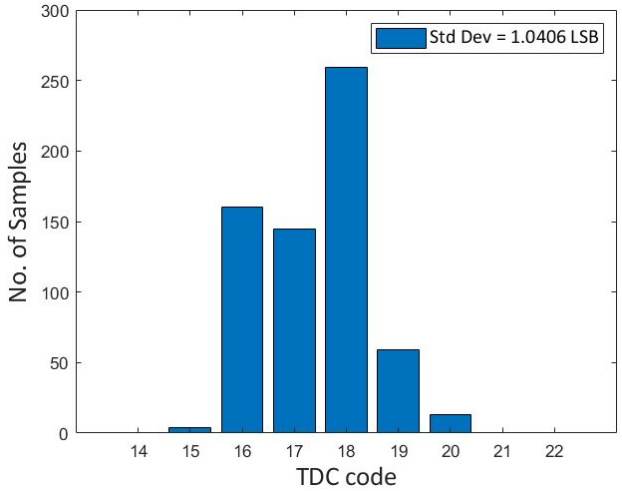






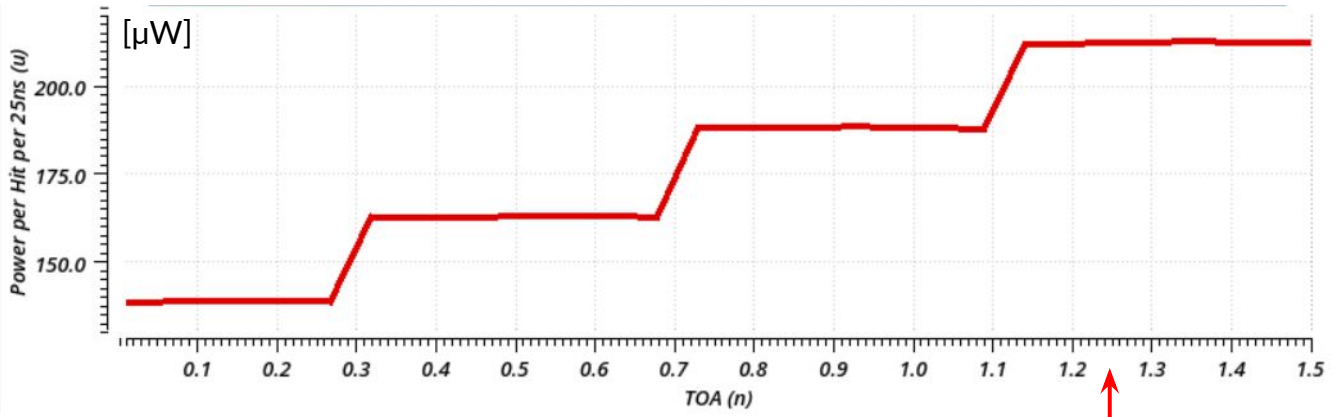
Sliding scale transforms the non-linearities into stochastic variable **thus effectively improving the conversion linearity at the expense of worsening single-shoot precision:**

- Transient noise simulation – sliding scale enabled:

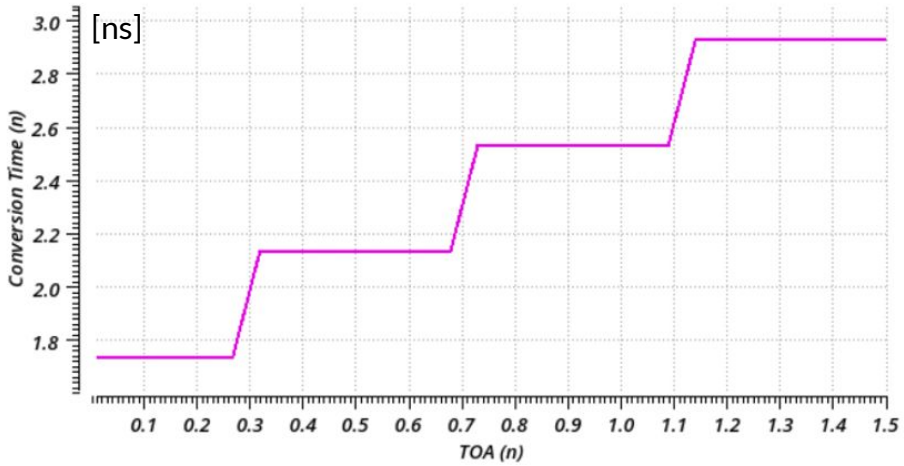


28nm TDC – Power, Conversion Time, Area

- Average power within 25ns window VS TOA (RCX):



- Time between Start signal and the end of conversion VS TOA (RCX):



- TDC/channel idle consumption (due to leakage): ~1.2µW
- TDC/channel power consumption depends on time-interval being measured
  - For uniformly distributed time-intervals Ti the average power consumption per Hit in a 25ns measurement window is:

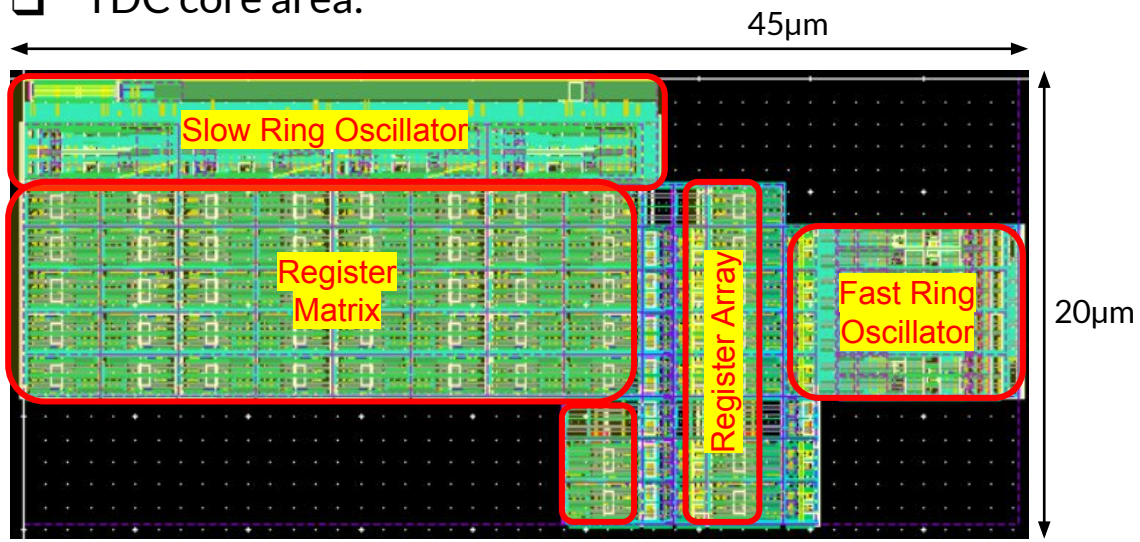
$$P_{\frac{av}{hit}/T_{CK}} = 173\mu W$$

- **<u>Average</u> power consumption:**

$$P_{av} = 1.2\mu W \cdot (1 - Occupancy) + P_{\frac{av}{hit}/T_{CK}} \cdot Occupancy$$

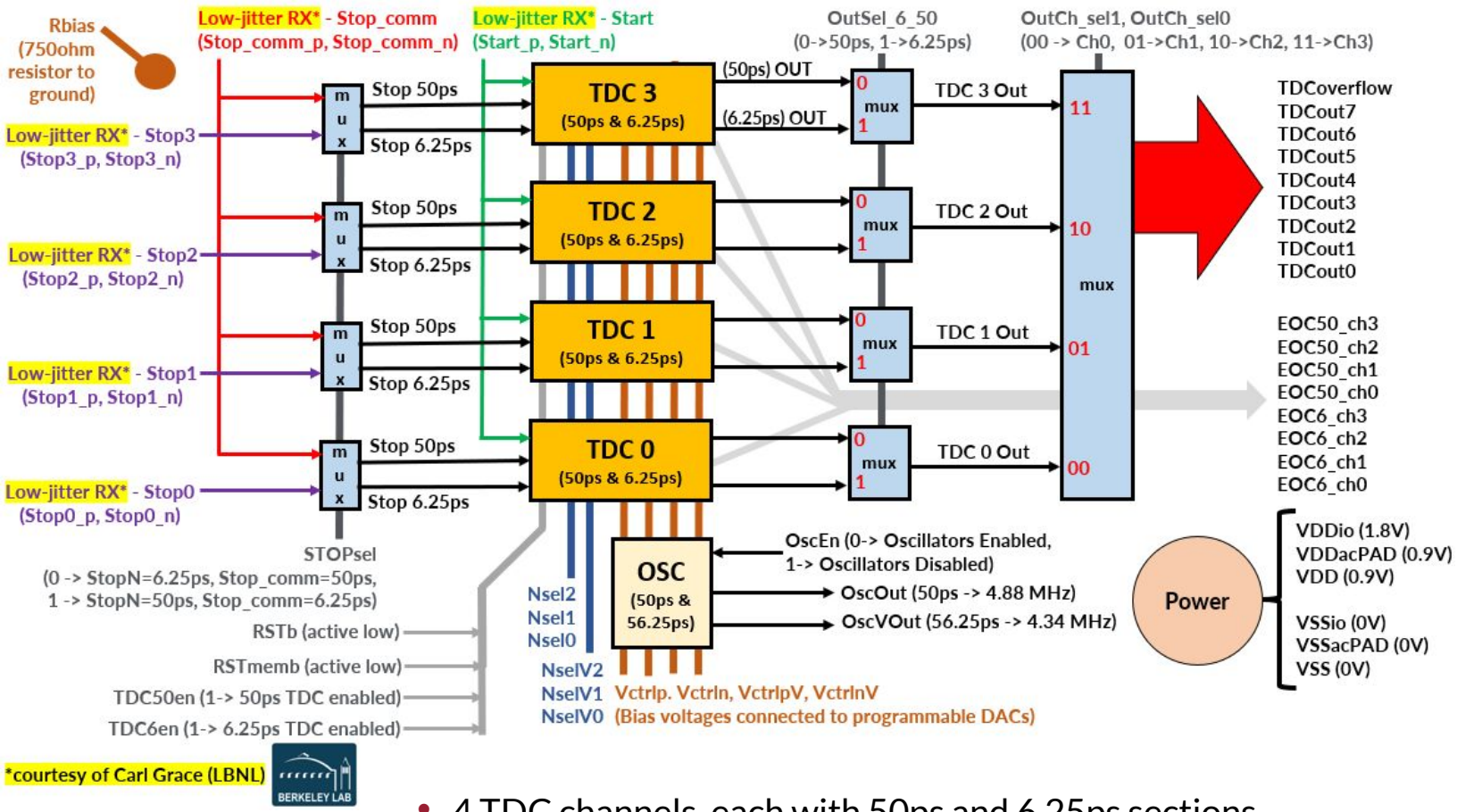
  - **For 10% occupancy: ~ 18.4µW**
  - **For 1% occupancy: ~2.9µW**

- TDC core area:

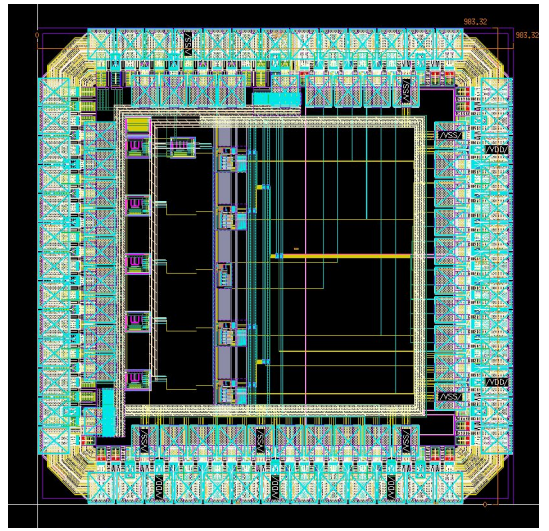


28nm TDC ASIC prototype

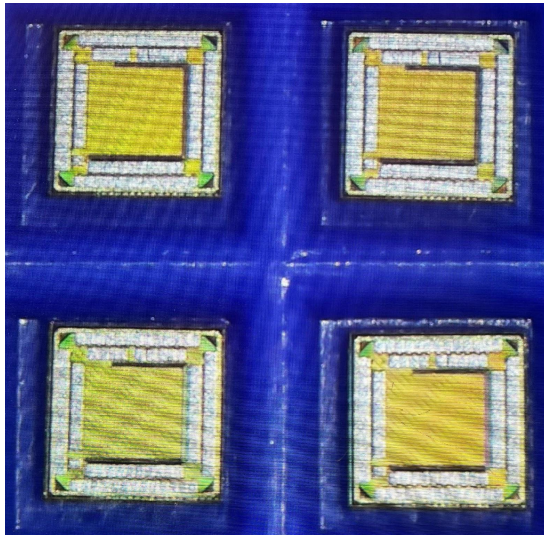
❑ ASIC block schematic:



❑ ASIC layout:



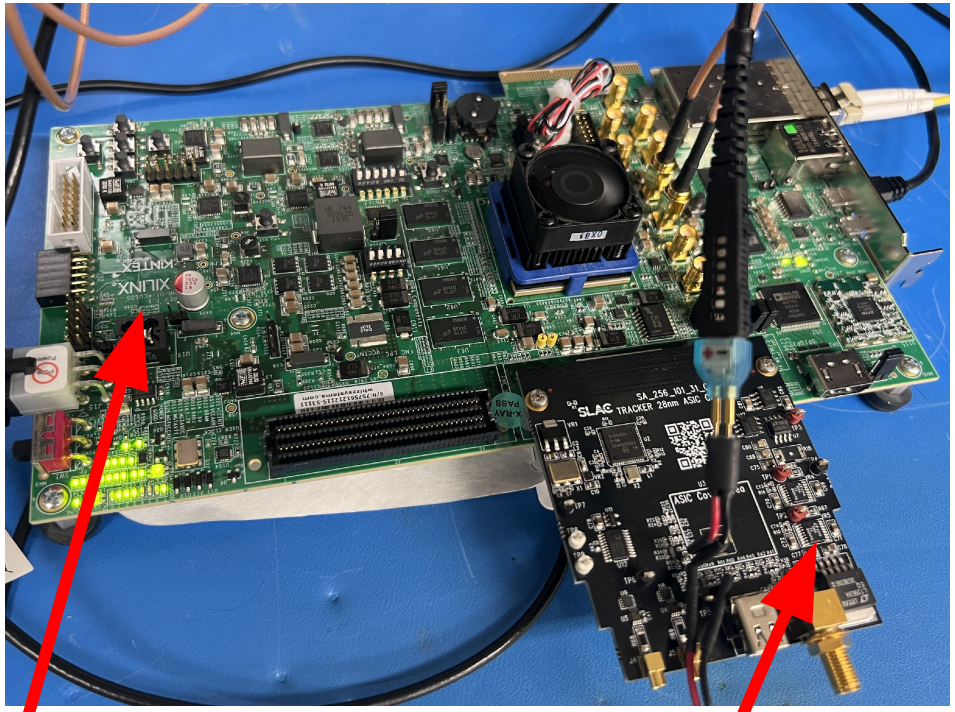
❑ ASICs photo:

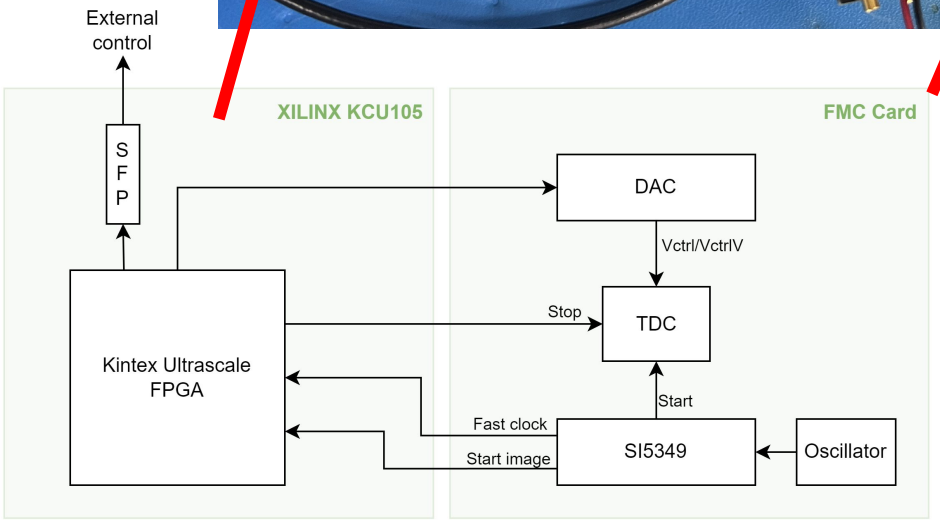


- 4 TDC channels, each with 50ps and 6.25ps sections
- Common Start, a common Stop1 and 4 separated Stop2 inputs
- Low-jitter receivers provided by LBNL
- Fast and Slow Oscillators for propagation delay control

Development Board and custom ASIC Carrier

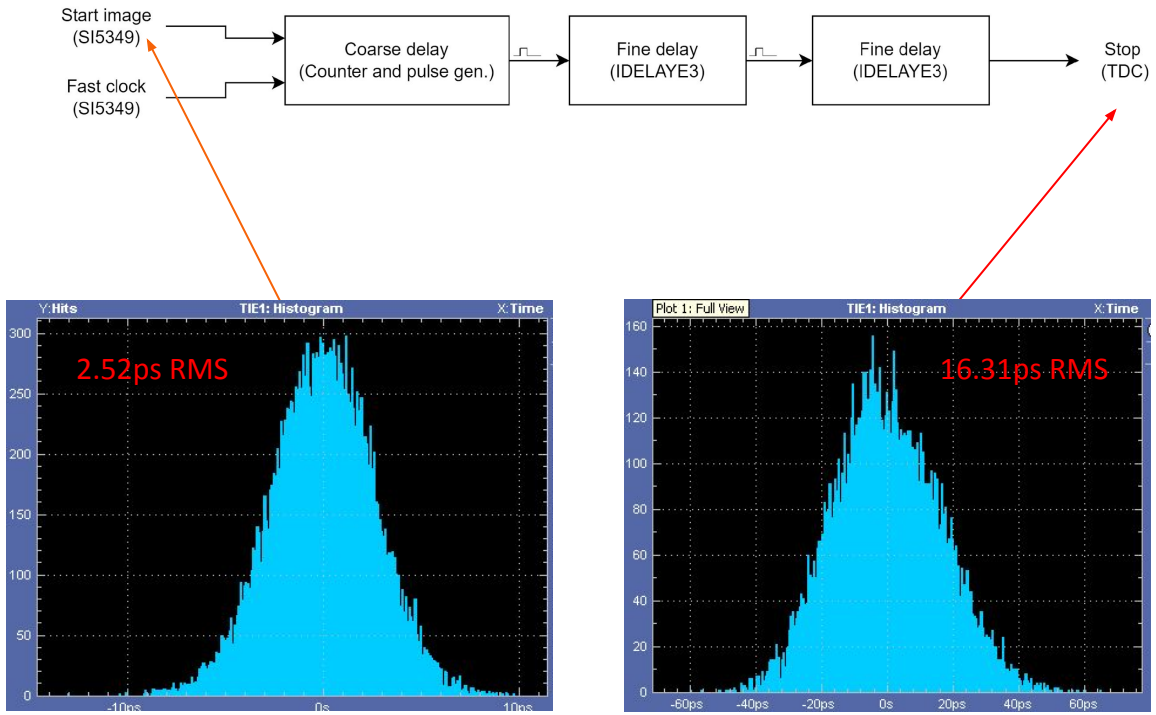
- AMD/Xilinx KCU105 development board for FPGA (KU040)
- FMC card for the ASIC carrier
  - Power regulation
  - Level translation
  - Low jitter PLL reference
  - Connectors for external reference and inputs option
- PLL (SI5349) provides start and stop signal sources:
  - Start signals directly comes from a PLL output
  - Jitter measurement: 2.6 ps-RMS
  - Output start images to the FPGA – constant phase
  - Provide fast clock signal that is used to shift the start signal
- DAC allows testing the ring oscillator reply in frequency
- External control through 10 Gbps serial link

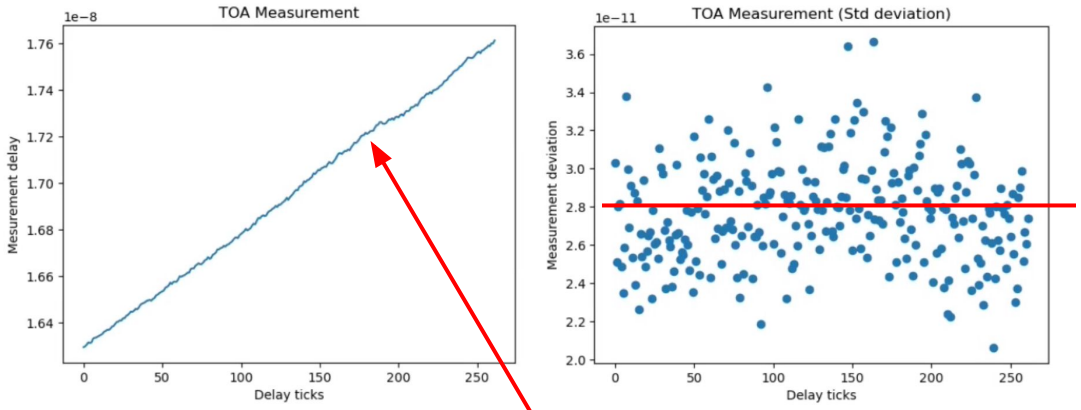




FPGA Calibration pulse results and path forward

- **TOA measurements (calibration):**
  - Measured using high speed scope (Tektronix DPO7254)
  - Averaged over 1000 samples
  - Max. Std deviation of 35ps

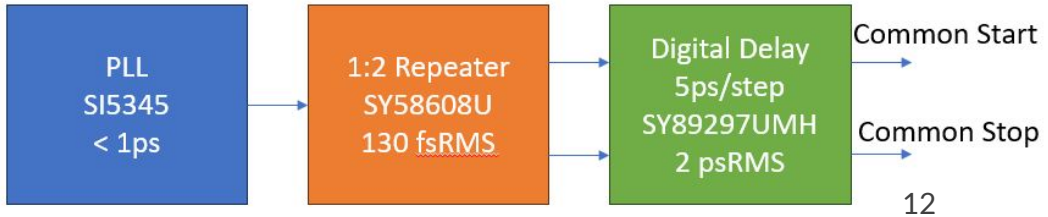




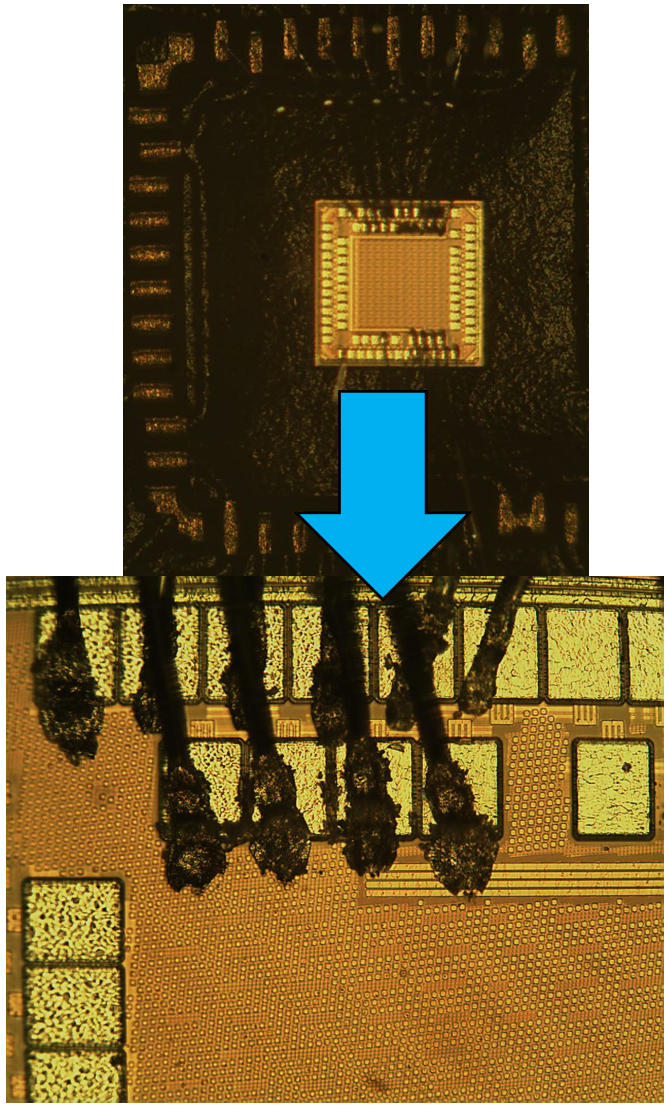
~28ps STD

IDELAY3's non-linearity components

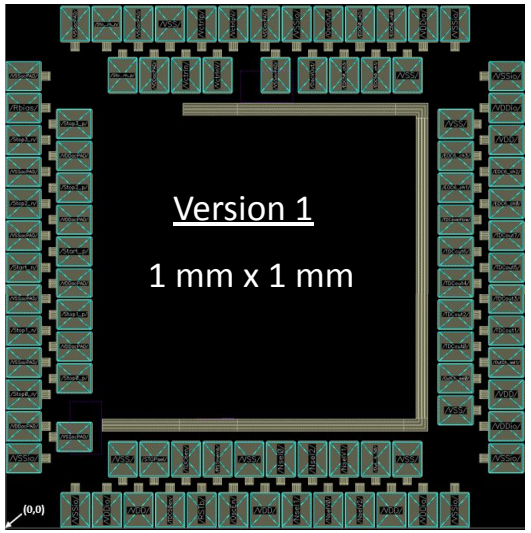
- **Status:**
  - Good enough for the 50ps/step linear sweeping
  - But **not** good enough for 6.5ps/step
  - Can be used to qualify the 50ps configuration
- **Path forward:**
  - Use of external delay line (SY89297UMH)



ASIC + PCB Wire bonding Issues



54 µm pitch (4 gap) and double row was too aggressive for the wire bonding pads



Retape out ASIC with less I/O pads, single row, and wider pitch

Summary and Future Plans

- **First tape out of 28nm at SLAC:**
  - As with any new technology node, there are large learning curves to overcome

- **Custom ASIC PCB carrier and FPGA firmware/software has been developed**
  - Calibration sweep circuit meets the 50ps/step requirement
  - Expecting much lower jitter in the common stop (< 3p-RSM) in the next ASIC carrier revision with new delay IC circuit

- **ASIC bonding pad placement was too aggressive in Version 1:**
  - Lesson learned: Getting feedback from wire bonding vendor and their recommendation prior to tape out
  - Version 2 will use a less aggressive pad pitch (Early 2024 tape out)

Backup

Linearity Improvement: Sliding-Scale

Ideal Converter:

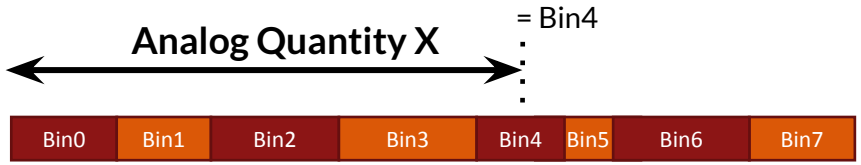
Real Converter:

[1] C. Cottini, **E. Gatti**, and V. Svelto, "A new method for analog to digital conversion," Nucl. Instr. Meth., vol. 24, p. 241, Aug. 1963.

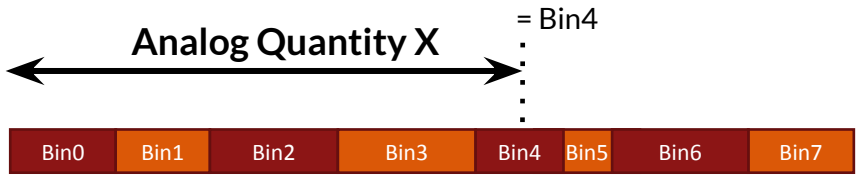
[2] **E. Gatti**, P. F. Manfredi, and D. Marino, "Analysis and characterization of cyclic-scale compensated analog-to-digital converters," Nucl. Instrum. Methods, vol. 165, no. 2, pp. 225–230, Oct. 1979.

- Regular Converter:

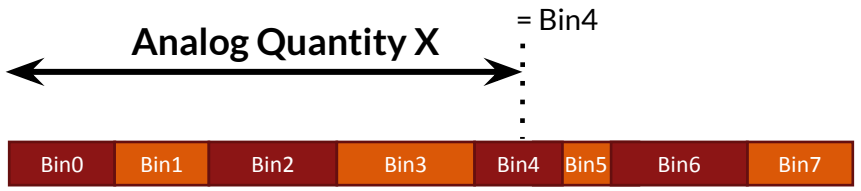
Measurment1:



Measurment2:

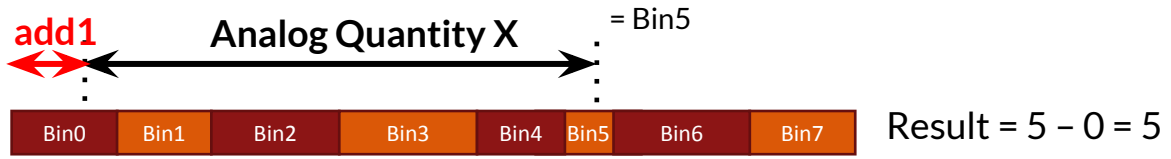


Measurment3:

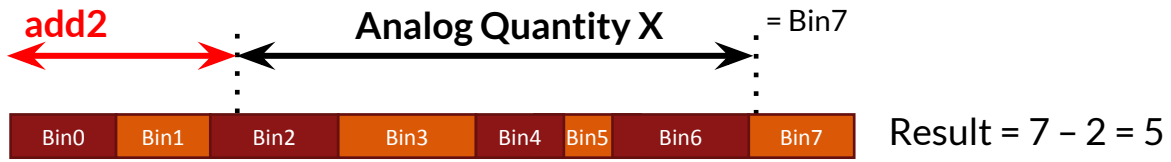


- Sliding Scale [1][2]

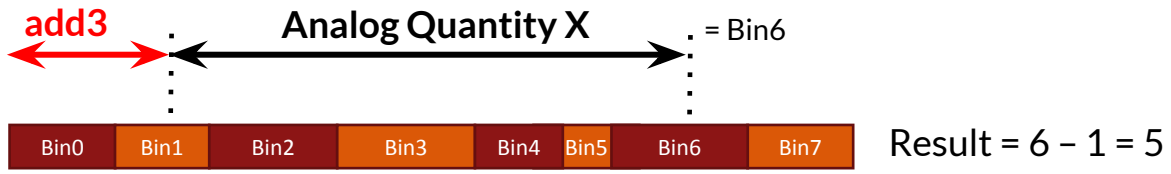
Result = Conversion - add



Result = 5 – 0 = 5



Result = 7 – 2 = 5



Result = 6 – 1 = 5

Readout Block Diagram

- **Controlled via an AXI-Lite bus:**
  - Configure TDC via memory mapped registers
  - Set DAC to configure the TDC's oscillators
  - Read TDC's oscillator frequency
  - Start and get status of custom FSMs
- **Start position finder:**
  - Search for the first non-overflow value
  - Generate stop pulse sync with start
  - Shift stop pulse by fast clock period steps
  - Set the 0 position with 5ps accuracy (IDEALYE3)
- **Scan and readout:**
  - Set fine delay position (increment of 5ps)
  - Generate AXI stream frame with position and TDCOut