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Q-Pix: ASIC Development and First Prototypes for Pixelated Charge Readout

Friday, 10 November 2023 09:30 (15 minutes)

The Q-Pix concept (arXiv: 1809.10213) is a continuously integrating low-power charge-sensitive amplifier (CSA) viewed by a Schmitt trigger. When the trigger threshold is met, the comparator initiates a 'reset' transition and returns the CSA circuitry to a stable baseline. This is the elementary Charge-Integrate / Reset (CIR) circuit. The instance of reset time is captured in a 32-bit clock value register, buffers the cycle and then begins again. What is exploited in this new architecture is the time difference between one clock capture and the next sequential capture, called the Reset Time Difference (RTD). The RTD measures the time to integrate a predefined integrated quantum of charge (Q). Waveforms are reconstructed without differentiation and an event is characterized by the sequence of RTDs. This technique easily distinguishes the background RTDs due to 39Ar decays (which also provide an automatic absolute charge calibration) and signal RTD sequences due to ionizing tracks. Q-Pix offers the ability to extract all track information providing very detailed track profiles and also utilizes a dynamically established network for DAQ for exceptional resilience against single point failures. This talk will present the status of the Q-Pix analog and digital ASICs, introduce results from first prototypes, and discuss future planned tests.

Early Career

Yes

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