The LArPix Pixelated Charge Readout System for Liquid Argon TPCs

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See also: Dan Dwyer, “LArPix and LightPix: Scalable Readout for Large Cryogenic Detectors” - Wednesday Plenary
Carl Grace, “Cold Electronics: Progress and Potential” - Wednesday RDC4
Stephen Greenberg, “LightPix: Scalable digital readout for cryogenic SiPM applications” Friday RDC1+RDC4
LArTPC Pixel Readout Motivation

- Conventional LArTPC readout is wire-based, ~4mm wire pitch
  - Multiple 2D readout planes
- 2D readout includes ambiguities and anisotropic responses
- Becomes more problematic in higher rate environments
- 3D pixelated readout overcomes most of these
LArTPC Pixel Readout Challenges

• **Note:** *not all unique to pixel readout*

• High **channel count**… ~4mm pixel pitch
  – with manageable data rate
  – with minimal # cables interfacing with cryostat

• **Low noise**
  – < 1ke− for MIP detection

• **Cryogenic compatibility**
  – Stringent heat dissipation limits, ~100 μW/pixel

• **Scalability**
  – Instrument large areas, $O(10^2$-$10^3)$ m$^2$, affordably and practically

• **Reliability**
  – Applications demand ~100% uptime and long operational periods, $O$(decades)
The LArPix-v2 Channel

- 64 channels / ASIC
- Simple front end (no signal shaping)
- Self-triggering discriminator
- Configurable thresholds and integration times
- On-chip digital control

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LArPix-v2 System Components

- Pixel tile PCB containing 1000’s of pixels/ft$^2$ and minimal active components
- LArPix ASIC loaded onto backside of pixel tiles
- Single 34-pin ribbon cable per tile
- PACMAN controller
  - Delivers clean power to 100’s of ASICs
  - Establishes I/O with ASICs
  - Handles DAQ and configuration for up to 8 tiles
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All components produced by commercially available vendors

Approaching ~$0.10/channel, ~$10K/m²
Hydra I/O Networking

- 2022 R&D 100 Award
- PISO/POSI pair on every edge for chip-to-chip UART data transmission
  - Digital multiplexing $O(10^3)$ channels per I/O channel
- Enables configurable network paths to send data in/out
  - Avoid single point failures
- Multiple (4) external links per tile PCB (not pictured)
LArPix System Applications

- **DUNE LArTPC Near Detector (ND-LAr)**
  - ~14,000,000 pixels across 5x7 array of 3x1x1 m$^3$ modules
  - Central cathode and 2 pixelated anode planes per module
  - Optically isolated TPCs

- Potentially a “phase 2” DUNE FD module
  - Order of magnitude larger than ND
  - 8x8 pixel tile grid compatible with existing protoDUNE-VD infrastructure
2x2 Demonstrator

- Demonstration of ND-LAr design
- 2x2 array of 1.2 x 0.6 x 0.6 m³ modules containing >300K pixel channels
- 4 modules operated individually at Bern
  - O(10⁸) cosmic events
2x2 Demonstrator

- Demonstration of ND-LAr design
- 2x2 array of 1.2 x 0.6 x 0.6 m$^3$ modules containing >300K pixel channels
- 4 modules operated individually at Bern
  - $O(10^8)$ cosmic events
- @ Fermilab underground facility (MINOS hall) between repurposed Minerva planes
- Will image neutrino interactions in the GeV-energy regime from the NuMI beam
Simulation

JINST 18 P04034 (2023)
Closing Remarks

- 2016-2018: LArPix v1 proof of principle ASIC
- 2023-2024: LArPix v2 system deployed in a 2.5 tonne active mass LArTPC neutrino detector including >330,000 channels (2x2 Demonstrator)

- Continuing to develop the system and scale up implementations, stay tuned!

<table>
<thead>
<tr>
<th>Component</th>
<th>LArPix ASIC</th>
<th>Pixel tile</th>
<th>PACMAN controller</th>
</tr>
</thead>
<tbody>
<tr>
<td>R&amp;D focus</td>
<td>- Correlated double sampling → noise - 10-bit ADC → resolution - Robustness</td>
<td>- Increase size 60% - Optimize pixel pad geometry - Shielding layer to reduce inductive</td>
<td>- 10-tile capable - Differential analog monitor with ADC</td>
</tr>
</tbody>
</table>
Backup
The LArPix ASIC will read out the charge signals from DUNE near detector LArTPC component, ND-LAr.

~15 million channels (3.8 x 3.8 mm$^2$ pixel pads) readout by ~0.25 million ASICs.
ArgonCube Design

- Modular approach, O(50 cm) drifts
- Central cathode provides drift field for 2 optically isolated TPCs
- Resistive shell field cage
- Light detection modules installed along the field cage
- Anode planes outfitted with tiles of PCB components containing gold-plated pixel pads on one side and LArPix ASICs on the other
## LArPix Readout System Overview

<table>
<thead>
<tr>
<th>Item</th>
<th>Quantity for 2x2</th>
<th>Quantity for FSD module</th>
<th>Quantity for ND-LAr</th>
</tr>
</thead>
<tbody>
<tr>
<td>LArPix ASIC</td>
<td>6,400 + 3,200</td>
<td>6,400 + 3,200</td>
<td>224,000 + ~100,000 (Actual spare count will be based on ASIC yield of first production wafer run)</td>
</tr>
<tr>
<td>Tile PCB</td>
<td>64 + 16 (100 ASICs/Tile)</td>
<td>40 + 10 (160 ASICs/Tile)</td>
<td>1,400 + 280 (160 ASICs/Tile)</td>
</tr>
<tr>
<td>Pacman</td>
<td>8 + 4</td>
<td>4 + 2 + 4</td>
<td>140 + 20</td>
</tr>
<tr>
<td>Cryogenic cables</td>
<td>64 + 8</td>
<td>40 + 10</td>
<td>1,400 + 280</td>
</tr>
<tr>
<td>Feedthrough assembly</td>
<td>8 + 8</td>
<td>2 + 2</td>
<td>70 + 7</td>
</tr>
</tbody>
</table>
1.2 MW LBNF Spill on ND-LAr

Flash Spectrum

FV interactions in color
- OOFV Neutrinos
- OOFV Other