BERKELEY LAB

The LArPix Pixelated Charge Readout System for Liquid Argon TPCs

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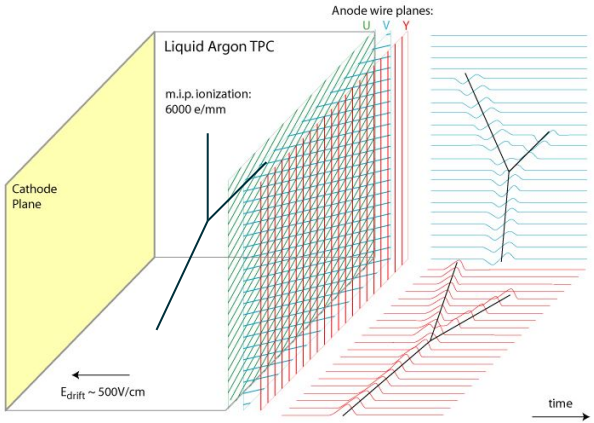
See also: Dan Dwyer, “LArPix and LightPix: Scalable Readout for Large Cryogenic Detectors” - Wednesday Plenary
Carl Grace, “Cold Electronics: Progress and Potential” - Wednesday RDC4
Stephen Greenberg, “LightPix: Scalable digital readout for cryogenic SiPM applications” Friday RDC1+RDC4

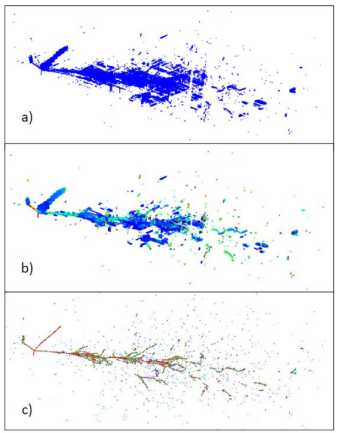
LArTPC Pixel Readout Motivation

- Conventional LArTPC readout is wire-based, ~4mm wire pitch
  - Multiple 2D readout planes
- 2D readout includes ambiguities and anisotropic responses
- Becomes more problematic in higher rate environments
- 3D pixelated readout overcomes most of these

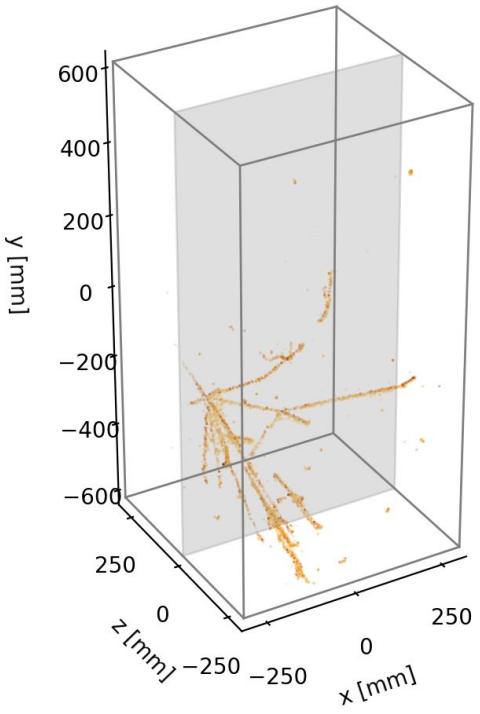
Courtesy of Bo Yu (BNL)



X. Qian *et al* 2018 *JINST* **13** P05032

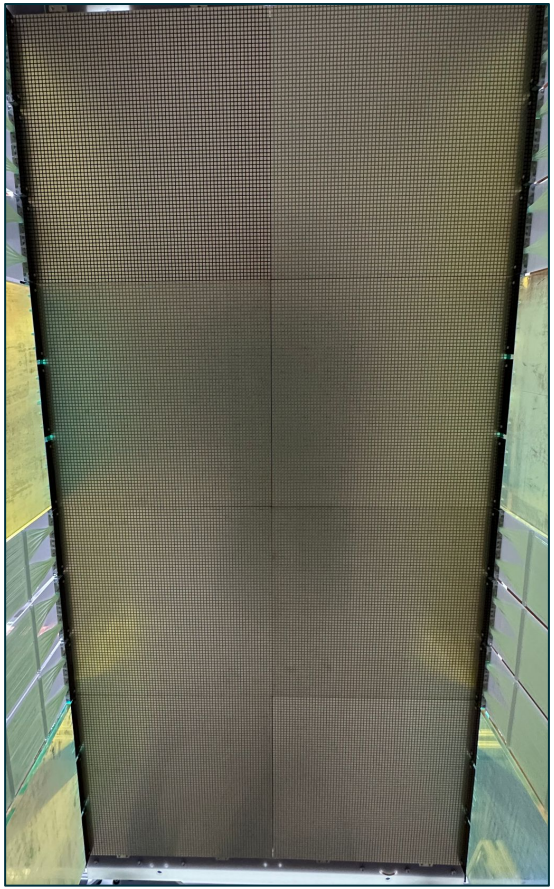


LArPix Raw Data



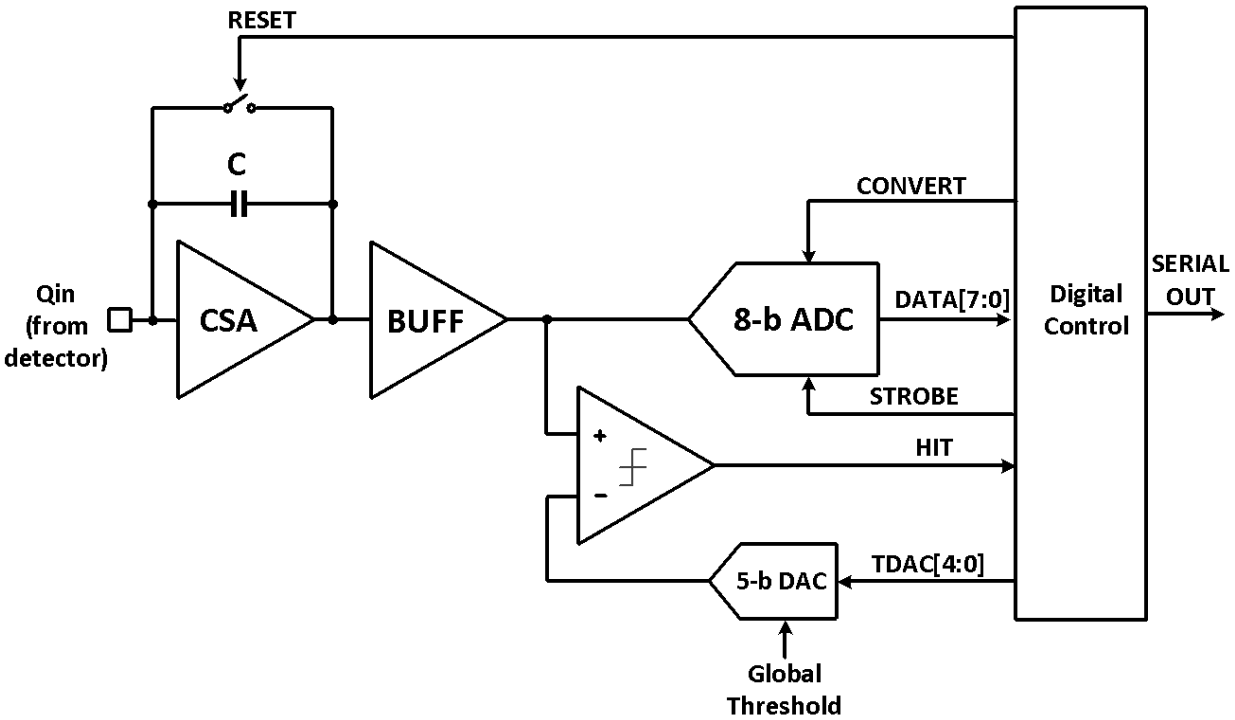
LArTPC Pixel Readout Challenges

- *Note: not all unique to pixel readout*
- High **channel count**… ~4mm pixel pitch
  - with manageable data rate
  - with minimal # cables interfacing with cryostat
- **Low noise**
  - < 1ke$^-$ for MIP detection
- **Cryogenic compatibility**
  - Stringent heat dissipation limits, ~100 μW/pixel
- **Scalability**
  - Instrument large areas, O(10^2-10^3) m^2, affordably and practically
- **Reliability**
  - Applications demand ~100% uptime and long operational periods, O(decades)



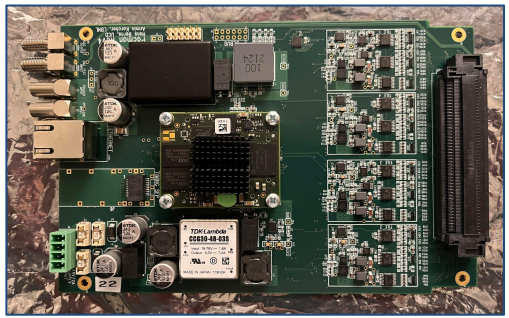
The LArPix-v2 Channel

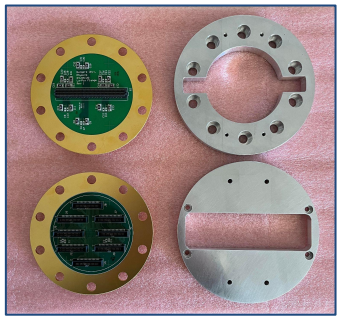
- 64 channels / ASIC
- Simple front end (no signal shaping)
- Self-triggering discriminator
- Configurable thresholds and integration times
- On-chip digital control

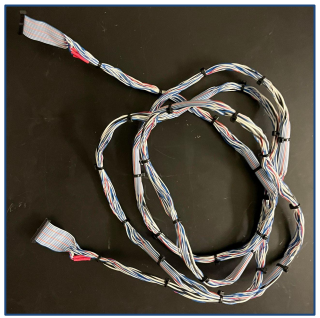


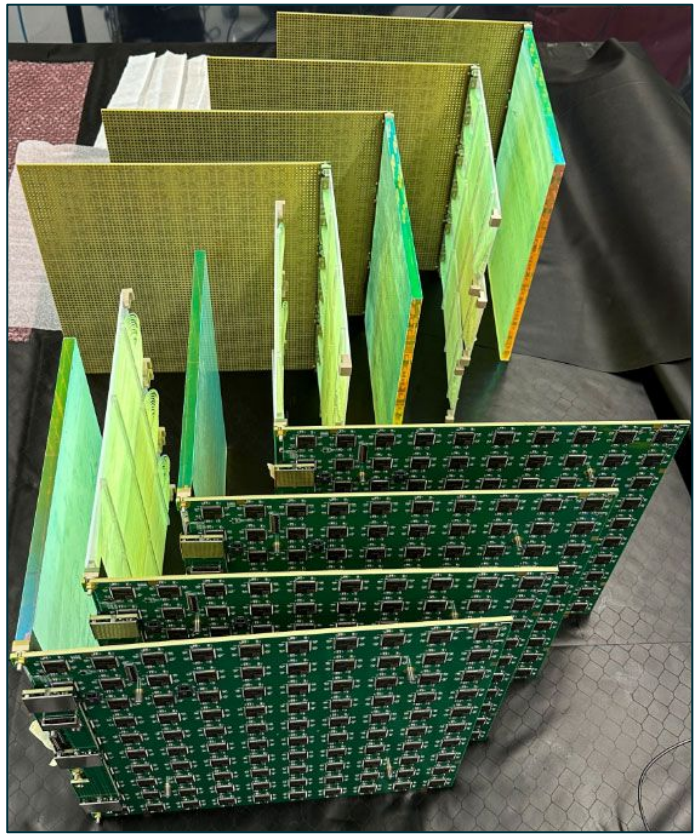
LArPix-v2 System Components

- Pixel tile PCB containing 1000's of pixels/ft^2 and minimal active components
- LArPix ASIC loaded onto backside of pixel tiles
- Single 34-pin ribbon cable per tile
- PACMAN controller
  - Delivers clean power to 100's of ASICs
  - Establishes I/O with ASICs
  - Handles DAQ and configuration for up to 8 tiles









LArPix-v2 System Components

- Pixel tile PCB containing 1000's of pi… d minimal active compone…
- LArPix ASIC lo…
- Sing…

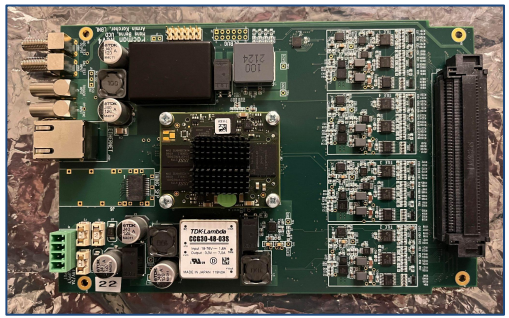
All components produced by commercially available vendors

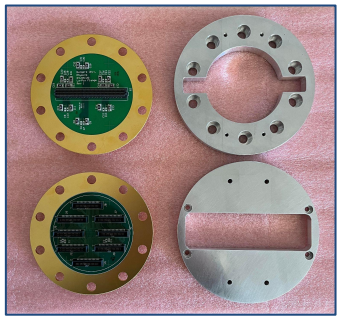
Approaching ~$0.10/channel, ~$10K/m^2

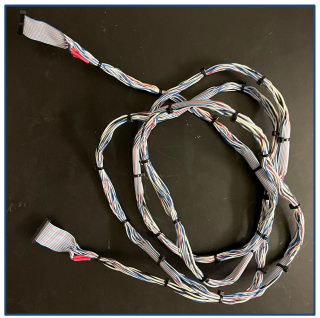
…100's of ASICs

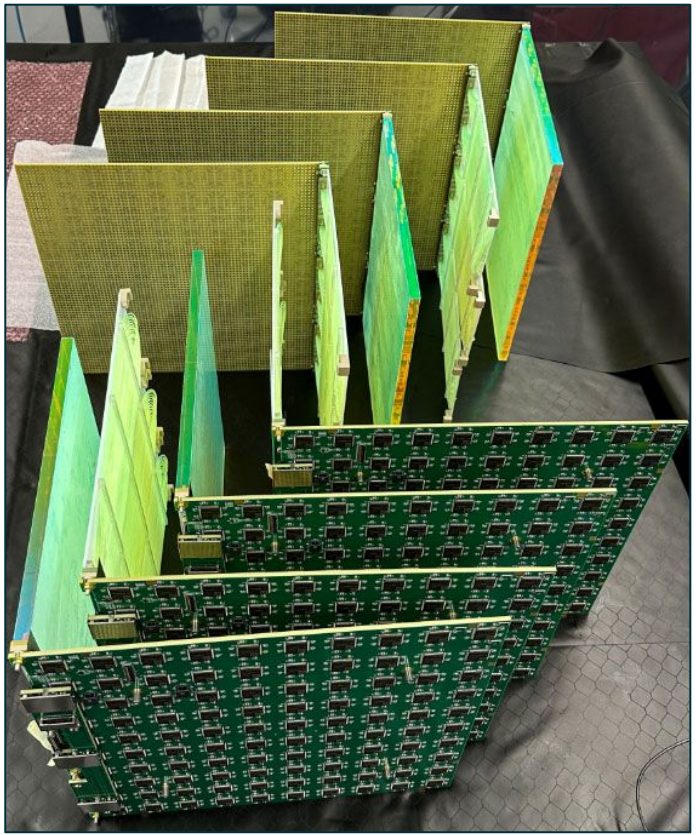
…I/O with ASICs

…handles DAQ and configuration for up to 8 tiles



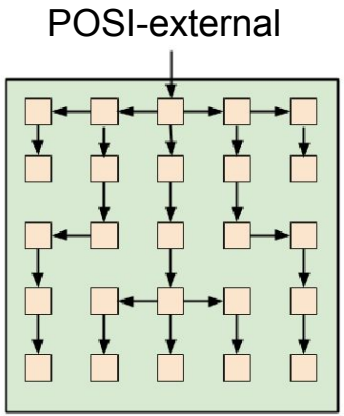




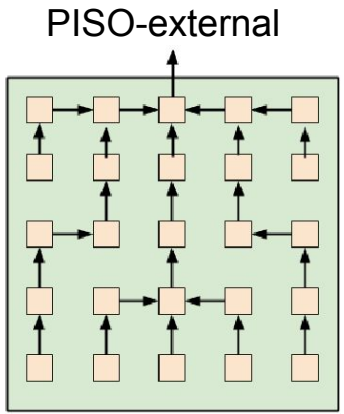


Hydra I/O Networking

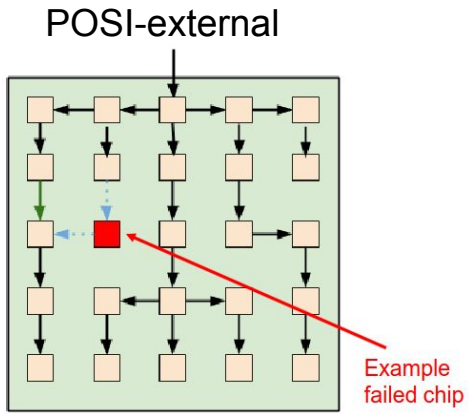
- 2022 R&D 100 Award
- PISO/POSI pair on every edge for chip-to-chip UART data transmission
  - Digital multiplexing O(10^3) channels per I/O channel
- Enables configurable network paths to send data in/out
  - Avoid single point failures
- Multiple (4) external links per tile PCB (not pictured)



Configuration commands in.



Data packets out.



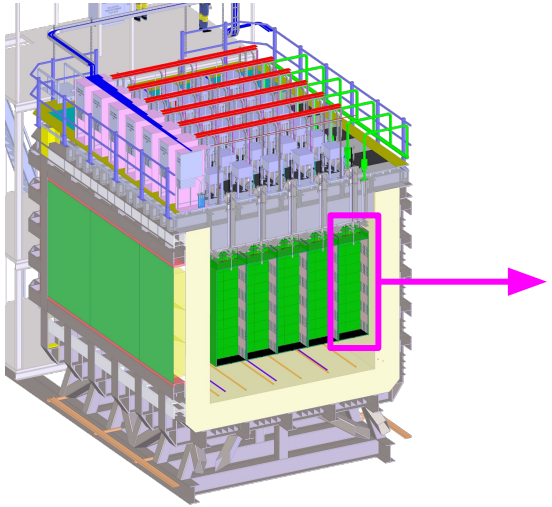
Alternative network to avoid problematic chip.

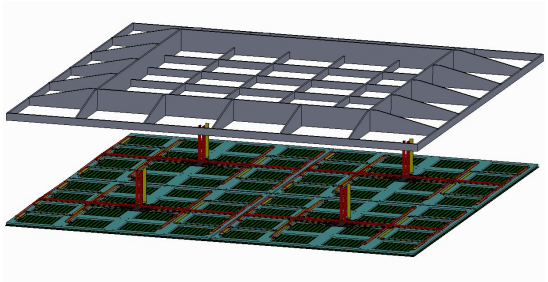
LArPix System Applications

- DUNE LArTPC Near Detector (ND-LAr)
  - ~14,000,000 pixels across 5x7 array of 3x1x1 m^3 modules
  - Central cathode and 2 pixelated anode planes per module
  - Optically isolated TPCs

- Potentially a “phase 2” DUNE FD module
  - order of magnitude larger than ND
  - 8x8 pixel tile grid compatible with existing protoDUNE-VD infrastructure

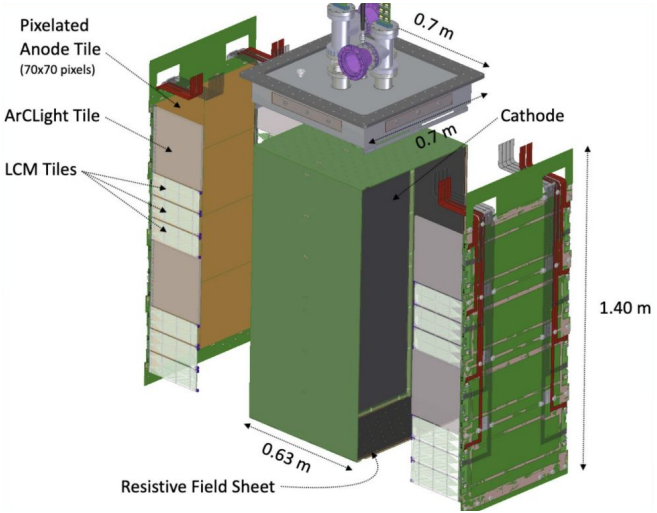
- ….

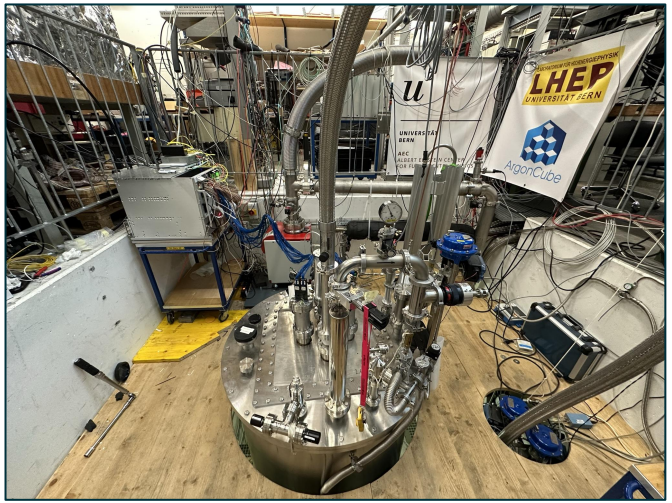




2x2 Demonstrator

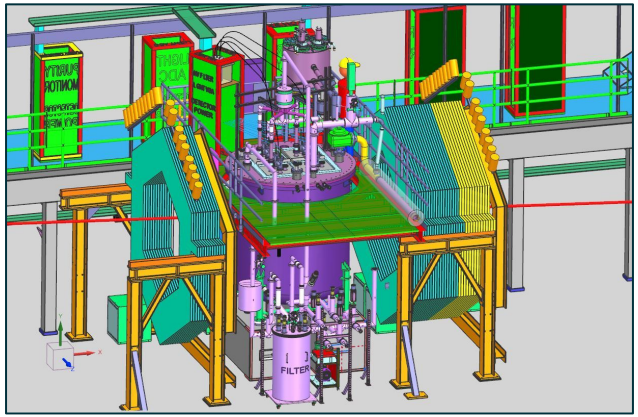
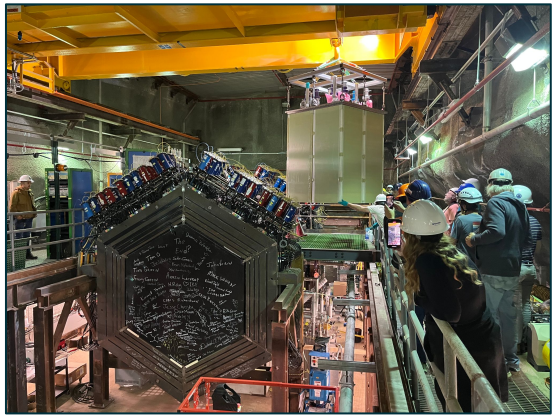
- Demonstration of ND-LAr design
- 2x2 array of 1.2 x 0.6 x 0.6 m^3 modules containing >300K pixel channels
- 4 modules operated individually at Bern
  - O(10^8) cosmic events

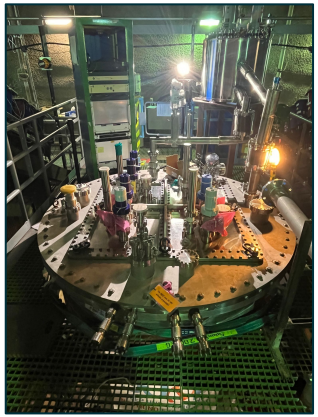




2x2 Demonstrator

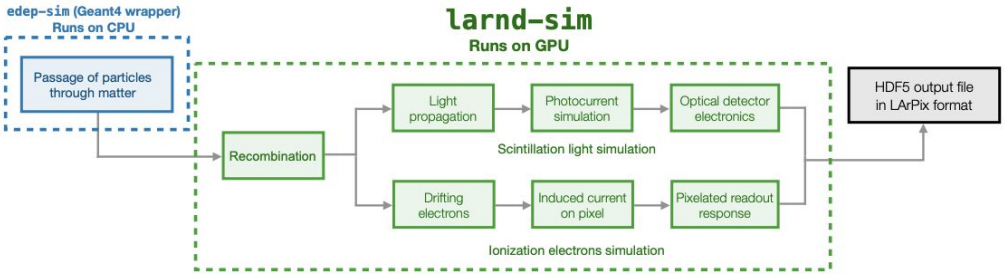
- Demonstration of ND-LAr design
- 2x2 array of 1.2 x 0.6 x 0.6 m^3 modules containing >300K pixel channels
- 4 modules operated individually at Bern
  - O(10^8) cosmic events
- @ Fermilab underground facility (MINOS hall) between repurposed Minerva planes
- Will image neutrino interactions in the GeV-energy regime from the NuMI beam

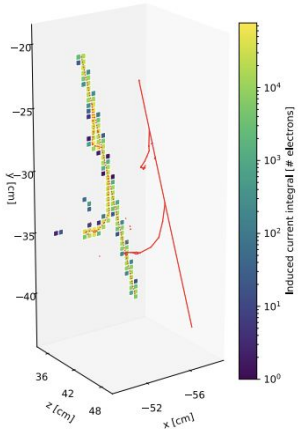



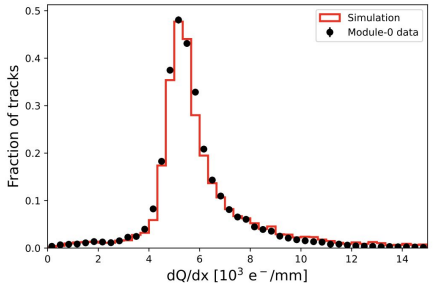


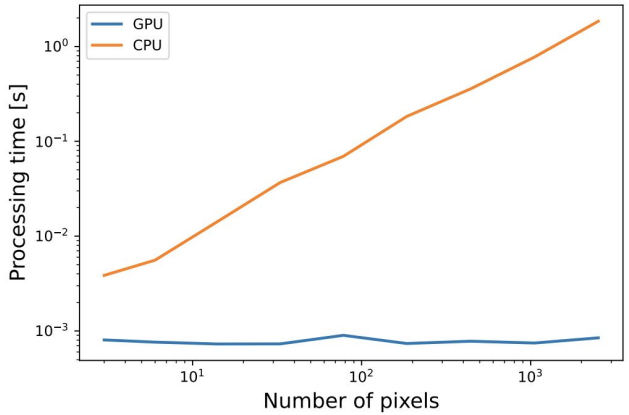
Simulation

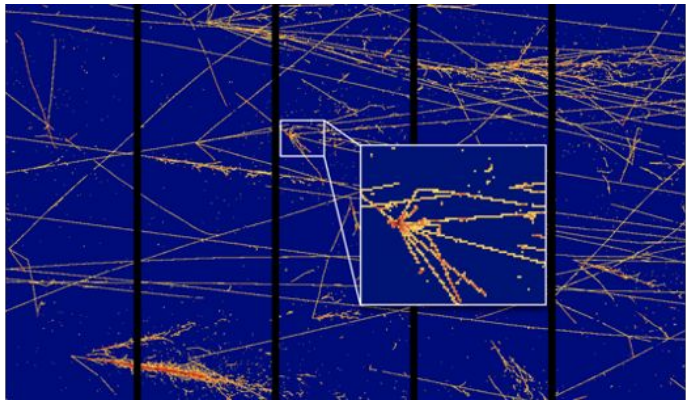
JINST 18 P04034 (2023)











Closing Remarks

- 2016-2018: LArPix v1 proof of principle ASIC
- 2023-2024: LArPix v2 system deployed in a 2.5 tonne active mass LArTPC neutrino detector including >330,000 channels (2x2 Demonstrator)

- Continuing to develop the system and scale up implementations, stay tuned!

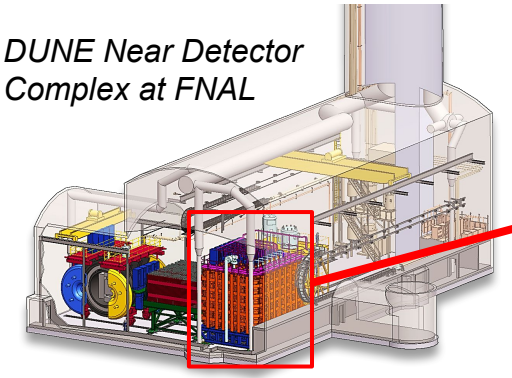
Component	LArPix ASIC	Pixel tile	PACMAN controller
R&D focus	– Correlated double sampling → noise – 10-bit ADC → resolution – Robustness	– Increase size 60% – Optimize pixel pad geometry – Shielding layer to reduce inductive	– 10-tile capable – Differential analog monitor with ADC

Backup

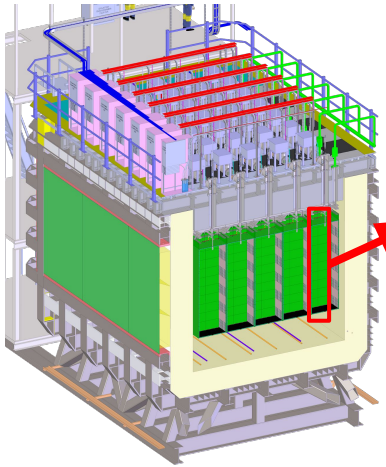
LArPix @ DUNE Near Detector

- The LArPix ASIC will read out the charge signals from DUNE near detector LArTPC component, ND-LAr
- ~15 million channels (3.8 x 3.8 mm^2 pixel pads) readout by ~0.25 million ASICs

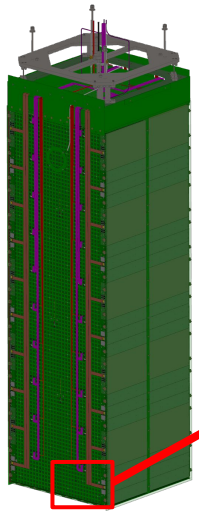
DUNE Near Detector Complex at FNAL



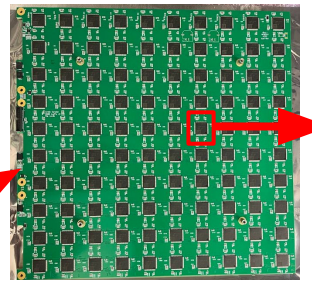
ND-LAr Detector



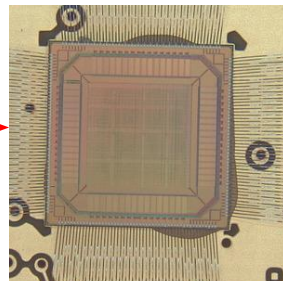
1/35 ND-LAr Modules



60%-size pixel tile



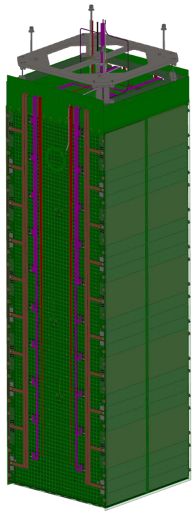
LArPix ASIC



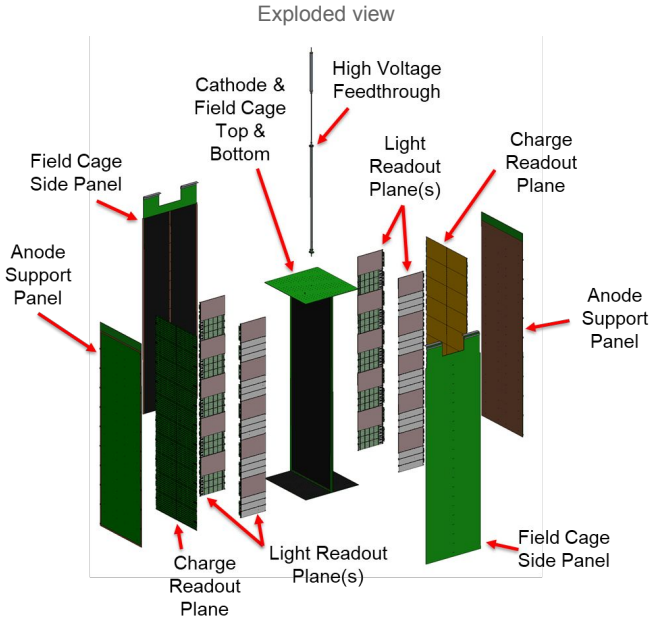
ArgonCube Design

- Modular approach, O(50 cm) drifts
- Central cathode provides drift field for 2 optically isolated TPCs
- Resistive shell field cage
- Light detection modules installed along the field cage
- Anode planes outfitted with tiles of PCB components containing gold-plated pixel pads on one side and LArPix ASICs on the other

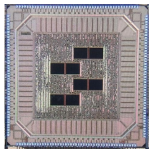
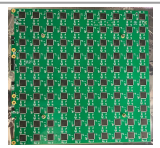
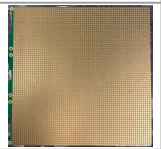
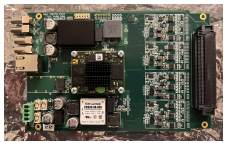
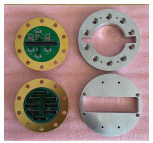
ArgonCube Module



Exploded view



LArPix Readout System Overview

Item	Quantity for 2x2	Quantity for FSD module	Quantity for ND-LAr
LArPix ASIC 	6,400 + 3,200	6,400 + 3,200	224,000 + ~100,000 (Actual spare count will be based on ASIC yield of first production wafer run)
Tile PCB  	64 + 16 (100 ASICs/Tile)	40 + 10 (160 ASICs/Tile)	1,400 + 280 (160 ASICs/Tile)
Pacman 	8 + 4	4 + 2 + 4	140 + 20
Cryogenic cables 	64 + 8	40 + 10	1,400 + 280
Feedthrough assembly 	8 + 8	2 + 2	70 + 7

1.2 MW LBNF Spill on ND-LAr